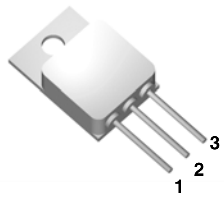
STRH100N10FSY1
STRH100N10FSY3

N-channel 100V - 0.024Ω - TO-254AA rad-hard low gate charge STripFET™ Power MOSFET

Features

Type	V_{DSS}
STRH100N10FSY1	100 V
STRH100N10FSY3	100 V

- Low $R_{DS(on)}$
- Fast switching
- Single event effect (SEE) hardned
- Low total gate charge
- Light weight
- 100% avalanche tested
- Application oriented characterization
- Hermetically sealed
- Heavy ion SOA
- 100 kRad TID
- SEL & SEGR with 34Mev/cm²/mg LET ions



Applications

- Satellite
- High reliability

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to sustain high TID and provide immunity to heavy ion effects. It is therefore suitable as power switch in mainly high-efficiency DC-DC converters. It is also intended for any application with low gate charge drive requirements.

Figure 1. Internal schematic diagram

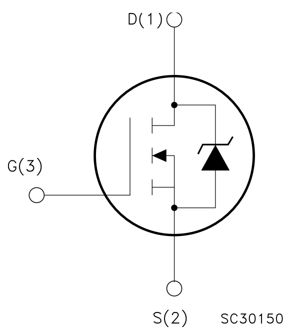


Table 1. Device summary

Order codes	Marking	Package	Packaging
STRH100N10FSY1 (1)	RH100N10FSY1	TO-254AA	Individual strip pack
STRH100N10FSY3 (2)	RH100N10FSY3	TO-254AA	Individual strip pack

1. Mil temp range
2. Space flights parts (full ESCC flow screening)

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings (pre-irradiation)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	100	V
V_{GS}	Gate-source voltage	±14	V
I_D (1)	Drain current (continuous) at T_C= 25 °C	72	A
I_D (1)	Drain current (continuous) at T_C= 100 °C	52	A
I_{DM} (2)	Drain current (pulsed)	288	A
P_{TOT} (1)	Total dissipation at T_C= 25 °C	170	W
dv/dt (3)	Peak diode recovery voltage slope	3.7	V/ns
T_{stg}	Storage temperature	–55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. Rated according to the Rthj-case + Rthc-s
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 80$ A, di/dt ≤ 1100A/µs, V_{DD} = 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	0.52	°C/W
Rthc-s	Case-to-sink typ	0.21	°C/W
Rthj-amb	Thermal resistance junction -amb max	48	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	40	A
E_{AS}	Single pulse avalanche energy (starting Tj=25 °C, I_D= I_{AR}, V_{DD}=50 V)	824	mJ
E_{AR}	Repetitive avalanche(1)	53	mJ

1. Pulse number = 10; f= 10 KHz; D.C. = 50%

2 Electrical characteristics

(T_{CASE} = 25°C unless otherwise specified)

2.1 Pre-irradiation

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	80% BV_{Dss}			10	µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±14 V			±100	nA
BV_{DSS}	Drain-to-source breakdown voltage	V_{GS} = 0V, I_D = 1m A	100			V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 1m A	2		4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 12V; I_D = 36 A		0.024	0.028	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{GS} = 0, V_{DS} = 25 V, f=1MHz	5280 568 168	6600 710 210	7980 852 252	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-to-source charge Gate-to-drain (“Miller”) charge	V_{DD} = 50 V, I_D = 36 A, V_{GS}=12 V	128 25.6 40	160 32 50	192 38.4 60	nC nC nC
R_G	Gate input resistance	f=1MHz Gate DC Bias=0 Test signal level=20mV open drain	1.6	2	2.4	Ω

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 50 V, I_D = 40 A, R_G = 4.7 Ω, V_{GS} = 12 V	29.6 48 92 46.4	37 60 115 58	44.4 72 138 69.6	ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				72 288	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 72 A, V_{GS} = 0			1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 72 A, di/dt = 100 A/µs V_{DD}= 50 V, Tj = 25 °C	265	332 4.48 27	398	ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 72 A, di/dt = 100 A/µs V_{DD}= 50 V, Tj = 150 °C	304	380 5.62 29.6	456	ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.2 Post-irradiation

The ST rad-hard Power MOSFETs are tested to verify the radiation capability. The technology is extremely resistant to assurance well functioning of the device inside the radiation environments. Every manufacturing lot is tested for total ionizing dose.

(@Tj=25 °C up to 100 Krad [a])

Table 9. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	80% BV_{Dss}			10	µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±14 V			±100	nA
BV_{DSS}	Drain-to-source breakdown voltage	V_{GS} = 0V, I_D = 1 mA	100			V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 1 mA	2		4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 12 V; I_D = 36 A		0.024	0.028	Ω

a. According to ESCC 22900 specification, Co60 gamma rays, dose rags:0.1rad/sec.

Table 10. Single event effect, SOA(1)

Ion	Let (Mev/(mg/cm^2)	Energy (MeV)	Range (µm)	V_{DS} (V) @V_{GS}0V
Kr	34	316	43	100
Xe	55.9	459	43	100

1. Rad-Hard Power MOSFETs have been characterized in heavy ion environment for single event effect (SEE). Single event effect characterization is illustrated

Figure 2. Bias condition during radiation

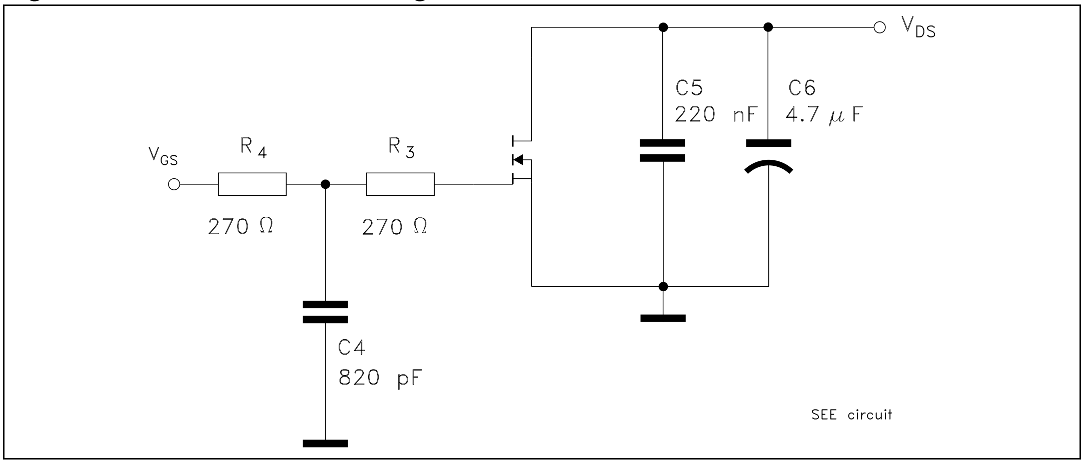


Table 11. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				72 288	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 72 A, V_{GS} = 0			1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 72 A, di/dt = 100 A/µs V_{DD}= 50 V, Tj = 25 °C	265	332 4.48 27	398	ns µC A
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1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.3 Electrical characteristics (curves)

Figure 3. Safe operating area

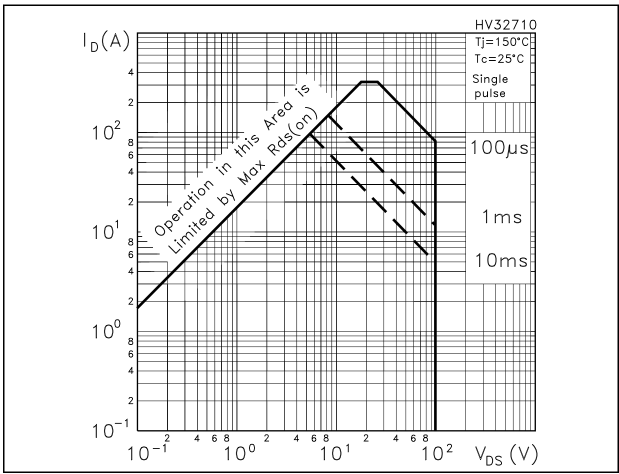


Figure 4. Thermal impedance

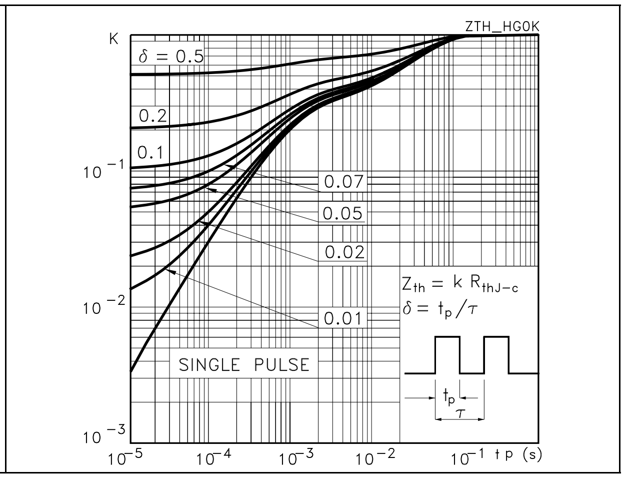


Figure 5. Output characteristics

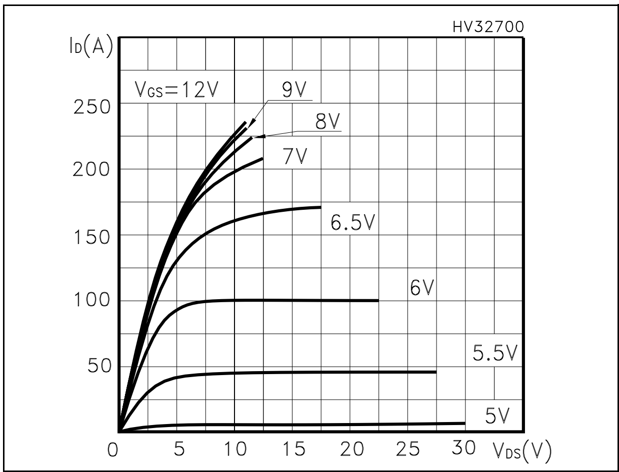


Figure 6. Transfer characteristics

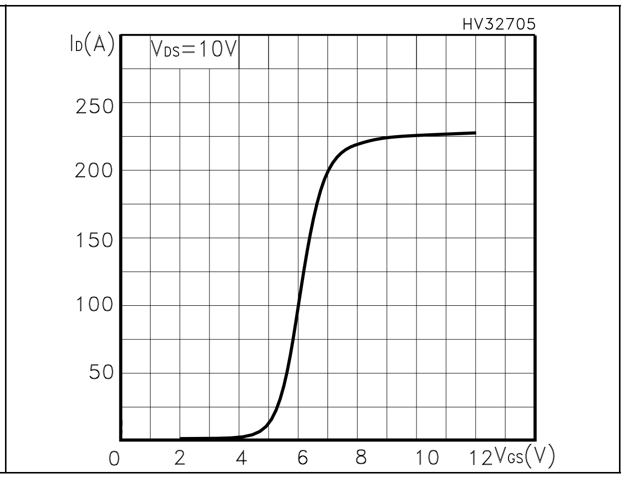


Figure 7. Gate charge vs gate-source voltage

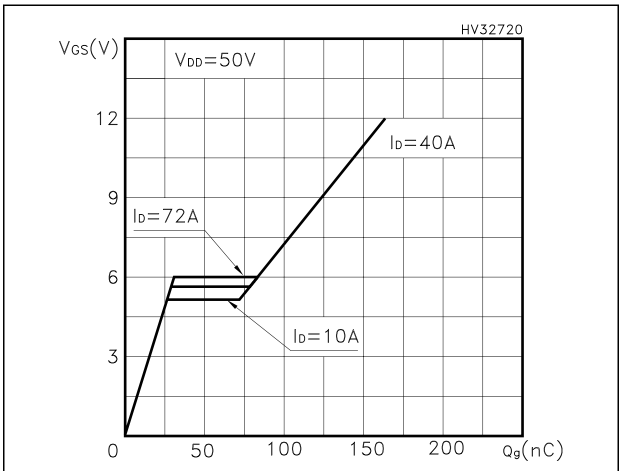


Figure 8. Capacitance variations

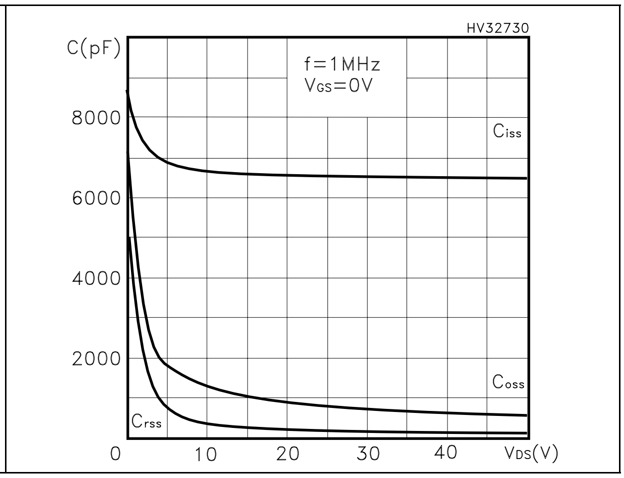


Figure 9. Normalized BV_{DSS} vs temperature

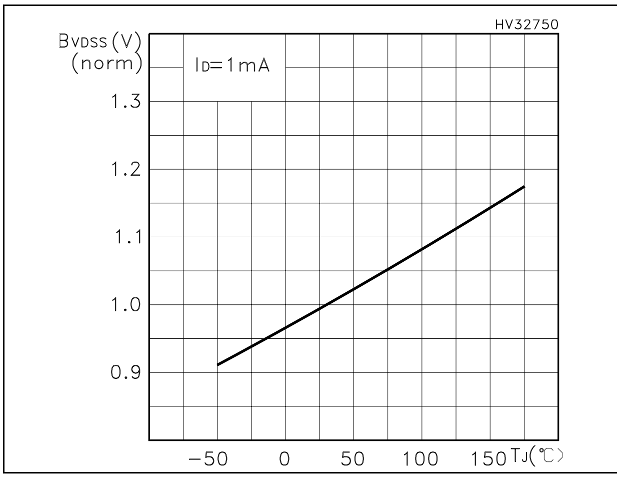


Figure 10. Static drain-source on resistance

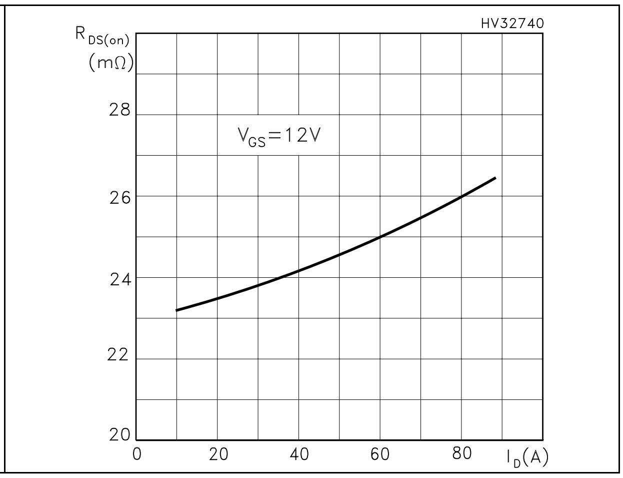


Figure 11. Normalized gate threshold voltage vs temperature

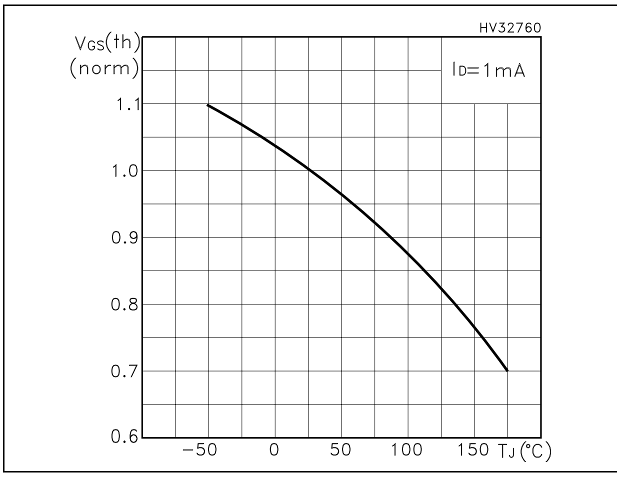


Figure 12. Normalized on resistance vs temperature

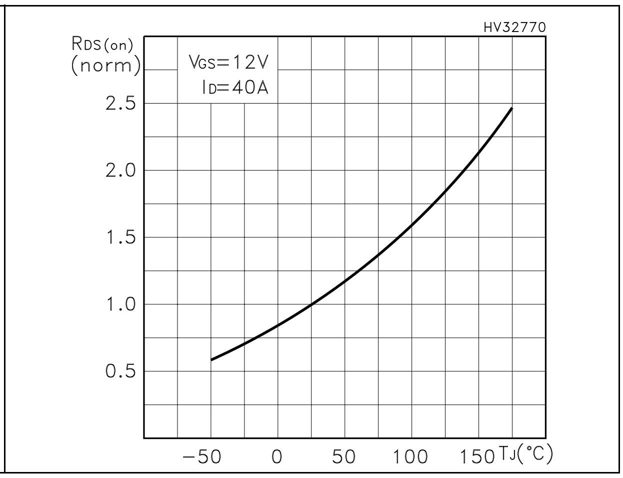
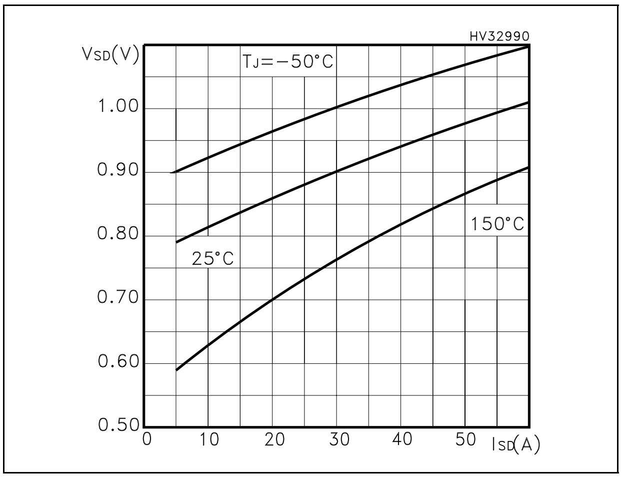
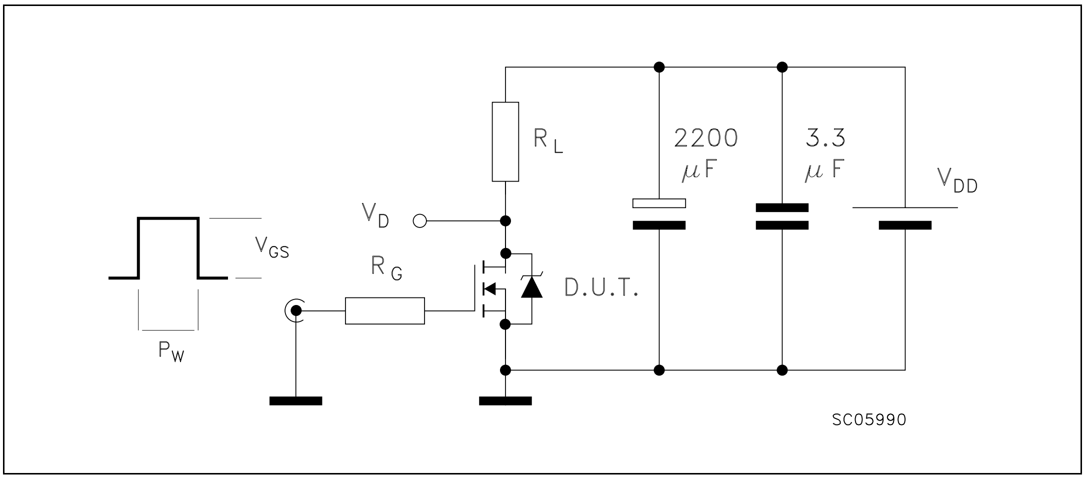


Figure 13. Source drain-diode forward characteristics



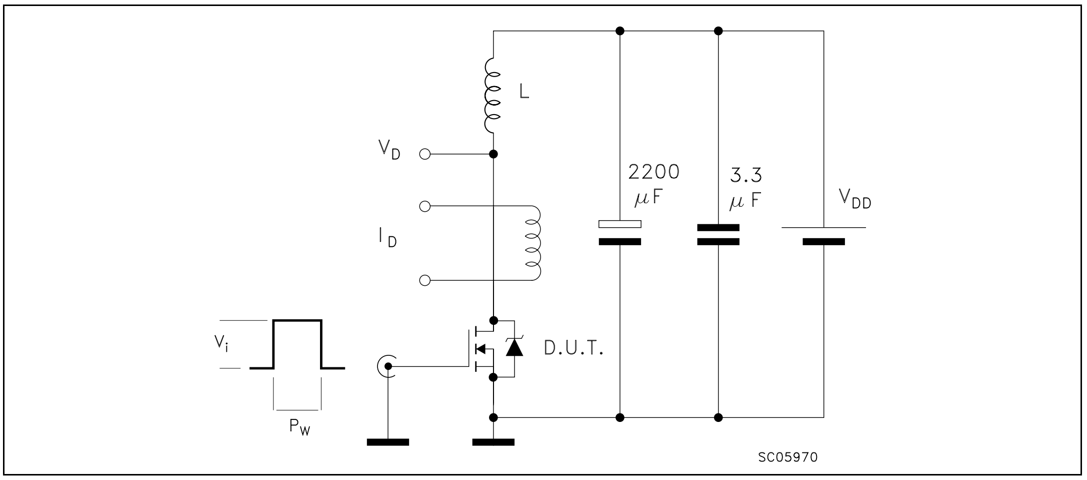
3 Test circuit

Figure 14. Switching times test circuit for resistive load (1)



1. Max driver V_{GS} slope = 1V/ns (no DUT)

Figure 15. Unclamped inductive load test circuit (single pulse and repetitive)



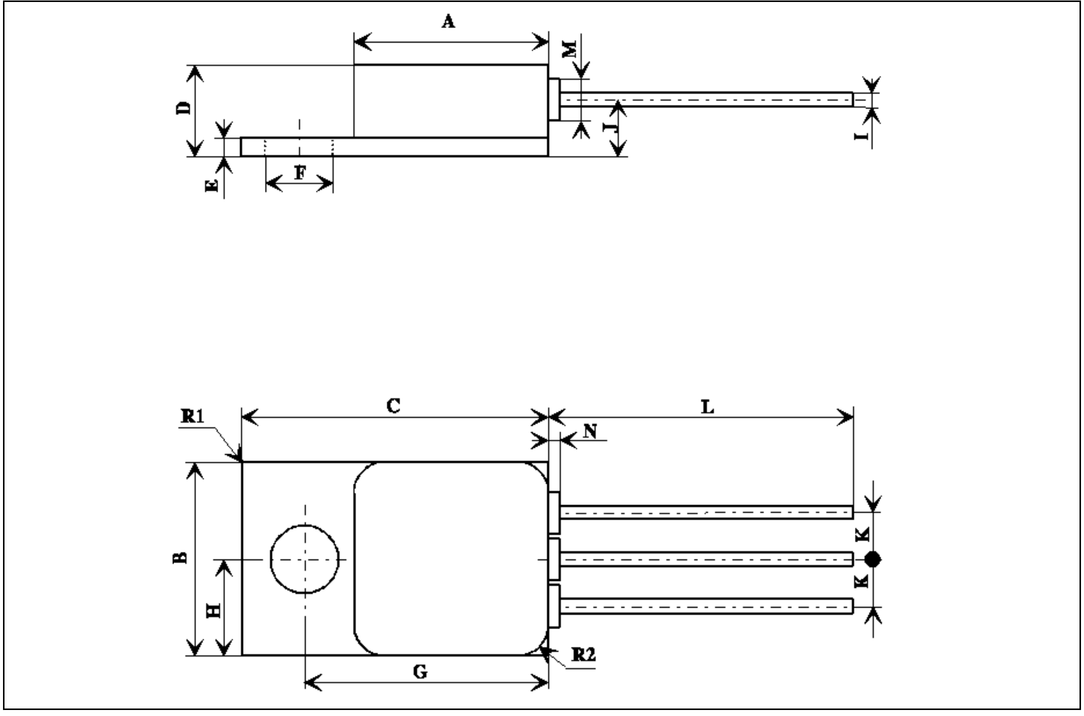
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

Table 12. TO-254AA mechanical data

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	13.59		13.84	0.535		0.545
B	13.59		13.84	0.535		0.545
C	20.07		20.32	0.790		0.80
D	6.32		6.60	0.249		0.260
E	1.02		1.27	0.040		0.050
F	3.53		3.78	0.139		0.149
G	16.89		17.40	0.665		0.685
H		6.86			0.270	
I	0.89		1.14	0.035		0.045
J		3.81			0.150	
K		3.81			0.150	
L	12.95		14.50	0.510		0.570
M		3.05			0.120	
N			0.71			0.025
R1			1.0			0.040
R2		1.65			0.065	

Figure 16. Mechanical drawing



5 Revision history

Table 13. Document revision history

Date	Revision	Changes
03-Jul-2006	1	First release
18-Dec-2006	2	*Figure 3.* has been updated
15-Mar-2007	3	Complete version
22-Oct-2007	4	Note 2 on device summary has been updated
14-Nov-2007	5	Added figures: *2* and *15*. Updated values on tables: *6*, *7*, *8* and *11* Minor text changes to improve readability