MICRON

MT58LC256K16/18G1
256K x 16/18 SYNCBURST SRAM

NEW ■ SYNCBURST PIPELINED – 2.5V I/O

SYNCHRONOUS SRAM

256K x 16/18 SRAM

+3.3V SUPPLY, +2.5V I/O, PIPELINED, BURST COUNTER AND SINGLE-CYCLE DESELECT

FEATURES

- Fast access times: 4.5, 5, 5.5, 6 and 7ns
- Fast OE# access time: 4.5, 5, 5.5 and 6ns
- +3.3V +0.3V/-0.165V power supply (Vcc)
- Separate +2.5V +0.4V/-0.125V isolated output buffer supply (VccQ)
- 3.3V-tolerant inputs
- SNOOZE MODE for reduced power standby
- Single-cycle disable (Pentium™ BSRAM compatible)
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock controlled, registered, address, data I/O and control for fully pipelined applications
- Internally self-timed WRITE cycle
- Burst control pin (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP package for high density, high speed
- Low capacitive bus loading
- High 30pF output drive capability at rated access time
- DIMMs also available
- x16 or x18 versions available

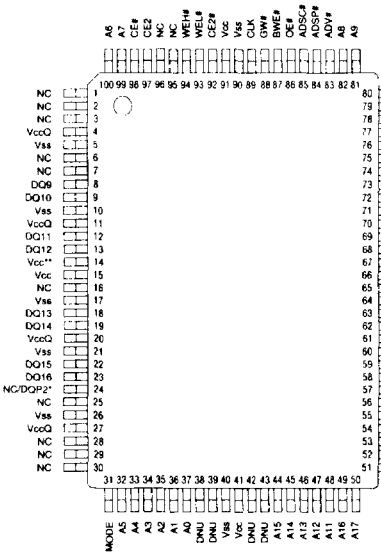
OPTIONS

	MARKING
• Timing	
4.5ns access/8ns cycle	-4.5
5ns access/8.5ns cycle	-5
5.5ns access/10ns cycle	-5.5
6ns access/11.1ns cycle	-6
7ns access/20ns cycle	-7
• Configurations	
256K x 16	MT58LC256K16G1
256K x 18	MT58LC256K18G1
• Package	
100-pin TQFP	LG

• Part Number Example: MT58LC256K18G1LG-5

PIN ASSIGNMENT (Top View)

100-Pin TQFP
(SA-1)



* No Connect (NC) is used in the x16 version. Parity (DQPx) is used in the x18 version.

** Pin 14 does not have to be directly connected to Vcc as long as the input voltage is ≥ VIH.

GENERAL DESCRIPTION

The Micron SyncBurst SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using an advanced CMOS process.

The MT58LC256K16/18G1 SRAM integrates a 256K x 16 or 256K x 18 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), burst control inputs (ADSC#, ADSP#, ADV#) byte write enables (WEH#, WEL#, BWE#) and global write (GW#).

Asynchronous inputs include the output enable (OE#), clock (CLK) and snooze enable (ZZ). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. The data-out (Q), enabled by OE#, is also asynchronous. WRITE cycles can be from 1 to 2 bytes wide as controlled by the write control inputs.

Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#)

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GENERAL DESCRIPTION (continued)

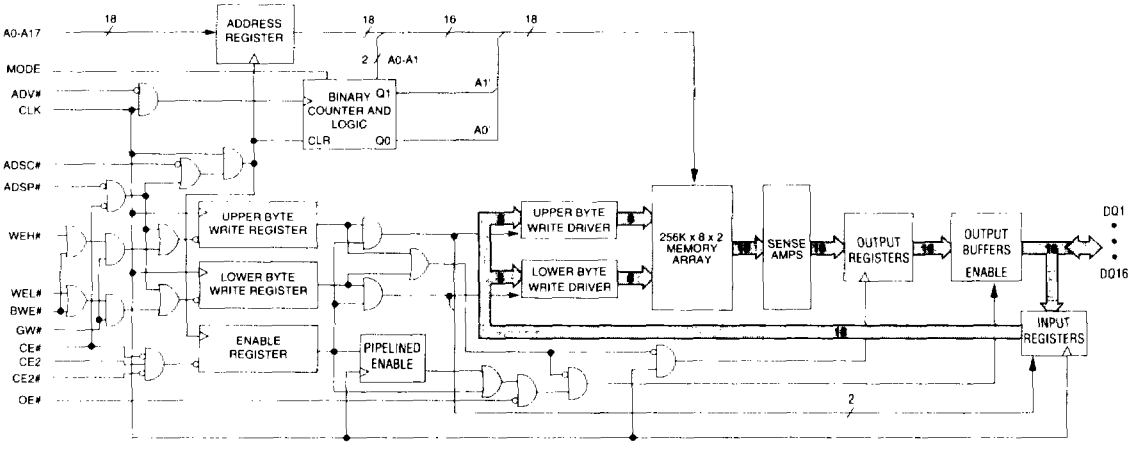
input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV#).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. WEL# controls DQ1-DQ8 and DQP1. WEH# controls DQ9-DQ16 and DQP2, conditioned by BWE# being LOW. GW# LOW causes all bytes to be written. Parity bits are available on the x18 version only. WRITE pass-through makes written data immediately available at the output register during the READ cycle following a WRITE as controlled solely by OE# to improve cache system response.

This device incorporates a single-cycle deselect feature during READ cycles. If the device is immediately deselected after a READ cycle, the output bus goes to a High-Z state ^{t}KQHZ ns after the rising edge of clock. This feature can be useful in eliminating bus contention when depth expansion is used in cache applications.

The MT58LC256K16/18G1 operates from a +3.3V power supply and all inputs and outputs are can communicate with other 2.5V I/O. All inputs are 3.3V-tolerant and can be used in mixed 3.3V and 2.5V systems. The device is ideally suited for systems that benefit from a wide synchronous data bus and 2.5V I/O. These devices are also ideal in generic 16-, 18-, 32-, 36-, 64- and 72-bit-wide applications.

FUNCTIONAL BLOCK DIAGRAM
256K x 16



NOTE: 1. Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

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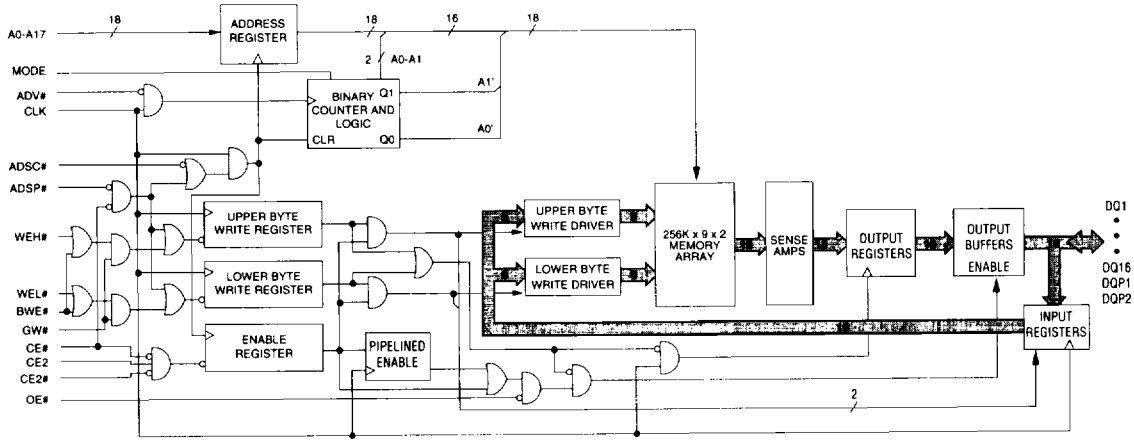
FUNCTIONAL BLOCK DIAGRAM
256K x 18



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PIN DESCRIPTIONS

TQFP PINS	SYMBOL	TYPE	DESCRIPTION
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 80, 48, 47, 46, 45, 44, 49, 50	A0-A17	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
94, 93	WEH#, WEL#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. WEL# controls DQ1-DQ8 and DQP1. WEH# controls DQ9-DQ16 and DQP2. Data I/O are tristated if either of these inputs are LOW.
87	BWE#	Input	Byte Write Enable: This active LOW input permits byte write operations and must meet the setup and hold times around the rising edge of CLK.
88	GW#	Input	Global Write: This active LOW input allows a full 18-bit WRITE to occur independent of the BWE# and WE#n lines and must meet the setup and hold times around the rising edge of CLK.
89	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions the internal use of ADSP#. This input is sampled only when a new external address is loaded.
92	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded.
97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded.
86	OE#	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
83	ADV#	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an ADSP# cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
84	ADSP#	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and ADSC#, but dependent upon CE# being LOW.

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PIN DESCRIPTIONS (continued)

TQFP PINS	SYMBOL	TYPE	DESCRIPTION
85	ADSC#	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if CE# is LOW. ADSC# is also used to place the chip into power-down state when CE# is HIGH.
31	MODE	Input	Mode: This input selects the burst sequence. A LOW on this pin selects LINEAR BURST. NC or HIGH on this pin selects INTERLEAVED BURST. Do not alter input state while device is operating.
64	ZZ	Input	Snooze Enable: This active HIGH asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When active, all other inputs are ignored.
58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23	DQ1-DQ16	Input/ Output	SRAM Data I/O: Low Byte is DQ1-DQ8. High Byte is DQ9-DQ16. Input data must meet setup and hold times around the rising edge of CLK.
74, 24	NC/DQP1 NC/DQP2	No Connect/ Input/Output	No Connect /Parity Data I/O: On the x18 device, Low Byte Parity is DQP1. High Byte Parity isDQP2. On the x16 device, these pins are No Connect (NC).
14, 15, 41, 65, 91	V_{CC}	Supply	Power Supply: +3.3V +10%/-5%. Pin 14 does not have to be directly connected to V_{CC} as long as the input voltage is $\geq V_{IH}$.
4, 11, 20, 27, 54, 61, 70, 77	$V_{CC}Q$	Supply	Isolated Output Buffer Supply: +2.5V +0.4V/-0.125V.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground: GND
38, 39, 42, 43	DNU	-	Do Not Use: These signals may either be unconnected or wired to GND to improve package heat dissipation.
1, 2, 3, 6, 7, 16, 25, 28, 29, 30, 51, 52, 53, 56, 57, 66, 75, 78, 79, 95, 96	NC	-	No Connect: These signals are not internally connected. These signals may be connected to ground to improve package heat dissipation.

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INTERLEAVED BURST ADDRESS TABLE (MODE = NC OR HIGH)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE (MODE = GND)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PARTIAL TRUTH TABLE FOR WRITE COMMANDS

Function	GW#	BWE#	WEL#	WEH#
READ	H	H	X	X
READ	H	L	H	H
WRITE Low Byte	H	L	L	H
WRITE High Byte	H	L	H	L
WRITE all bytes	H	L	L	L
WRITE all bytes	L	X	X	X

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TRUTH TABLE

OPERATION	ADDRESS USED	CE#	CE2#	CE2	ZZ	ADSP#	ADSC#	ADV#	WRITE#	OE#	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	L	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	H	L	X	X	X	L-H	High-Z
SNOOZE MODE, Power-down	None	X	X	X	H	X	X	X	X	X	X	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. WRITE#=L means any one or more byte write enable signals (WEL# or WEH#) and BWE# are LOW or GW# is LOW. WRITE#=H means all byte write enable signals and GW# are HIGH.
2. WEL# enables WRITEs to DQ1-DQ8, DQP1. WEH# enables WRITEs to DQ9-DQ16, DQP2. DQP1 and DQP2 are available on the x18 version only.
3. All inputs except OE# must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a WRITE operation following a READ operation, OE# and ZZ must be HIGH before the input data setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. ADSP# LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and BWE# LOW or GW# LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
Voltage on $V_{CC}Q$ Supply Relative to V_{SS} .... -0.5V to +4.6V
V_{IN} (DQxx) ..... -0.5V to $V_{CC}Q$+0.5V
V_{IN} (inputs) ..... -0.5V to V_{CC}+0.5V
Storage Temperature (plastic) ..... -55°C to +150°C
Junction Temperature** ..... +150°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See Micron Technical Note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = +3.3V +0.3V/-0.165V; $V_{CC}Q$ = +2.5V +0.4V/-0.125V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Databus (DQxx)	$V_{IH}Q$	1.7	$V_{CC}Q$+0.3	V	1, 2
	Inputs	V_{IH}	1.7	V_{CC}+0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.7	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	13
Output Leakage Current	Output(s) disabled, 0V ≤ V_{IN} ≤ $V_{CC}Q$ (DQxx)	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	1.7		V	1
	I_{OH} = -1.0mA	V_{OH}	2.0		V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}		0.7	V	1
	I_{OL} = 1.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.135	3.6	V	1
Isolated Output Buffer Supply		$V_{CC}Q$	2.375	2.9	V	1

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = +3.3V +0.3V/-0.165V; VccQ = +2.5V +0.4V/-0.125V unless otherwise noted)

				MAX						
DESCRIPTION	CONDITIONS	SYM	TYP	-4.5	-5	-5.5	-6	-7	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC MIN; Vcc = MAX; VccQ = MAX; outputs open	Icc	TBD	350	340	300	265	150	mA	3, 11, 12
Power Supply Current: Idle	Device selected; Vcc = MAX; VccQ = MAX ADSC#, ADSP#, GW#, BW#s, ADV# ≥ V_{IH}; inputs ≤ Vss +0.2 or ≥ Vcc -0.2; Data (DQxx) ≤ Vss +0.2 or ≥ VccQ -0.2; cycle time ≥ ^tKC MIN	Icc1	TBD	80	80	80	75	50	mA	11, 12
CMOS Standby	Device deselected; Vcc=MAX; VccQ=MAX inputs ≤ Vss +0.2 or ≥ Vcc -0.2; Data (DQxx) ≤ Vss +0.2 or ≥ VccQ -0.2; all inputs static; CLK frequency = 0	Isb2	TBD	5	5	5	5	5	mA	11, 12
TTL Standby	Device deselected; Vcc = MAX; VccQ = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; CLK frequency = 0	Isb3	TBD	25	25	25	25	25	mA	11, 12
Clock Running	Device deselected; Vcc=MAX; VccQ=MAX inputs ≤ Vss +0.2 or ≥ Vcc -0.2; Data (DQxx) ≤ Vss +0.2 or ≥ VccQ -0.2; cycle time ≥ ^tKC MIN	Isb4	TBD	80	80	80	75	50	mA	11, 12

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Control Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	3	4	pF	4
Input/Output Capacitance (DQ)	VccQ = 2.5V	C_O	6	8	pF	4
Address and Clock Input Capacitance		C_A	2.5	3	pF	4

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air, soldered on 4.25 x 1.125 inch 4-layer PCB	θ_{JA}	TBD	°C/W	4
Thermal resistance - Junction to Case		θ_{JC}	TBD	°C/W	4

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = +3.3V +0.3V/-0.165V; VccQ = +2.5V +0.4V/-0.125V)

DESCRIPTION		-4.5		-5		-5.5		-6		-7			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock													
Clock cycle time	^tKC	8		8.5		10		11.1		20		ns	
Clock HIGH time	^tKH	2.5		2.5		3.2		3.8		6		ns	
Clock LOW time	^tKL	2.5		2.5		3.2		3.8		6		ns	
Output Times													
Clock to output valid	^tKQ		4.5		5		5.5		6		8	ns	
Clock to output invalid	^tKQX	1.5		2		2		2		2		ns	
Clock to output in Low-Z	^tKQLZ	1.5		2		2		2		2		ns	4, 6, 7
Clock to output in High-Z	^tKQHZ	2	4.5	2	5	2	5.5	2	6	2	6	ns	4, 6, 7
OE# to output valid	^tOEQ		4.5		4.8		5.5		6		6	ns	9
OE# to output in Low-Z	^tOELZ	0		0		0		0		0		ns	4, 6, 7
OE# to output in High-Z	^tOEHZ		4.5		4.8		5.5		6		6	ns	4, 6, 7
Setup Times													
Address	^tAS	2.0		2.0		2.0		2.5		3.0		ns	8, 10
Address Status (ADSC#, ADSP#)	^tADSS	2.0		2.0		2.0		2.5		3.0		ns	8, 10
Address Advance (ADV#)	^tAAS	2.0		2.0		2.0		2.5		3.0		ns	8, 10
Write Signals (WEL#, WEH#, BWE#, GW#)	^tWS	2.0		2.0		2.0		2.5		3.0		ns	8, 10
Data-in	^tDS	2.0		2.0		2.0		2.5		3.0		ns	8, 10
Chip Enables (CE#, CE2#, CE2)	^tCES	2.0		2.0		2.0		2.5		3.0		ns	8, 10
Hold Times													
Address	^tAH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Address Status (ADSC#, ADSP#)	^tADSH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Address Advance (ADV#)	^tAAH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Write Signals (WEL#, WEH#, BWE#, GW#)	^tWH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Data-in	^tDH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Chip Enables (CE#, CE2#, CE2)	^tCEH	0.5		0.5		0.5		0.5		0.5		ns	8, 10

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AC TEST CONDITIONS

Input pulse levels	Vss to 2.5V
Input rise and fall times	2.5ns
Input timing reference levels	1.25V
Output reference levels	1.25V
Output load	See Figures 1 and 2

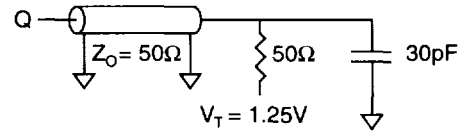

Fig. 1 OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +4.6V$ for $t \leq {}^tKC/2$ for $I \leq 20mA$
   Undershoot: $V_{IL} \geq -0.7V$ for $t \leq {}^tKC/2$ for $I \leq 20mA$
   Power-up: $V_{IH} \leq +3.6V$, $V_{CC} \leq 3.135V$ and $V_{CC}Q \leq 2.375V$ for $t \leq 200ms$
3. Icc is given with no output current. Icc increases with faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified using Fig. 1 with C_L = 5pF versus 30pF. Transition is measured ±150mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$.
8. A WRITE cycle is defined by at least one byte write enable LOW and ADSP# HIGH for the required setup and hold times. A READ cycle is defined by all byte write enables HIGH and (ADSC# or ADV# LOW) or ADSP# LOW for the required setup and hold times.
9. OE# is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either ADSP# or ADSC# is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK (when either ADSP# or ADSC# is LOW) to remain enabled.
11. "Device Deselected" means device is in POWER-DOWN mode as defined in the Truth Table. "Device Selected" means device is active (not in POWER-DOWN mode).
12. Typical values are measured at Vcc = 3.3V, VccQ = 2.5V, 25°C, and 15ns cycle time.
13. MODE pin has an internal pull-up and exhibits an input leakage current of ±10µA.

LOAD DERATING CURVES

Micron 256K x 16 and 256K x 18 Synchronous SRAM timing is dependent upon the capacitive loading on the outputs. The data sheet is written assuming a load of 30pF.

Consult the factory for copies of I/O current versus voltage curves. For capacitive loading derating curves see Micron Technical Note TN-05-20, "3.3V SRAM Capacitive Loading."

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SNOOZE MODE

SNOOZE MODE is a low current, "power-down" mode in which the device is deselected and current is reduced to I_{SB2}. The duration of SNOOZE MODE is dictated by the length of time the ZZ pin is in a HIGH state. After entering SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored.

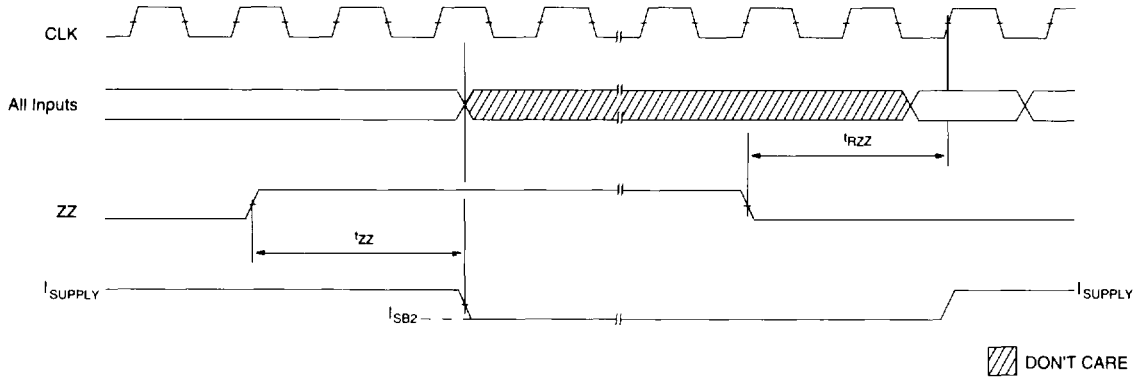
The ZZ pin (pin 64) is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When the ZZ pin becomes a logic HIGH, I_{SB2} is guaranteed after the setup time ^tZZ is met. Any access pending when entering SNOOZE MODE is not guaranteed to successfully complete. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

SNOOZE MODE ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Current during SNOOZE MODE	ZZ ≥ V_{IH}	I_{SB2Z}		5	mA	
ZZ HIGH to SNOOZE MODE time		^tZZ	2(^tKC)		ns	1
SNOOZE MODE Operation recovery time		^tRZZ		2(^tKC)	ns	1

NOTE: 1. This parameter is sampled.

SNOOZE MODE WAVEFORM



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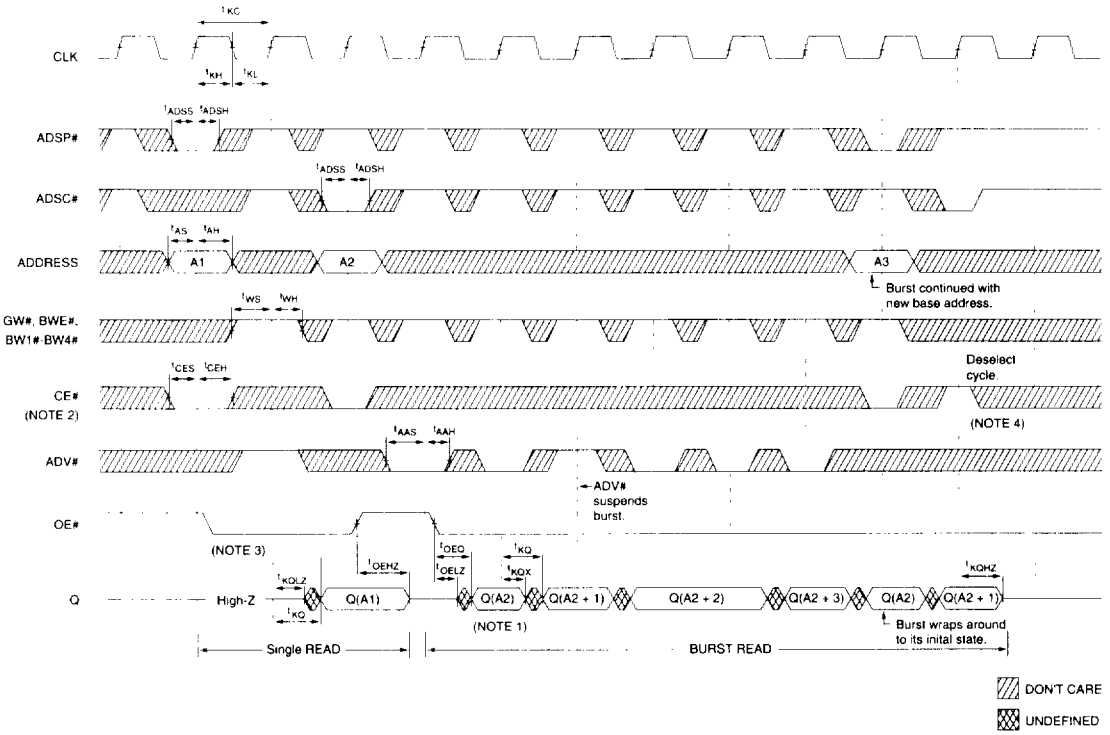
READ TIMING



NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence. OE# does not cause Q to be driven until after the following clock rising edge.
4. Outputs are disabled within one clock cycle after deselect.

READ TIMING PARAMETERS

	-4.5		-5		-5.5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tKC	8		8.5		10		11.1		20		ns
tKH	2.5		2.5		3.2		3.8		6		ns
tKL	2.5		2.5		3.2		3.8		6		ns
tKQ		4.5		5		5.5		6		8	ns
tKQX	1.5		2		2		2		2		ns
tKQLZ	1.5		2		2		2		2		ns
tKQHZ	2	4.5	2	5	2	5.5	2	6	2	6	ns
tOEQ		4.5		4.8		5.5		6		6	ns
tOELZ	0		0		0		0		0		ns
tOEHZ		4.5		4.8		5.5		6		6	ns

	-4.5		-5		-5.5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAS	2.0		2.0		2.0		2.5		3.0		ns
tADSS	2.0		2.0		2.0		2.5		3.0		ns
tAAS	2.0		2.0		2.0		2.5		3.0		ns
tWS	2.0		2.0		2.0		2.5		3.0		ns
tCES	2.0		2.0		2.0		2.5		3.0		ns
tAH	0.5		0.5		0.5		0.5		0.5		ns
tADSH	0.5		0.5		0.5		0.5		0.5		ns
tAAH	0.5		0.5		0.5		0.5		0.5		ns
tWH	0.5		0.5		0.5		0.5		0.5		ns
tCEH	0.5		0.5		0.5		0.5		0.5		ns

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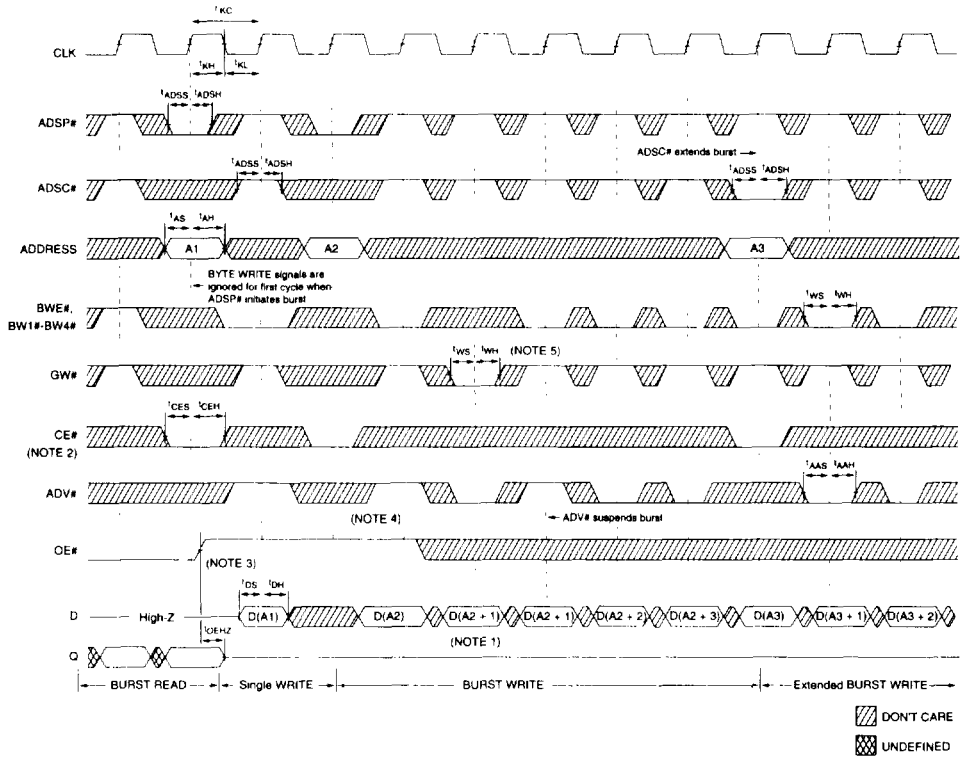
WRITE TIMING



NOTE:
1. D(A2) refers to input for address A2. D(A2+1) refers to input for the next internal burst address following A2.
2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
3. OE# must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. ADV# must be HIGH to permit a WRITE to the loaded address.
5. Full width WRITE can be initiated by GW# LOW or GW# HIGH and BWE#, WEL# and WEH# LOW.

WRITE TIMING PARAMETERS

	-4.5		-5		-5.5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tKC	8		8.5		10		11.1		20		ns
tKH	2.5		2.5		3.2		3.8		6		ns
tKL	2.5		2.5		3.2		3.8		6		ns
tOEHZ		4.5		4.8		5.5		6		6	ns
tAS	2.0		2.0		2.0		2.5		3.0		ns
tADSS	2.0		2.0		2.0		2.5		3.0		ns
tAAS	2.0		2.0		2.0		2.5		3.0		ns
tWS	2.0		2.0		2.0		2.5		3.0		ns

	-4.5		-5		-5.5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tDS	2.0		2.0		2.0		2.5		3.0		ns
tCES	2.0		2.0		2.0		2.5		3.0		ns
tAH	0.5		0.5		0.5		0.5		0.5		ns
tADSH	0.5		0.5		0.5		0.5		0.5		ns
tAAH	0.5		0.5		0.5		0.5		0.5		ns
tWH	0.5		0.5		0.5		0.5		0.5		ns
tDH	0.5		0.5		0.5		0.5		0.5		ns
tCEH	0.5		0.5		0.5		0.5		0.5		ns

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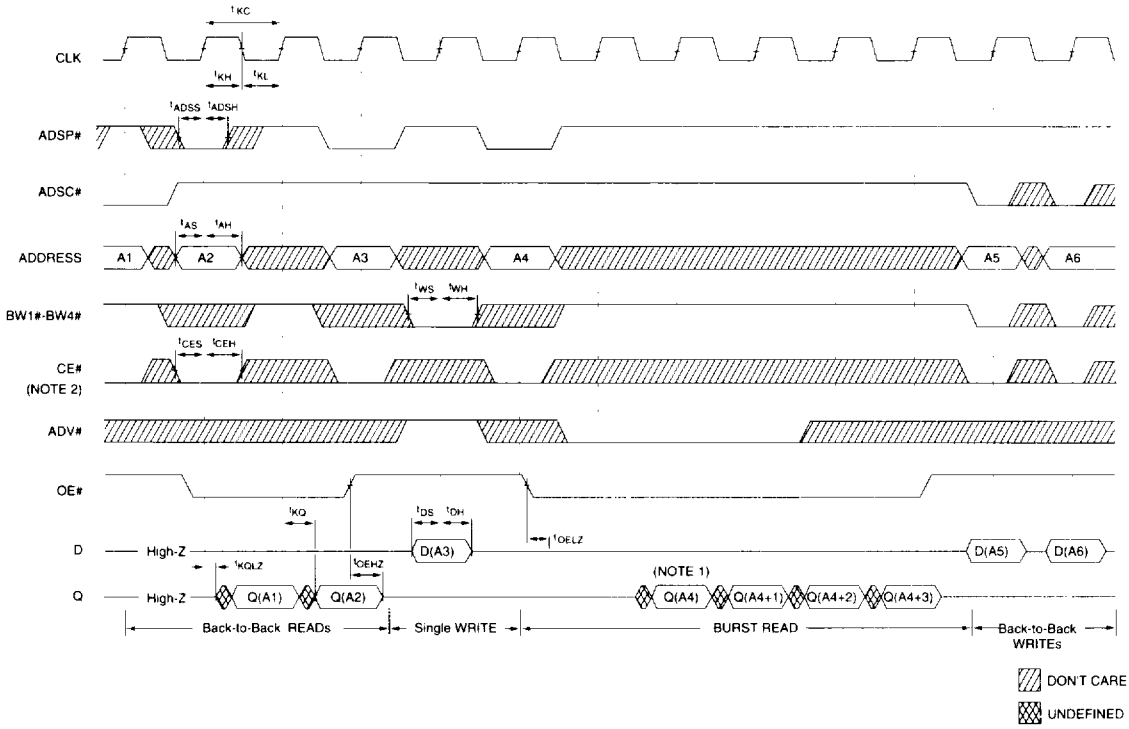
READ/WRITE TIMING



NOTE:
1. Q(A4) refers to output from address A4. Q(A4+1) refers to output from the next internal burst address following A4.
2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
3. The data bus (Q) remains in High-Z following a WRITE cycle unless an ADSP#, ADSC# or ADV# cycle is performed.
4. GW# is HIGH.
5. Back-to-back READs may be controlled by either ADSP# or ADSC#.

READ/WRITE TIMING PARAMETERS

	-4.5		-5		-5.5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tKC	8		8.5		10		11.1		20		ns
tKH	2.5		2.5		3.2		3.8		6		ns
tKL	2.5		2.5		3.2		3.8		6		ns
tKQ		4.5		5		5.5		6		8	ns
tKQLZ	1.5		2		2		2		2		ns
tOELZ	0		0		0		0		0		ns
tOEHZ		4.5		4.8		5.5		6		6	ns
tAS	2.0		2.0		2.0		2.5		3.0		ns
tADSS	2.0		2.0		2.0		2.5		3.0		ns

	-4.5		-5		-5.5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tWS	2.0		2.0		2.0		2.5		3.0		ns
tDS	2.0		2.0		2.0		2.5		3.0		ns
tCES	2.0		2.0		2.0		2.5		3.0		ns
tAH	0.5		0.5		0.5		0.5		0.5		ns
tADSH	0.5		0.5		0.5		0.5		0.5		ns
tWH	0.5		0.5		0.5		0.5		0.5		ns
tDH	0.5		0.5		0.5		0.5		0.5		ns
tCEH	0.5		0.5		0.5		0.5		0.5		ns

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