



576Mb CIO Reduced Latency (RLDRAM[®] II)

MT49H16M36
MT49H32M18
MT49H64M9

For the latest data sheet, refer to Micron's Web site: www.micron.com/rldram

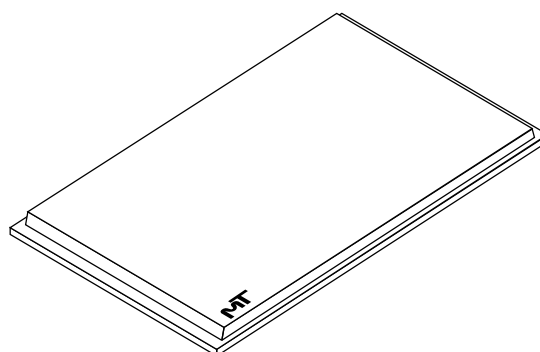
Features

- 533 MHz DDR operation (1,067 Mb/s/pin data rate)
- Organization
16 Meg x 36, 32 Meg x 18, and 64 Meg x 9
8 banks
- Cyclic bank switching for maximum bandwidth
- Reduced cycle time (15ns at 533 MHz)
- Nonmultiplexed addresses (address multiplexing option available)
- SRAM-type interface
- Programmable READ latency (RL), row cycle time, and burst sequence length
- Balanced READ and WRITE latencies in order to optimize data bus utilization
- Data mask for WRITE commands
- Differential input clocks (CK, CK#)
- Differential input data clocks (DKx, DKx#)
- On-chip DLL generates CK edge-aligned data and output data clock signals
- Data valid signal (QVLD)
- 32ms refresh (16K refresh for each bank; 64K refresh command must be issued in total each 32ms)
- 144-ball μ BGA package
- HSTL I/O (1.5V or 1.8V nominal)
- 25 Ω –60 Ω matched impedance outputs
- 2.5V V_{EXT}, 1.8V V_{DD}, 1.5V or 1.8V V_{DDQ} I/O
- On-die termination (ODT) RTT

Table 1: Valid Part Numbers

Part Number	Description
MT49H16M36FM-xx	16 Meg x 36 RLDRAM II
MT49H32M18FM-xx	32 Meg x 18 RLDRAM II
MT49H64M9FM-xx	64 Meg x 9 RLDRAM II

Figure 1: 144-Ball μ BGA



Options

- Clock cycle timing
1.875ns @ ^tRC = 15
2.5ns @ ^tRC = 15
2.5ns @ ^tRC = 17.5
2.5ns @ ^tRC = 20
3.3ns @ ^tRC = 16.7
3.3ns @ ^tRC = 20
- Configuration
16 Meg x 36
32 Meg x 18
64 Meg x 9
- Operating temperature range
Commercial
0° to +95°C
Industrial
T_C = -40°C to +95°C
T_A = -40°C to +85°C
- Package
144-ball μ BGA
(11mm x 18.5mm, lead-free)

Marking

-18
-25E
-25Z
-25
-33E
-33

MT49H16M36
MT49H32M18
MT49H64M9

None
IT

FM
BM¹

Notes: 1. Contact Micron for availability of lead-free products.



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General Description

The Micron[®] 576Mb reduced latency DRAM (RLDRAM[®]) II is a high-speed memory device designed for high bandwidth communication data storage—telecommunications, networking, and cache applications, etc. The chip's 8-bank architecture is optimized for high speed and achieves a peak bandwidth of 38.4 Gb/s, using a 36-bit interface and a maximum system clock of 533 MHz.

The double data rate (DDR) interface transfers two 36-, 18-, or 9-bit wide data word per clock cycle at the I/O pins. Output data is referenced to the free-running output data clock.

Commands, addresses, and control signals are registered at every positive edge of the differential input clock, while input data is registered at both positive and negative edges of the input data clock(s).

Read and write accesses to the RLD_{RAM} are burst-oriented. The burst length is programmable from 2, 4, or 8 by setting the mode register.

The device is supplied with 2.5V and 1.8V for the core and 1.5V or 1.8V for the output drivers.

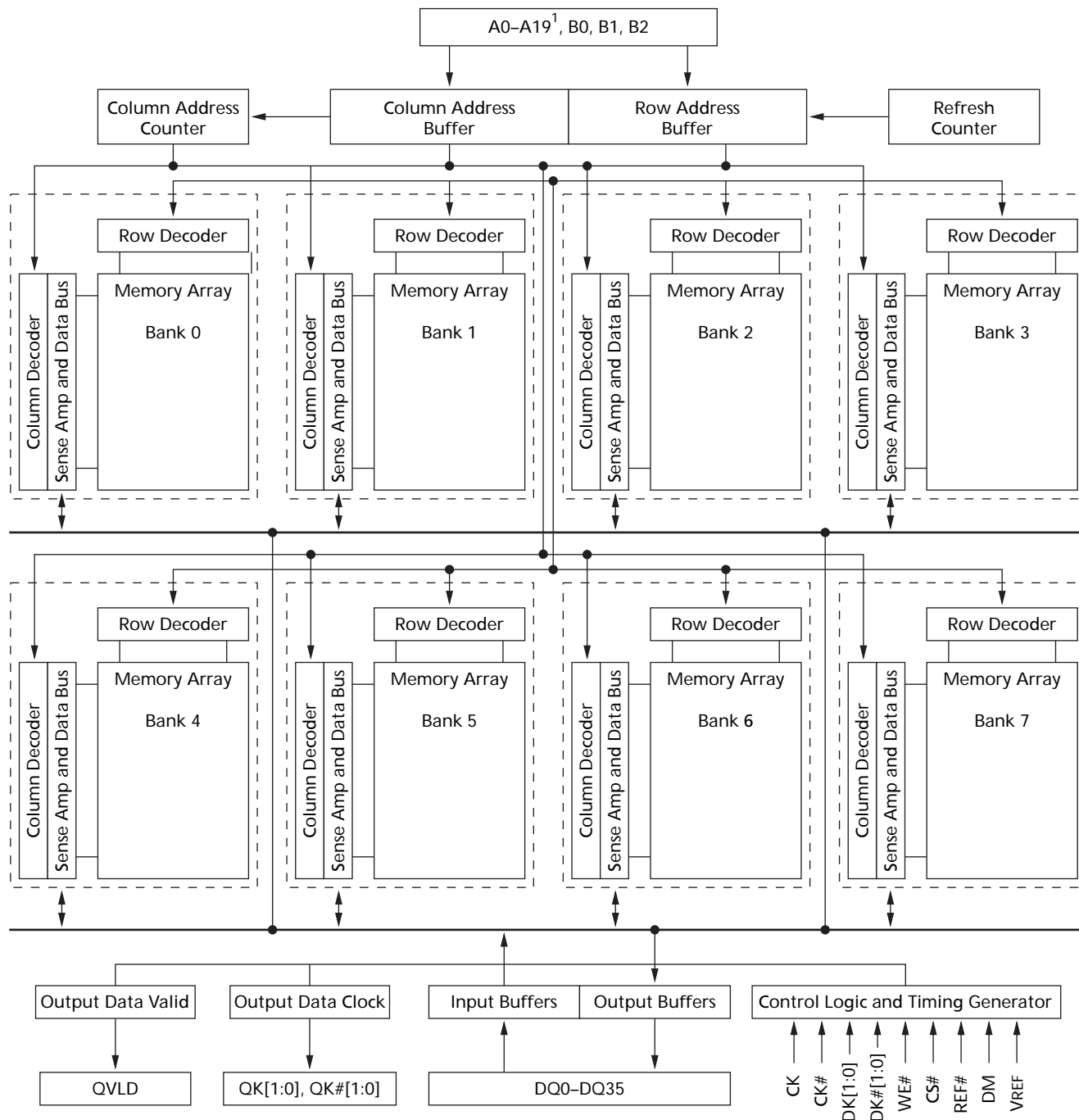
Bank-scheduled refresh is supported with row address generated internally.

A standard μ BGA 144-ball package is used to enable ultra high-speed data transfer rates and a simple upgrade path from former products.



Functional Block Diagram

Figure 2: 16 Meg x 36



Notes: 1. When the BL = 4 setting is used, A19 is a "Don't Care." When the BL = 8 setting is used, both A18 and A19 become "Don't Care."



576Mb: x36, x18, x9 2.5V V_{EXT}, 1.8V V_{DD}, HSTL, RLDRAM II Ball Assignment and Description

Ball Assignment and Description

Table 2: 16 Meg x 36 Ball Assignment (Top View) 144-Ball μ BGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	VSS	VEXT	VSS					VSS	VEXT	TMS	TCK
B	VDD	DQ8	DQ9	VSSQ					VSSQ	DQ1	DQ0	VDD
C	VTT	DQ10	DQ11	VDDQ					VDDQ	DQ3	DQ2	VTT
D	(A22) ¹	DQ12	DQ13	VSSQ					VSSQ	QK0#	QK0	VSS
E	(A21) ²	DQ14	DQ15	VDDQ					VDDQ	DQ5	DQ4	(A20) ²
F	A5	DQ16	DQ17	VSSQ					VSSQ	DQ7	DQ6	QVLD
G	A8	A6	A7	VDD					VDD	A2	A1	A0
H	B2	A9	VSS	VSS					VSS	VSSL	A4	A3
J	DK0	DK0#	VDD	VDD					VDD	VDDL	B0	CK
K	DK1	DK1#	VDD	VDD					VDD	VDD	B1	CK#
L	REF#	CS#	VSS	VSS					VSS	VSS	A14	A13
M	WE#	A16	A17	VDD					VDD	A12	A11	A10
N	A18	DQ24	DQ25	VSSQ					VSSQ	DQ35	DQ34	A19
P	A15	DQ22	DQ23	VDDQ					VDDQ	DQ33	DQ32	DM
R	VSS	QK1	QK1#	VSSQ					VSSQ	DQ31	DQ30	VSS
T	VTT	DQ20	DQ21	VDDQ					VDDQ	DQ29	DQ28	VTT
U	VDD	DQ18	DQ19	VSSQ					VSSQ	DQ27	DQ26	VDD
V	VREF	ZQ	VEXT	VSS					VSS	VEXT	TDO	TDI

- Notes: 1. Reserved for future use. This may optionally be connected to GND.
 2. Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to GND.



576Mb: x36, x18, x9 2.5V V_{EXT}, 1.8V V_{DD}, HSTL, RLDRAM II Ball Assignment and Description

Table 3: 32 Meg x 18 Ball Assignment (Top View) 144-Ball μ BGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	VSS	VEXT	VSS					VSS	VEXT	TMS	TCK
B	VDD	DNU ⁴	DQ4	VSSQ					VSSQ	DQ0	DNU ⁴	VDD
C	VTT	DNU ⁴	DQ5	VDDQ					VDDQ	DQ1	DNU ⁴	VTT
D	(A22) ¹	DNU ⁴	DQ6	VSSQ					VSSQ	QK0#	QK0	VSS
E	(A21) ²	DNU ⁴	DQ7	VDDQ					VDDQ	DQ2	DNU ⁴	A20
F	A5	DNU ⁴	DQ8	VSSQ					VSSQ	DQ3	DNU ⁴	QVLD
G	A8	A6	A7	VDD					VDD	A2	A1	A0
H	B2	A9	VSS	VSS					VSS	VSSL	A4	A3
J	NF ³	NF ³	VDD	VDD					VDD	VDDL	B0	CK
K	DK	DK#	VDD	VDD					VDD	VDD	B1	CK#
L	REF#	CS#	VSS	VSS					VSS	VSS	A14	A13
M	WE#	A16	A17	VDD					VDD	A12	A11	A10
N	A18	DNU ⁴	DQ14	VSSQ					VSSQ	DQ9	DNU ⁴	A19
P	A15	DNU ⁴	DQ15	VDDQ					VDDQ	DQ10	DNU ⁴	DM
R	VSS	QK1	QK1#	VSSQ					VSSQ	DQ11	DNU ⁴	VSS
T	VTT	DNU ⁴	DQ16	VDDQ					VDDQ	DQ12	DNU ⁴	VTT
U	VDD	DNU ⁴	DQ17	VSSQ					VSSQ	DQ13	DNU ⁴	VDD
V	VREF	ZQ	VEXT	VSS					VSS	VEXT	TDO	TDI

- Notes:
1. Reserved for future use. This may optionally be connected to GND.
 2. Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to GND.
 3. No function. This signal is internally connected and has parasitic characteristics of a clock input signal.
 4. Do not use. This signal is internally connected and has parasitic characteristics of an I/O. This may optionally be connected to GND.



576Mb: x36, x18, x9 2.5V V_{EXT}, 1.8V V_{DD}, HSTL, RLD_{RAM} II Ball Assignment and Description

Table 4: 64 Meg x 9 Ball Assignment (Top View) 144-Ball μ BGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	VSS	VEXT	VSS					VSS	VEXT	TMS	TCK
B	VDD	DNU ³	DNU ³	VSSQ					VSSQ	DQ0	DNU ³	VDD
C	VTT	DNU ³	DNU ³	VDDQ					VDDQ	DQ1	DNU ³	VTT
D	(A22) ¹	DNU ³	DNU ³	VSSQ					VSSQ	QK0#	QK0	VSS
E	A21	DNU ³	DNU ³	VDDQ					VDDQ	DQ2	DNU ³	A20
F	A5	DNU ³	DNU ³	VSSQ					VSSQ	DQ3	DNU ³	QVLD
G	A8	A6	A7	VDD					VDD	A2	A1	A0
H	B2	A9	VSS	VSS					VSS	VSSL	A4	A3
J	NF ²	NF ²	VDD	VDD					VDD	VDDL	B0	CK
K	DK	DK#	VDD	VDD					VDD	VDD	B1	CK#
L	REF#	CS#	VSS	VSS					VSS	VSS	A14	A13
M	WE#	A16	A17	VDD					VDD	A12	A11	A10
N	A18	DNU ³	DNU ³	VSSQ					VSSQ	DQ4	DNU ³	A19
P	A15	DNU ³	DNU ³	VDDQ					VDDQ	DQ5	DNU ³	DM
R	VSS	DNU ³	DNU ³	VSSQ					VSSQ	DQ6	DNU ³	VSS
T	VTT	DNU ³	DNU ³	VDDQ					VDDQ	DQ7	DNU ³	VTT
U	VDD	DNU ³	DNU ³	VSSQ					VSSQ	DQ8	DNU ³	VDD
V	VREF	ZQ	VEXT	VSS					VSS	VEXT	TDO	TDI

- Notes:
1. Reserved for future use. This signal is not connected.
 2. No function. This signal is internally connected and has parasitic characteristics of a clock input signal.
 3. Do not use. This signal is internally connected and has parasitic characteristics of an I/O. This may optionally be connected to GND.



576Mb: x36, x18, x9 2.5V V_{EXT}, 1.8V V_{DD}, HSTL, RLDRAM II Ball Assignment and Description

Table 5: Ball Descriptions

Symbol	Type	Description
CK, CK#	Input	Input clock: CK and CK# are differential clock inputs. Addresses and commands are latched on the rising edge of CK. CK# is ideally 180 degrees out of phase with CK.
CS#	Input	Chip select: CS# enables the command decoder when LOW and disables it when HIGH. When the command decoder is disabled, new commands are ignored, but internal operations continue.
WE#, REF#	Input	Command inputs: Sampled at the positive edge of CK, WE#, and REF# define (together with CS#) the command to be executed.
A[0:21]	Input	Address inputs: A[0:21] define the row and column addresses for READ and WRITE operations. During a MODE REGISTER SET, the address inputs define the register settings. They are sampled at the rising edge of CK. In the x36 configuration, A[21:20] are reserved for address expansion; in the x18 configuration, A[21] is reserved for address expansion. These expansion addresses can be treated as address inputs, but they do not affect the operation of the device.
A22	–	Reserved for future use. This signal is not connected and may be connected to ground.
BA[0:2]	Input	Bank address inputs: Select to which internal bank a command is being applied.
DQ0–DQ35	Input/Output	Data input/output: The DQ signals form the 36-bit data bus. During READ commands, the data is referenced to both edges of QK. During WRITE commands, the data is sampled at both edges of DKx.
QKx, QKx#	Output	Output data clocks: QKx and QKx# are opposite polarity, output data clocks. During READs, they are free running and edge-aligned with data output from the RLDRAM. QKx# is ideally 180 degrees out of phase with QKx. For the x36 device, QK0 and QK0# are aligned with DQ0–DQ17. QK1 and QK1# are aligned with DQ18–DQ35. For the x18 device, QK0 and QK0# are aligned with DQ0–DQ8. QK1 and QK1# are aligned with DQ9–DQ17. Consult the RLDRAM II design guide for more details.
DKx, DKx#	Input	Input data clock: DKx and DKx# are the differential input data clocks. All input data is referenced to both edges of DKx. DKx# is ideally 180 degrees out of phase with DKx. For the x36 device, DQ0–DQ17 are referenced to DK0 and DK0#, and DQ18–DQ35 are referenced to DK1 and DK1#. For the x9 and x18 devices, all DQs are referenced to DK and DK#.
DM	Input	Input data mask: The DM signal is the input mask signal for WRITE data. Input data is masked when DM is sampled HIGH, along with the WRITE input data. DM is sampled on both edges of DK (DK1 for the x36 configuration).
QVLD	Output	Data valid: The QVLD indicates valid output data. QVLD is edge-aligned with QKx and QKx#.
TMS TDI	Input	IEEE 1149.1 test inputs: These balls may be left no connects if the JTAG function is not used in the circuit.
TCK	Input	IEEE 1149.1 clock input: This ball must be tied to V _{ss} if the JTAG function is not used in the circuit.
TDO	Output	IEEE 1149.1 test output: JTAG output.
ZQ	Input/Output	External impedance [25–60Ω]: This signal is used to tune the device outputs to the system data bus impedance. DQ output impedance is set to $0.2 \times RQ$, where RQ is a resistor from this signal to ground. Connecting ZQ to GND invokes the minimum impedance mode. Connecting ZQ to V _{DD} invokes the maximum impedance mode. Refer to Figure 8 on page 19 to activate this function.
VREF	Input	Input reference voltage: Nominally V _{DDQ} /2. Provides a reference voltage for the input buffers.
VEXT	Supply	Power supply: 2.5V nominal. See Table 23 on page 45 for range.
VDD	Supply	Power supply: 1.8V nominal. See Table 23 on page 45 for range.
VDDQ	Supply	DQ power supply: Nominally, 1.5V or 1.8V. Isolated on the device for improved noise immunity. See Table 23 on page 45 for range.


Table 5: Ball Descriptions (continued)

Symbol	Type	Description
VDDL	Supply	DLL power supply: Nominally, 1.8V. Isolated on the device for improved noise immunity. See Table 23 on page 45 for range.
Vss	Supply	Ground.
VssQ	Supply	DQ ground: Isolated on the device for improved noise immunity.
VssL	Supply	DLL ground: Isolated on the device for improved noise immunity.
VTT	Supply	Power supply: Isolated termination supply. Nominally, V _{DDQ} /2. See Table 23 on page 45 for range.
NF	–	No function: These balls may be connected to ground.
DNU	–	Do not use: These balls may be connected to ground.

Commands

According to the functional signal description, the following command sequences are possible. All input states or sequences not shown are illegal or reserved. All command and address inputs must meet setup and hold times around the rising edge of CK.

Table 6: Address Widths at Different Burst Lengths

Burst Length	Configuration		
	x36	x18	x9
BL = 2	19:0	20:0	21:0
BL = 4	18:0	19:0	20:0
BL = 8	17:0	18:0	19:0

Table 7: Command Table

Note 1

Operation	Code	CS#	WE#	REF#	A[21:0]	B[2:0]	Notes
Device Deselect/NO OPERATION	DESEL/NOP	H	X	X	X	X	
MRS: MODE REGISTER SET	MRS	L	L	L	OPCODE	X	2
READ	READ	L	H	H	A	BA	3
WRITE	WRITE	L	L	H	A	BA	3
AUTO REFRESH	AREF	L	H	L	X	BA	

- Notes: 1. X = "Don't Care"
 H = logic HIGH
 L = logic LOW
 A = valid address
 BA = valid bank address
 2. Only A(17:0) are used for the MRS command.
 3. See Table 6.


Table 8: Description of Commands

Command	Description
DESEL/NOP ¹	The NOP command is used to perform a no operation to the RLDRAM, which essentially deselects the chip. Use the NOP command to prevent unwanted commands from being registered during idle or wait states. Operations already in progress are not affected. Output values depend on command history.
MRS	The mode register is set via the address inputs A(17:0). See Figure 8 on page 19 for further information. The MRS command can only be issued when all banks are idle and no bursts are in progress.
READ	The READ command is used to initiate a burst read access to a bank. The value on the BA(2:0) inputs selects the bank, and the address provided on inputs A(21:0) selects the data location within the bank.
WRITE	The WRITE command is used to initiate a burst write access to a bank. The value on the BA(2:0) inputs selects the bank, and the address provided on inputs A(21:0) selects the data location within the bank. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If the DM signal is registered LOW, the corresponding data will be written to memory. If the DM signal is registered HIGH, the corresponding data inputs will be ignored (i.e., this part of the data word will not be written).
AREF	The AREF is used during normal operation of the RLDRAM to refresh the memory content of a bank. The command is nonpersistent, so it must be issued each time a refresh is required. The value on the BA(2:0) inputs selects the bank. The refresh address is generated by an internal refresh controller, effectively making each address bit a "Don't Care" during the AREF command. The RLDRAM requires 128K cycles at an average periodic interval of $0.24\mu\text{s}^2$ (MAX). To improve efficiency, eight AREF commands (one for each bank) can be posted to the RLDRAM at periodic intervals of $1.95\mu\text{s}^3$.

- Notes:
1. When the chip is deselected, internal NOP commands are generated and no commands are accepted.
 2. Actual refresh is $32\text{ms}/16\text{K}/8 = 0.244\mu\text{s}$.
 3. Actual refresh is $32\text{ms}/16\text{K} = 1.95\mu\text{s}$.


Table 9: AC Electrical Characteristics (-13E/-25E/-25Z)
Note 1

Description	Symbol	-18E		-25E		-25Z		Units	Notes
		Min	Max	Min	Max	Min	Max		
Clock									
Clock cycle time	t_{CK}, t_{DK}	1.875	5.7	2.5	5.7	2.5	5.7	ns	
System frequency	f_{CK}, f_{DK}	175	533	175	400	175	400	MHz	
Random cycle time	t_{RC}	15		15		17.5		ns	
Clock jitter - period	t_{JITPER}	-100	100	-150	150	-150	150	ps	2
Clock jitter - cycle to cycle	t_{JITCC}		200		300		300	ps	
Clock HIGH time	t_{CKH}, t_{DKH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Clock LOW time	t_{CKL}, t_{DKL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Clock to input data clock	t_{CKDK}	-0.3	0.3	-0.5	0.5	-0.5	0.5	ns	
Mode register set cycle time to any command	t_{MRSC}	6		6		6		t_{CK}	
Setup Times									
Address/command and input setup time	t_{AS}/t_{CS}	0.3		0.4		0.4		ns	
Data-in and data mask to DK setup time	t_{DS}	0.17		0.25		0.25		ns	
Hold Times									
Address/command and input hold time	t_{AH}/t_{CH}	0.3		0.4		0.4		ns	
Data-in and data mask to DK hold time	t_{DH}	0.17		0.25		0.25		ns	
Data and Data Strobe									
Output data clock HIGH time	t_{QKH}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CKH}	
Output data clock LOW time	t_{QKL}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CKL}	
QK edge to clock edge skew	t_{CKQK}	-0.2	0.2	-0.25	0.25	-0.25	0.25	ns	
QK edge to output data edge	$t_{QKQ0},$ t_{QKQ1}	-0.12	0.12	-0.2	0.2	-0.2	0.2	ns	3
QK edge to any output data edge	t_{QKQ}	-0.22	0.22	-0.3	0.3	-0.3	0.3	ns	4
QK edge to QVLD	t_{QKVLD}	-0.22	0.22	-0.3	0.3	-0.3	0.3	ns	

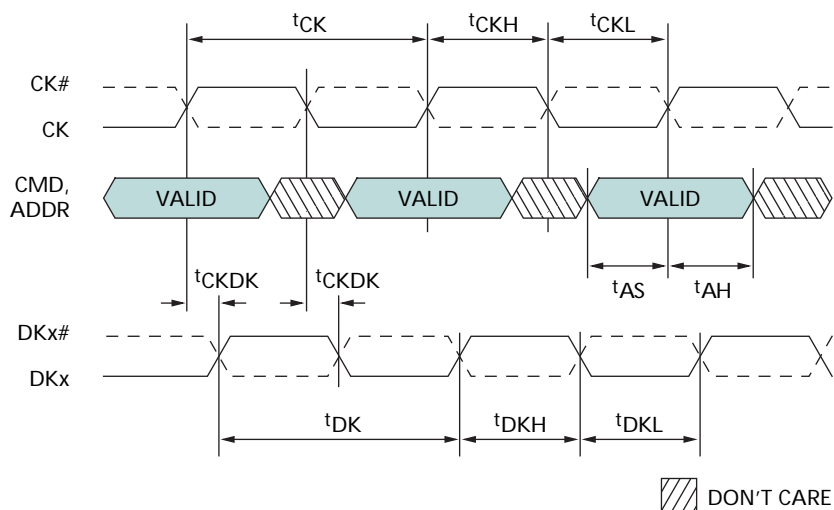
- Notes: 1. All timing parameters are measured relative to the crossing point of CK/CK#, DK/DK# and to the crossing point with V_{REF} of the command, address, and data signals.
2. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
3. t_{QKQ0} is referenced to Q0–Q17 in x36 and Q0–Q8 in x18.
 t_{QKQ1} is referenced to Q18–Q35 in x36 and Q9–Q17 in x18.
4. t_{QKQ} takes into account the skew between any QKx and any Q.


Table 10: AC Electrical Characteristics (-25/-33Z/-33)

Note 1

Description	Symbol	-25		-33Z		-33		Units	Notes
		Min	Max	Min	Max	Min	Max		
Clock									
Clock cycle time	t_{CK}, t_{DK}	2.5	5.7	3.3	5.7	3.3	5.7	ns	
System frequency	f_{CK}, f_{DK}	175	400	175	300	175	300	MHz	
Random cycle time	t_{RC}	20		16.7		20		ns	
Clock jitter - period	t_{JITPER}	-150	150	-200	200	-200	200	ps	2
Clock jitter - cycle to cycle	t_{JITCC}		200		400		400	ps	
Clock HIGH time	t_{CKH}, t_{DKH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Clock LOW time	t_{CKL}, t_{DKL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Clock to input data clock	t_{CKDK}	-0.3	1.0	-0.3	1.5	-0.3	1.5	ns	
Mode register set cycle time to any command	t_{MRSC}	6		6		6		t_{CK}	
Setup Times									
Address/command and input setup time	t_{AS}/t_{CS}	0.4		0.5		0.5		ns	
Data-in and data mask to DK setup time	t_{DS}	0.25		0.3		0.3		ns	
Hold Times									
Address/command and input hold time	t_{AH}/t_{CH}	0.4		0.5		0.5		ns	
Data-in and data mask to DK hold time	t_{DH}	0.25		0.3		0.3		ns	
Data and Data Strobe									
Output data clock HIGH time	t_{QKH}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CKH}	
Output data clock LOW time	t_{QKL}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CKL}	
QK edge to clock edge skew	t_{CKQK}	-0.25	0.25	-0.3	0.3	-0.3	0.3	ns	
QK edge to output data edge	$t_{QKQ0},$ t_{QKQ1}	-0.2	0.2	-0.25	0.25	-0.25	0.25	ns	3
QK edge to any output data edge	t_{QKQ}	-0.3	0.3	-0.35	0.35	-0.35	0.35	ns	4
QK edge to QVLD	t_{QKVLD}	-0.3	0.3	-0.35	0.35	-0.35	0.35	ns	

- Notes:
1. All timing parameters are measured relative to the crossing point of CK/CK#, DK/DK# and to the crossing point with V_{REF} of the command, address, and data signals.
 2. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
 3. t_{QKQ0} is referenced to Q0–Q17 in x36 and Q0–Q8 in x18.
 t_{QKQ1} is referenced to Q18–Q35 in x36 and Q9–Q17 in x18.
 4. t_{QKQ} takes into account the skew between any QKx and any Q.

Figure 3: Clock/Input Data Clock Command/Address Timings


Initialization

The RLDRAM must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operations or permanent damage to the device.

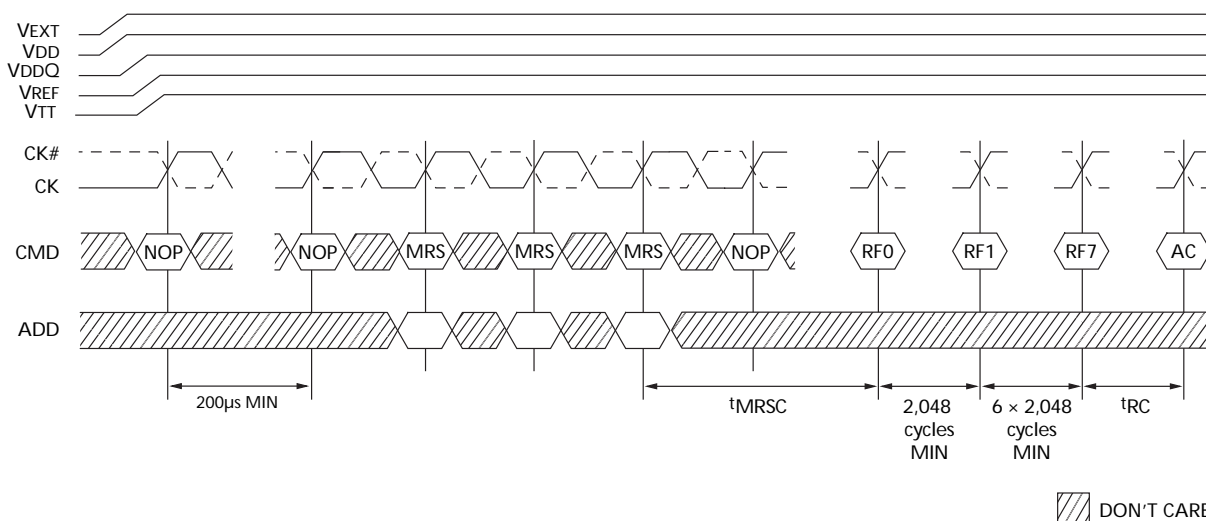
The following sequence is used for power-up:

1. Apply power (V_{EXT}, V_{DD}, V_{DDQ}, V_{REF}, V_T). If CK/CK# cannot be static and meet VID(DC) prior to the supply voltages being stable, CS# must be HIGH. Apply V_{DD} and V_{EXT} before or at the same time as V_{DDQ}. Apply V_{DDQ} before or at the same time as V_{REF} and V_T. Although there is no timing relation between V_{EXT} and V_{DD}, the chip starts the power-up sequence only after both voltages are at their nominal levels. Maintain all remaining balls in NOP conditions.
2. Maintain stable conditions for 200µs (MIN).
3. Issue three back-to-back and clock consecutive MRS commands: two dummies plus one valid MRS. It is recommended that the address lines during the dummy MRS commands are the same value as they are during the valid MRS.
4. ^tMRSC after the valid MRS, issue eight AUTO REFRESH commands, one on each bank and separated by 2,048 cycles. Initial bank refresh order does not matter.
5. After ^tRC, the chip is ready for normal operation.



576Mb: x36, x18, x9 2.5V V_{EXT}, 1.8V V_{DD}, HSTL, RLDRAM II Programmable Impedance Output Buffer

Figure 4: Power-Up Sequence



Notes: 1. RFx: REFRESH Bank x
AC: Any command

Programmable Impedance Output Buffer

The RLDRAM II is equipped with programmable impedance output buffers. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (R_Q) is connected between the Z_Q ball and V_{SS}. The value of the resistor must be five times the desired impedance. For example, a 300Ω resistor is required for an output impedance of 60Ω. To ensure that output impedance is one fifth the value of R_Q (within 15 percent), the range of R_Q is 125Ω to 300Ω.

Output impedance updates may be required because, over time, variations may occur in supply voltage and temperature. The device samples the value of R_Q. An impedance update is transparent to the system and does not affect device operation. All data sheet timing and current specifications are met during an update.

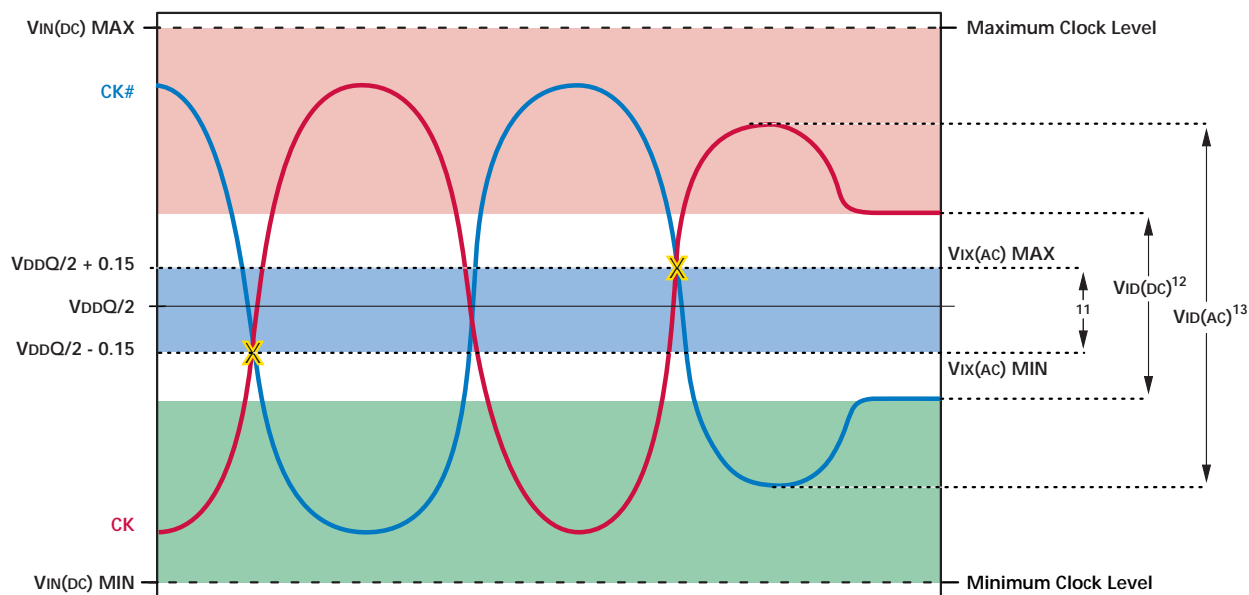
Clock Considerations

The RLDRAM II utilizes internal delay-locked loops for maximum output, data valid windows. It can be placed into a stopped-clock state to minimize power with a modest restart time of 1,024 cycles.

Table 11: Clock Input Operating Conditions

Notes 1–8

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock input voltage level; CK and CK#	V _{IN} (DC)	-0.3	V _{DDQ} + 0.3	V	
Clock input differential voltage; CK and CK#	V _{ID} (DC)	0.2	V _{DDQ} + 0.6	V	9
Clock input differential voltage; CK and CK#	V _{ID} (AC)	0.4	V _{DDQ} + 0.6	V	9
Clock input crossing point voltage; CK and CK#	V _{IX} (AC)	V _{DDQ} /2 - 0.15	V _{DDQ} /2 + 0.15	V	10

Figure 5: Clock Input


- Notes:
1. DKx and DKx# have the same requirements as CK and CK#.
 2. All voltages referenced to V_{SS}.
 3. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operations are tested for the full voltage range specified.
 4. Outputs (except for I_{DD} measurements) measured with equivalent load.
 5. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are tested for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 2 V/ns in the range between V_{IL}(AC) and V_{IH}(AC).
 6. The AC and DC input level specifications are as defined in the HSTL Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
 7. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross. The input reference level for signals other than CK/CK# is V_{REF}.
 8. CK and CK# input slew rate must be ≥ 2 V/ns (≥ 4 V/ns if measured differentially).
 9. VID is the magnitude of the difference between the input level on CK and the input level on CK#.
 10. The value of V_{Ix} is expected to equal V_{DDQ}/2 of the transmitting device and must track variations in the DC level of the same.
 11. CK and CK# must cross within this region.
 12. CK and CK# must meet at least VID(DC) MIN when static and centered around V_{DDQ}/2.
 13. Minimum peak-to-peak swing.



Mode Register Set Command (MRS)

The mode register stores the data for controlling the operating modes of the memory. It programs the RLDRAM configuration, burst length, test mode, and I/O options. During a MRS command, the address inputs A(17:0) are sampled and stored in the mode register. ^tMRSC must be met before any command can be issued to the RLDRAM. The mode register may be set at any time during device operation. However, any pending operations are not guaranteed to successfully complete. See the RLDRAM II design guide for more details.

Figure 6: Mode Register Set Timing

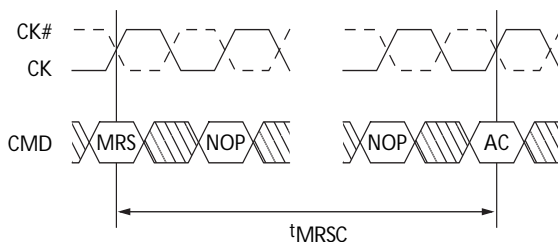
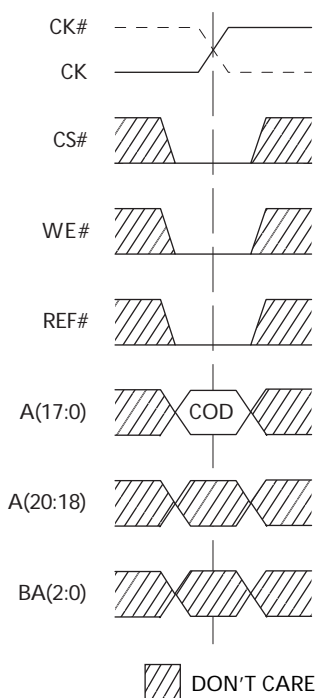


Figure 7: Mode Register Set

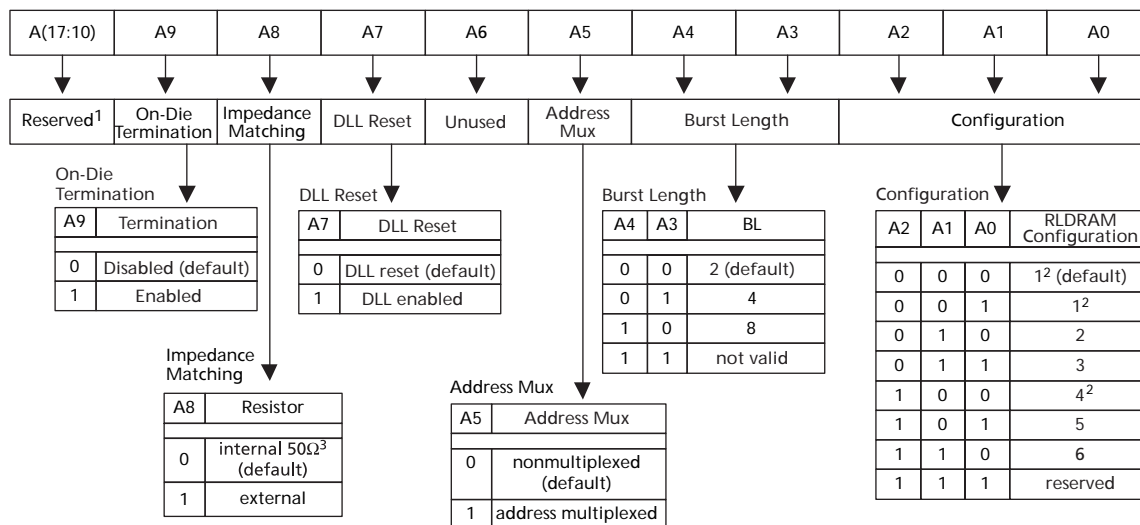


Note: COD: code to be loaded into the register.



576Mb: x36, x18, x9 2.5V V_{EXT}, 1.8V V_{DD}, HSTL, RLDRAM II Configuration Table

Figure 8: Mode Register Bit Map



- Notes: 1. Bits A(17:10) *must* be set to zero.
 2. BL = 8 is not available for configurations 1 and 4.
 3. ±15% temperature variation.

Configuration Table

Table 12 shows, for different operating frequencies, the different RLDRAM configurations that can be programmed into the mode register. The READ and WRITE latency (^tRL and ^tWL) values along with the row cycle times (^tRC) are shown in clock cycles as well as in nanoseconds. The shaded areas correspond to configurations that are not allowed.

Table 12: RLDRAM Configuration Table (Calculating ^tRC Based Off of Clock Frequency)

Example Clock Frequencies	Symbol	Configuration						Units
		1 ¹	2	3	4 ¹	5	6	
	^t RC	4	6	8	3	5	7	cycles
	^t RL	4	6	8	3	5	7	cycles
	^t WL	5	7	9	4	6	8	cycles
533 MHz	^t RC			15.0				ns
	^t RL			15.0				ns
	^t WL			16.875				ns
400 MHz	^t RC		15.0	20.0			17.5	ns
	^t RL		15.0	20.0			17.5	ns
	^t WL		17.5	22.5			20.0	ns
300 MHz	^t RC		20.0	26.7		16.7	23.3	ns
	^t RL		20.0	26.7		16.7	23.3	ns
	^t WL		23.3	30.0		20.0	26.7	ns
200 MHz	^t RC	20.0	30.0	40.0	15.0	25.0	35.0	ns
	^t RL	20.0	30.0	40.0	15.0	25.0	35.0	ns
	^t WL	25.0	35.0	45.0	20.0	30.0	40.0	ns

- Notes: 1. BL = 8 is not available for configurations 1 and 4.



Write Basic Information

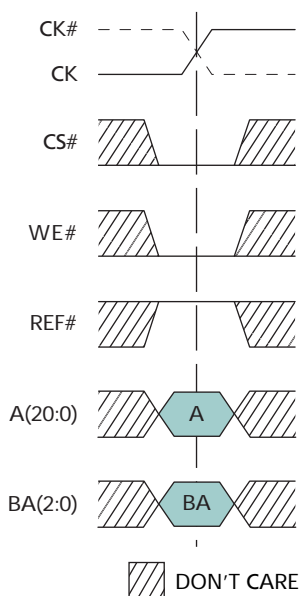
Write accesses are initiated with a WRITE command, as shown in Figure 9. Row and bank addresses are provided together with the WRITE command.

During WRITE commands, data will be registered at both edges of DK according to the programmed burst length (BL). A WRITE latency (WL) one cycle longer than the programmed READ latency (RL + 1) is present, with the first valid data registered at the first rising DK edge WL cycles after the WRITE command.

Any WRITE burst may be followed by a subsequent READ command. Figures 13 and 14 illustrate the timing requirements for a WRITE followed by a READ for bursts of two and four, respectively.

Setup and hold times for incoming DQ relative to the DK edges are specified as t_{DS} and t_{DH} . The input data is masked if the corresponding DM signal is HIGH. The setup and hold times for data mask are also t_{DS} and t_{DH} .

Figure 9: WRITE Command



Note: A: Address; BA: Bank address.



576Mb: x36, x18, x9 2.5V V_{EXT}, 1.8V V_{DD}, HSTL, RLDRAM II
Write Basic Information

Figure 10: Basic WRITE Burst/DM Timing

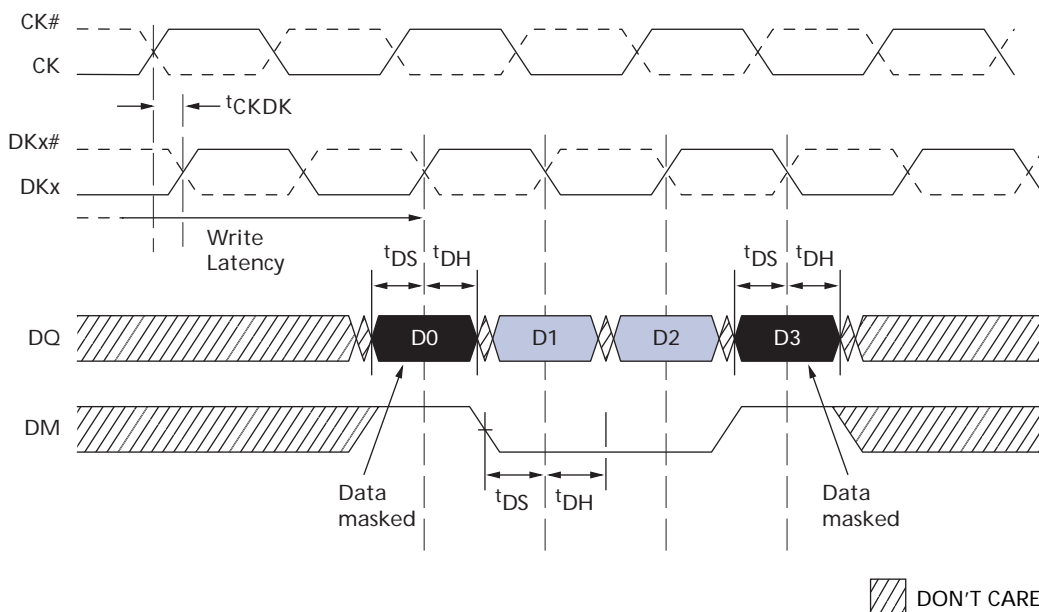
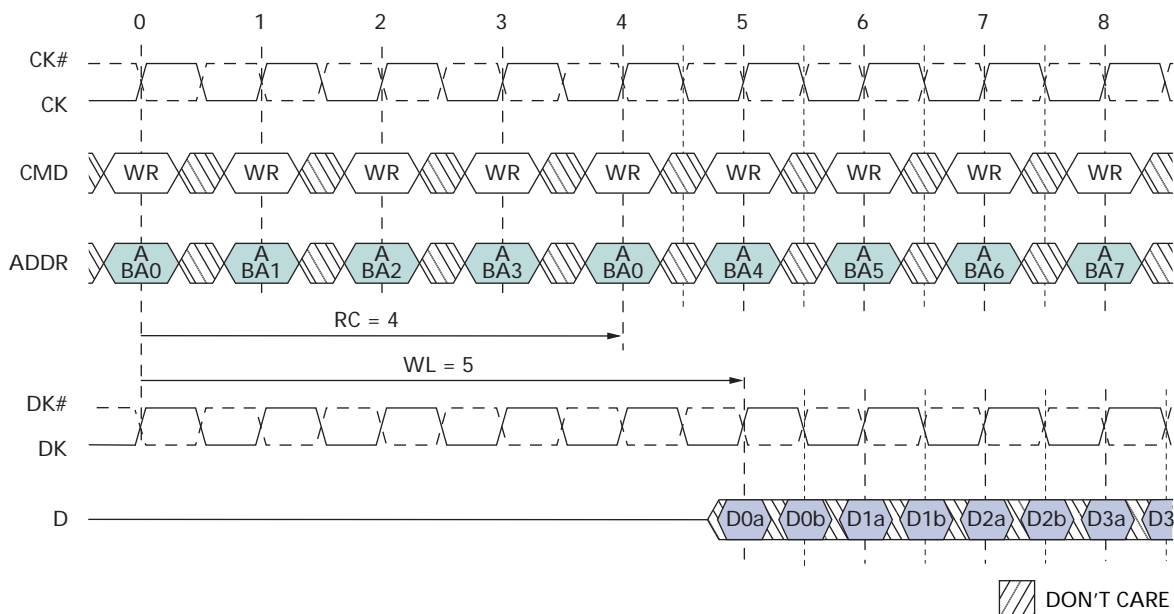


Figure 11: WRITE Burst Basic Sequence: BL = 2, RL = 4, WL = 5, Configuration 1

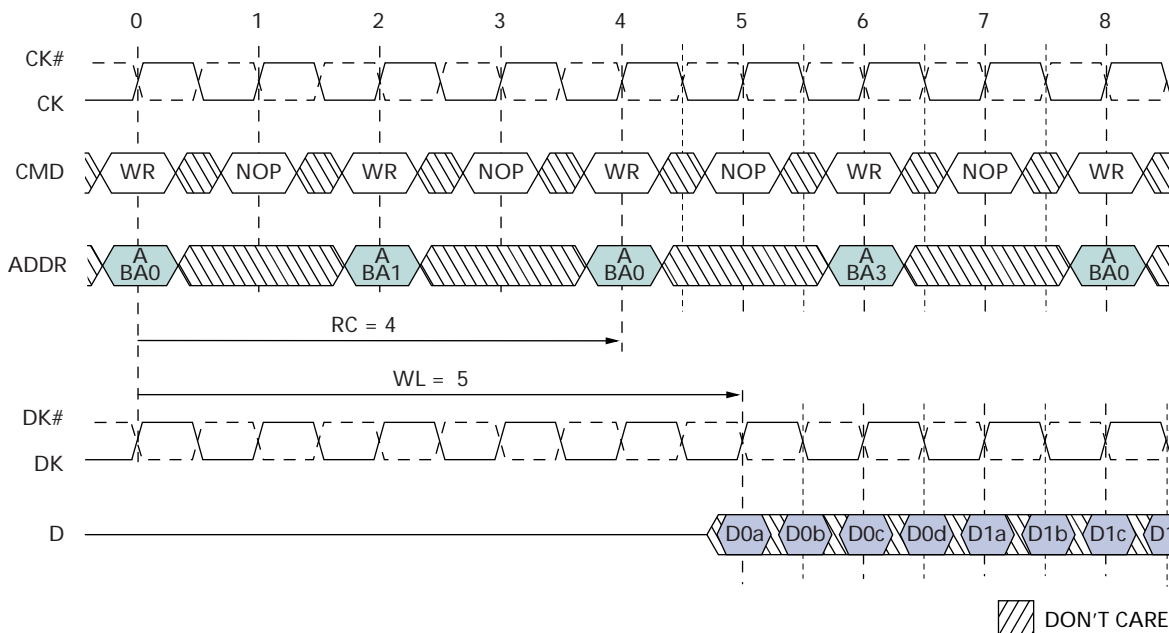


- Notes: 1. A/BAx: Address A of bank x
 WR: WRITE command
 Dxy: Data y to bank x
 RC: Row cycle time



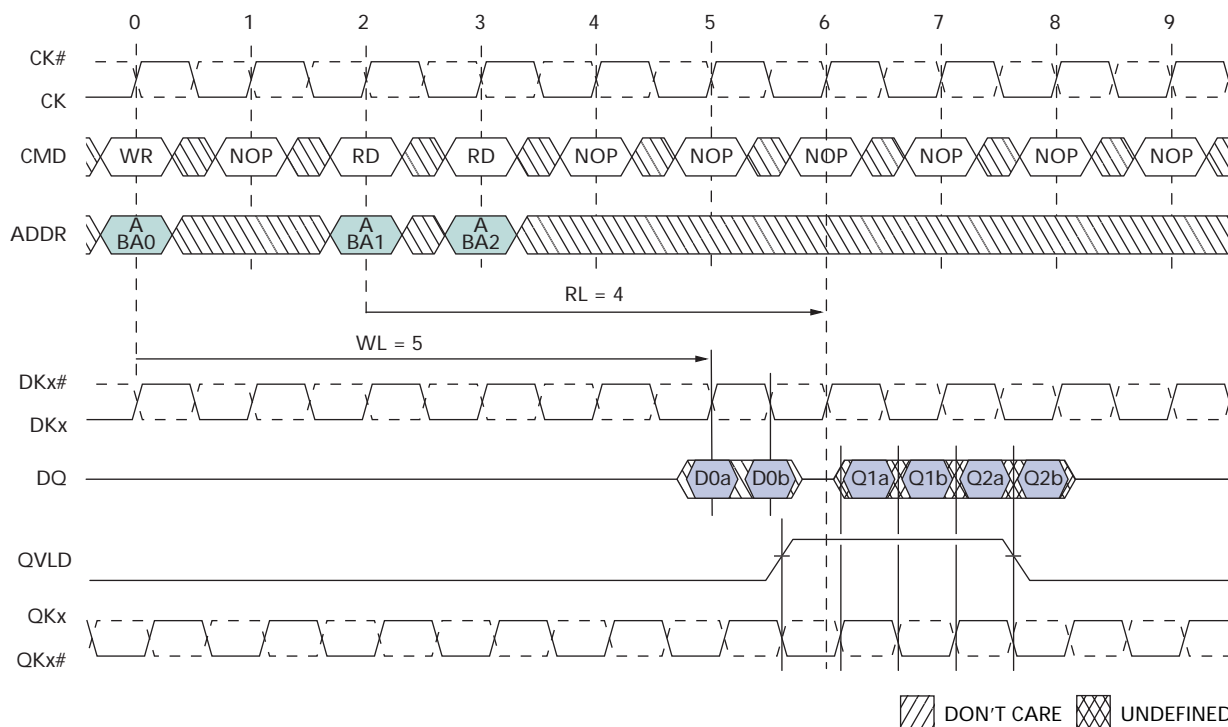
576Mb: x36, x18, x9 2.5V V_{EXT}, 1.8V V_{DD}, HSTL, RLDRAM II
Write Basic Information

Figure 12: WRITE Burst Basic Sequence: BL = 4, RL = 4, WL = 5, Configuration 1



Notes: 1. Any free bank may be used in any given CMD. The sequence shown is only one example of a bank sequence.

Figure 13: WRITE Followed By READ: BL = 2, RL = 4, WL = 5, Configuration 1

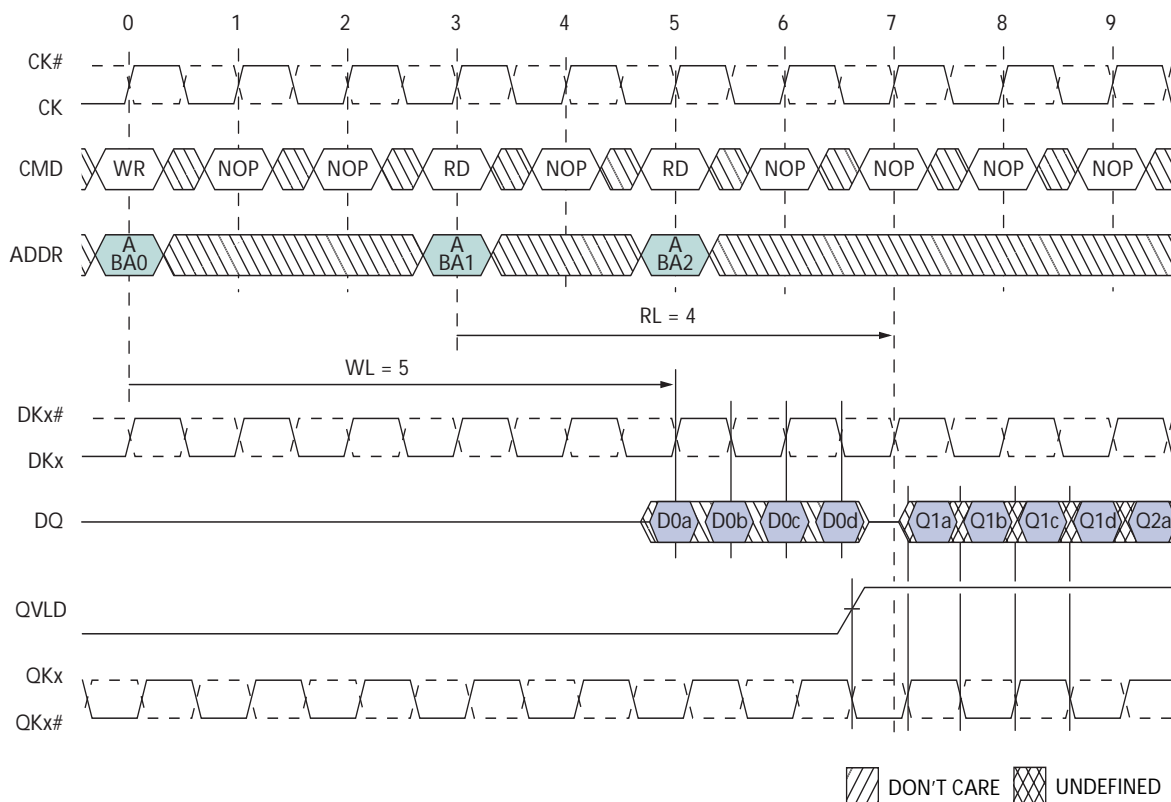


Note: RD: READ
Qxy: Data y from bank x



576Mb: x36, x18, x9 2.5V V_{EXT}, 1.8V V_{DD}, HSTL, RLDRAM II
Write Basic Information

Figure 14: WRITE Followed By READ: BL = 4, RL = 4, WL = 5, Configuration 1





Read Basic Information

Read accesses are initiated with a READ command, as shown in Figure 15. Row and bank addresses are provided with the READ command.

During READ bursts, the memory device drives the read data edge-aligned with the QK signal. After a programmable READ latency, data is available at the outputs. The data valid signal indicates that valid data will be present in the next half clock cycle.

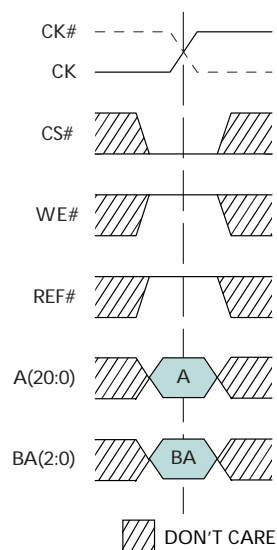
The skew between QK and the crossing point of CK is specified as t_{CKQK} . t_{QKQ0} is the skew between QK0 and the last valid data edge considered over all the data generated at the DQ signals. t_{QKQ1} is the skew between QK1 and the last valid data edge considered over all the data generated at the DQ signals. t_{QKQx} is derived at each QKx clock edge and is not cumulative over time. t_{QKQ} is the maximum of t_{QKQ0} and t_{QKQ1} .

After completion of a burst, assuming no other commands have been initiated, output data (DQ) will go High-Z. Back-to-back READ commands are possible, producing a continuous flow of output data.

The data valid window is derived from each QK transitions and is defined as: $\text{MIN}(t_{QKH}, t_{QKL}) - 2(t_{QKQ} [\text{MAX}])$.

Any READ burst may be followed by a subsequent WRITE command. Figures 19 and 20 illustrate the timing requirements for a READ followed by a WRITE. Depending on the programmed READ latency, a READ-to-WRITE delay occurs in order to prevent bus contention. Some systems having long line lengths or severe skews may need additional idle cycles inserted. Refer to the RLDRAM II design guide for more details.

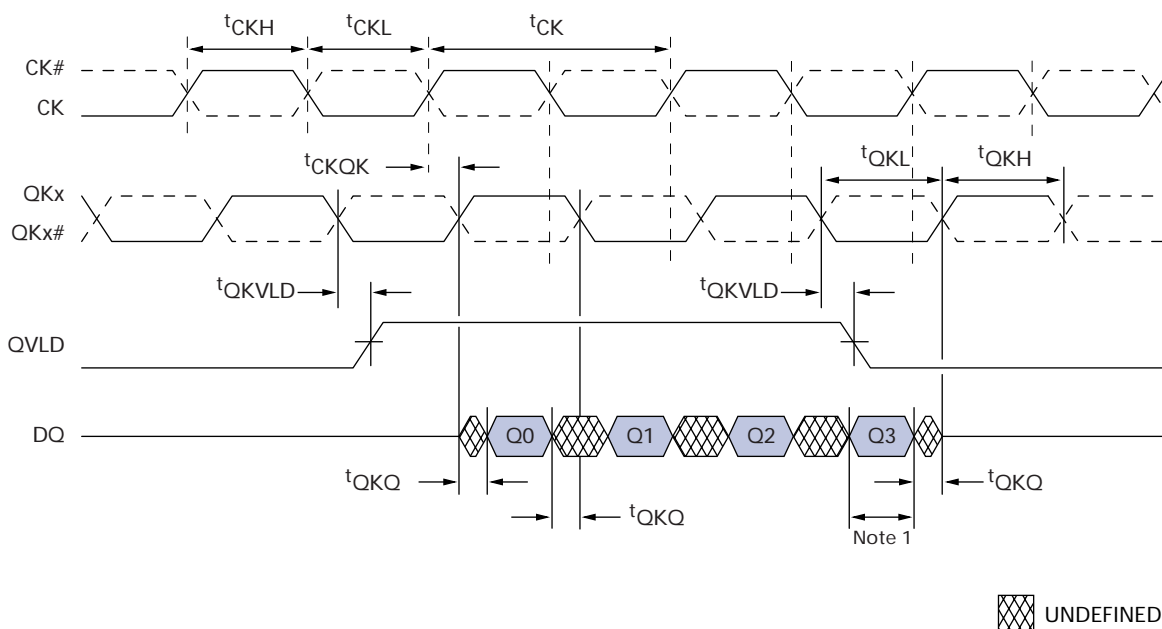
Figure 15: READ Command





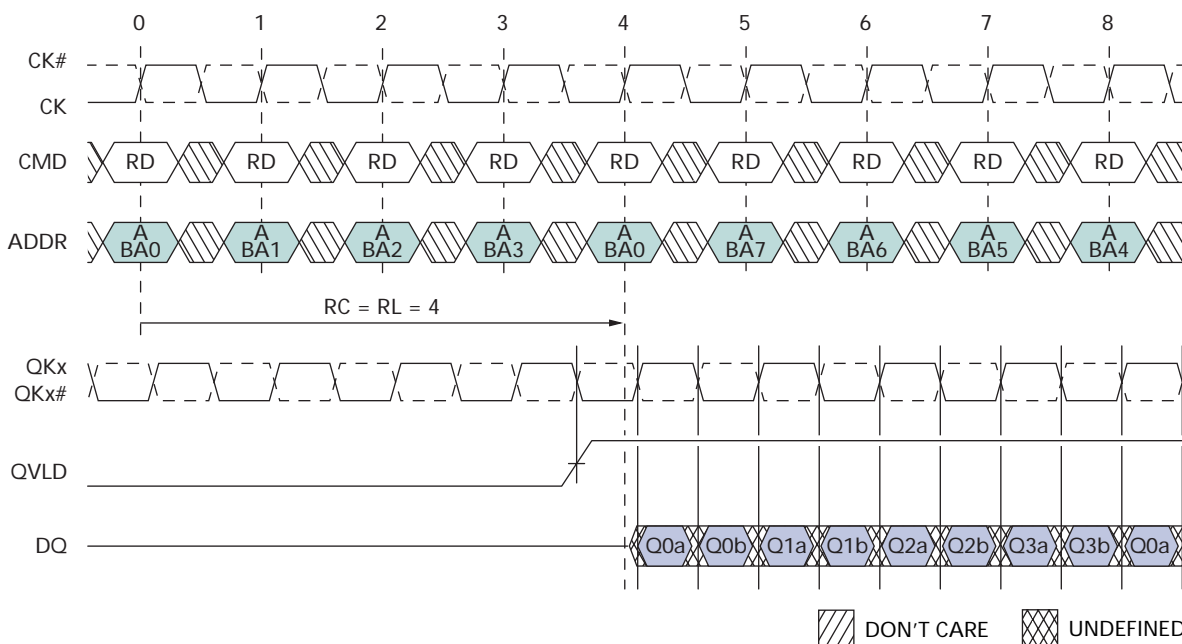
576Mb: x36, x18, x9 2.5V V_{EXT}, 1.8V V_{DD}, HSTL, RLDRAM II
Read Basic Information

Figure 16: Basic READ Burst Timing



- Notes: 1. Minimum data valid window can be expressed as $\text{MIN}(t_{QKH}, t_{QKL}) - 2 \times t_{QKQx} (\text{MAX})$.
 2. t_{QKQ0} is referenced to DQ0–DQ17 in x36 and DQ0–DQ8 in x18.
 t_{QKQ1} is referenced to DQ18–DQ35 in x36 and DQ9–DQ17 in x18.
 3. t_{QKQ} takes into account the skew between any QKx and any DQ.

Figure 17: READ Burst: BL = 2, RL = 4, Configuration 1





576Mb: x36, x18, x9 2.5V V_{EXT}, 1.8V V_{DD}, HSTL, RLDRAM II
Read Basic Information

Figure 18: READ Burst: BL = 4, RL = 4, Configuration 1

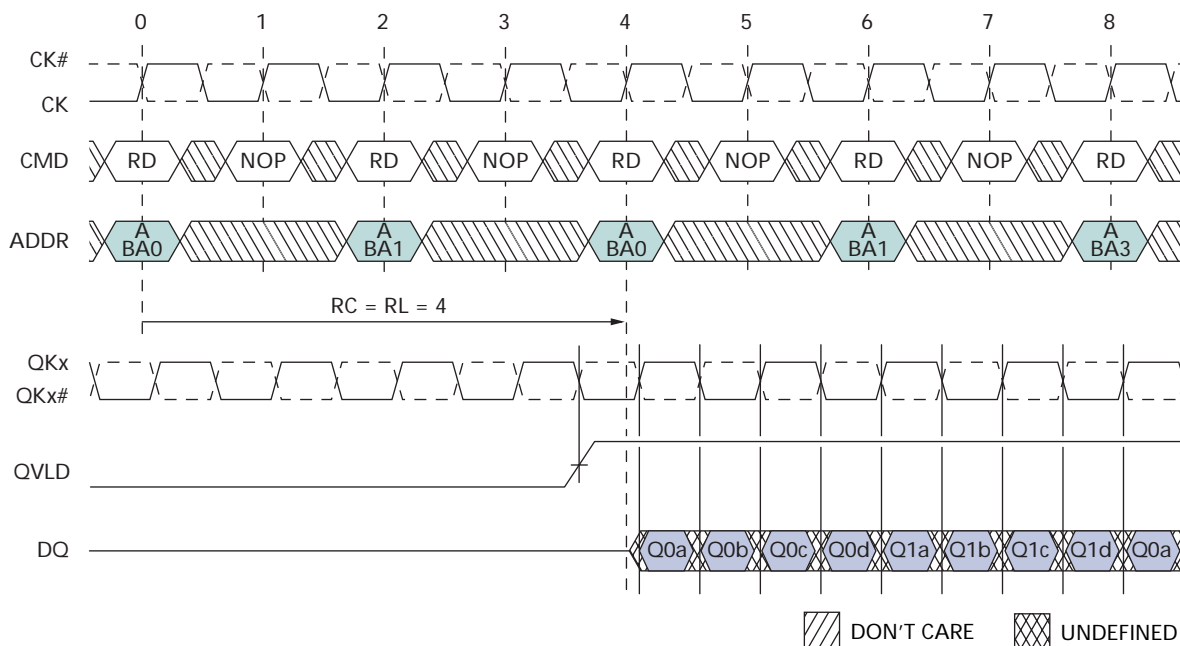
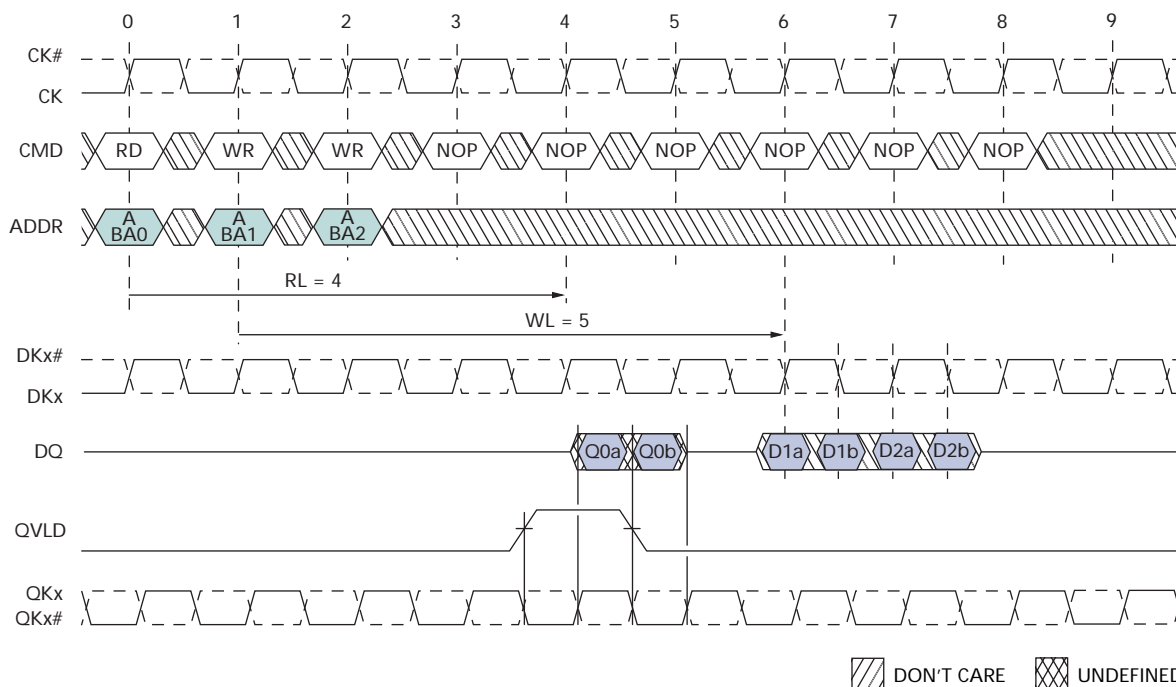


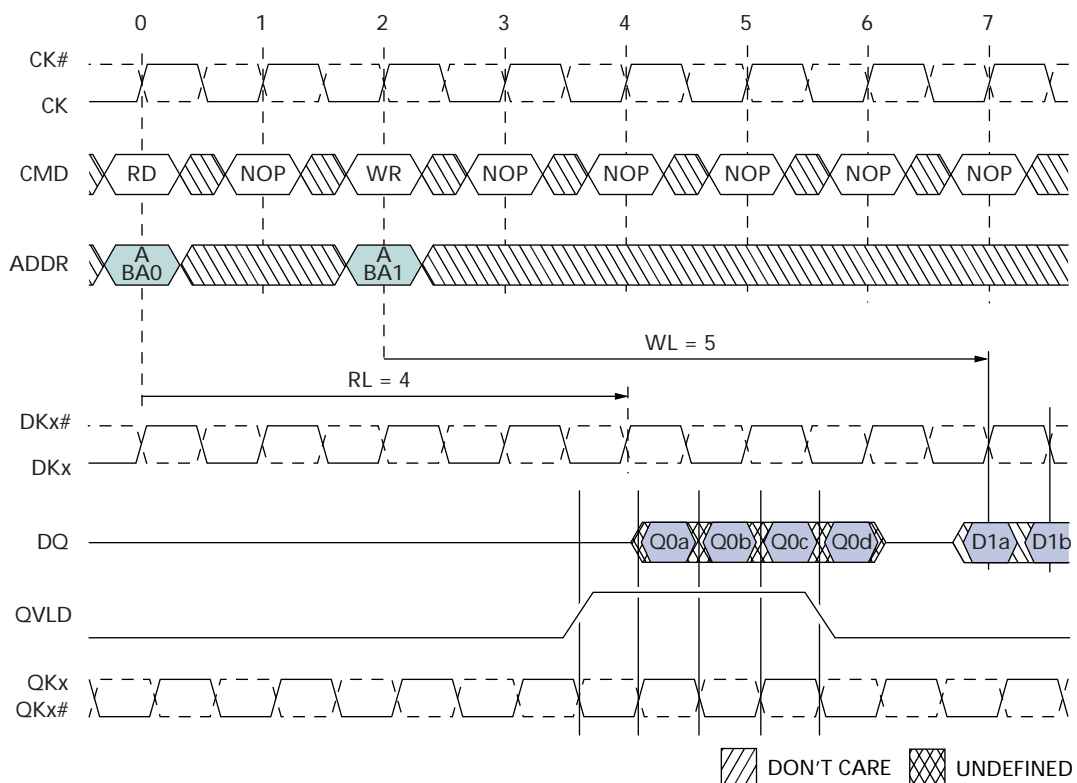
Figure 19: READ followed by WRITE, BL = 2, RL = 4, WL = 5, Configuration 1





576Mb: x36, x18, x9 2.5V V_{EXT}, 1.8V V_{DD}, HSTL, RLDRAM II
Read Basic Information

Figure 20: READ followed by WRITE, BL = 4, RL = 4, WL = 5, Configuration 1





AUTO REFRESH Command (AREF)

AREF is used to perform a REFRESH cycle on one row in a specific bank. The row addresses are generated by an internal refresh counter for each bank; external address balls are “Don’t Care.” The delay between the AREF command and a subsequent command to the same bank must be at least t_{RC} .

Within a period of 32ms (t_{REF}), the entire memory must be refreshed. Figure 22 illustrates an example of a continuous refresh sequence. Other refresh strategies, such as burst refresh, are also possible.

Figure 21: AUTO REFRESH Command

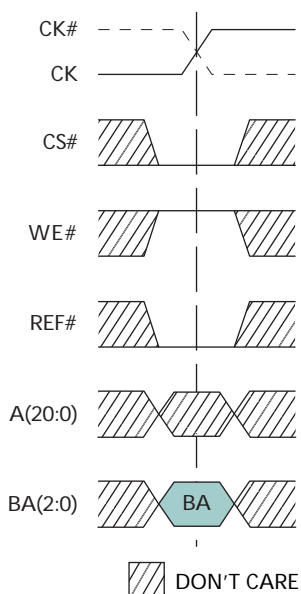
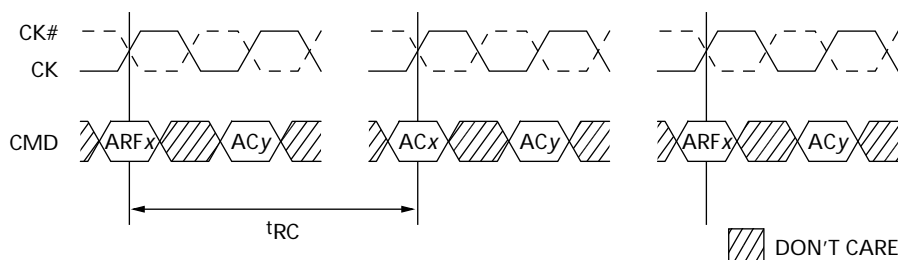


Figure 22: AUTO REFRESH Cycle



- Notes:
1. AC_x: Any command on bank x
 ARF_x: Auto refresh bank x
 AC_y: Any command on different bank
 2. t_{RC} is configuration-dependent. Refer to Table 12 on page 19.



On-Die Termination

On-die termination (ODT) is enabled by setting A9 to “1” during a MRS command. With ODT on, all the DQs and DM are terminated to V_{TT} with a resistance R_{TT}. The command, address, and clock signals are not terminated. Figure 23 below shows the equivalent circuit of a DQ receiver with ODT. ODTs are dynamically switched off during READ commands and are designed to be off prior to the RLD RAM driving the bus. Similarly, ODTs are designed to switch on after the RLD RAM has issued the last piece of data.

Table 13: On-Die Termination DC Parameters

Description	Symbol	Min	Max	Units	Notes
Termination voltage	V _{TT}	0.95 × V _{REF}	1.05 × V _{REF}	V	1, 2
On-Die termination	R _{TT}	135	165	Ω	3

- Notes: 1. All voltages referenced to V_{SS} (GND).
 2. V_{TT} is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
 3. The R_{TT} value is measured at +70°C T_C.

Figure 23: On-Die Termination-Equivalent Circuit

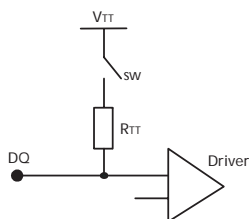
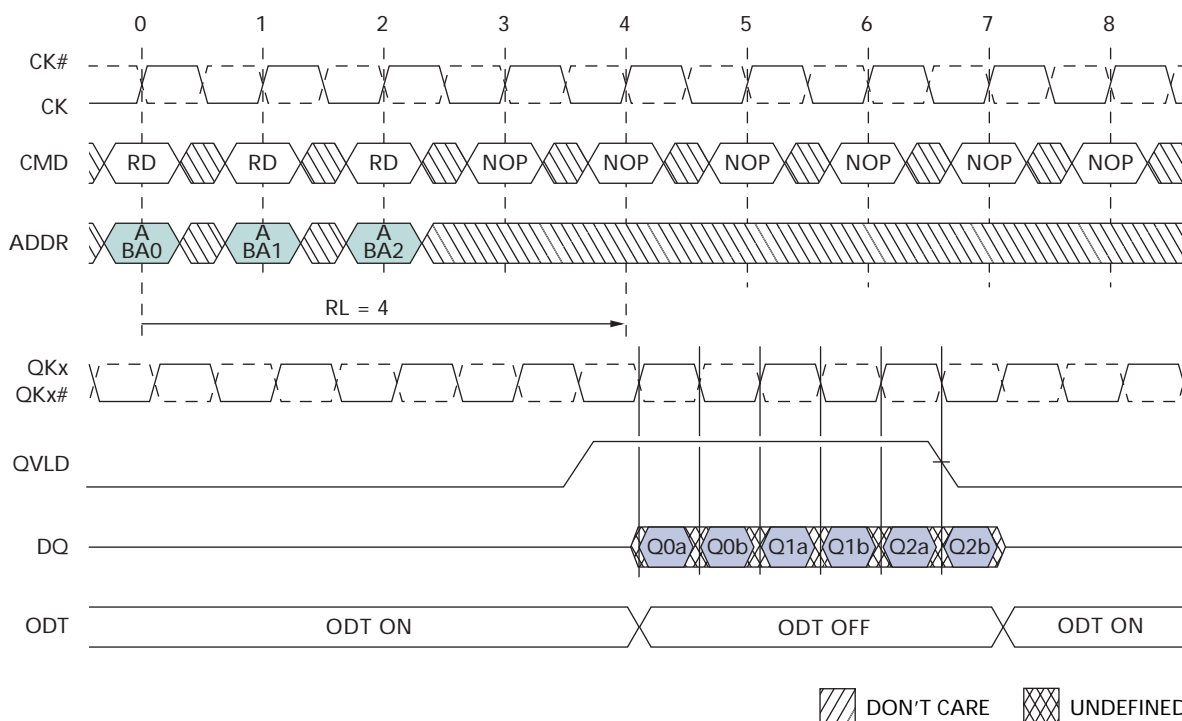


Figure 24: READ Burst with ODT: BL = 2, Configuration 1



▨ DON'T CARE ▩ UNDEFINED



Figure 25: READ NOP READ with ODT: BL = 2, Configuration 1

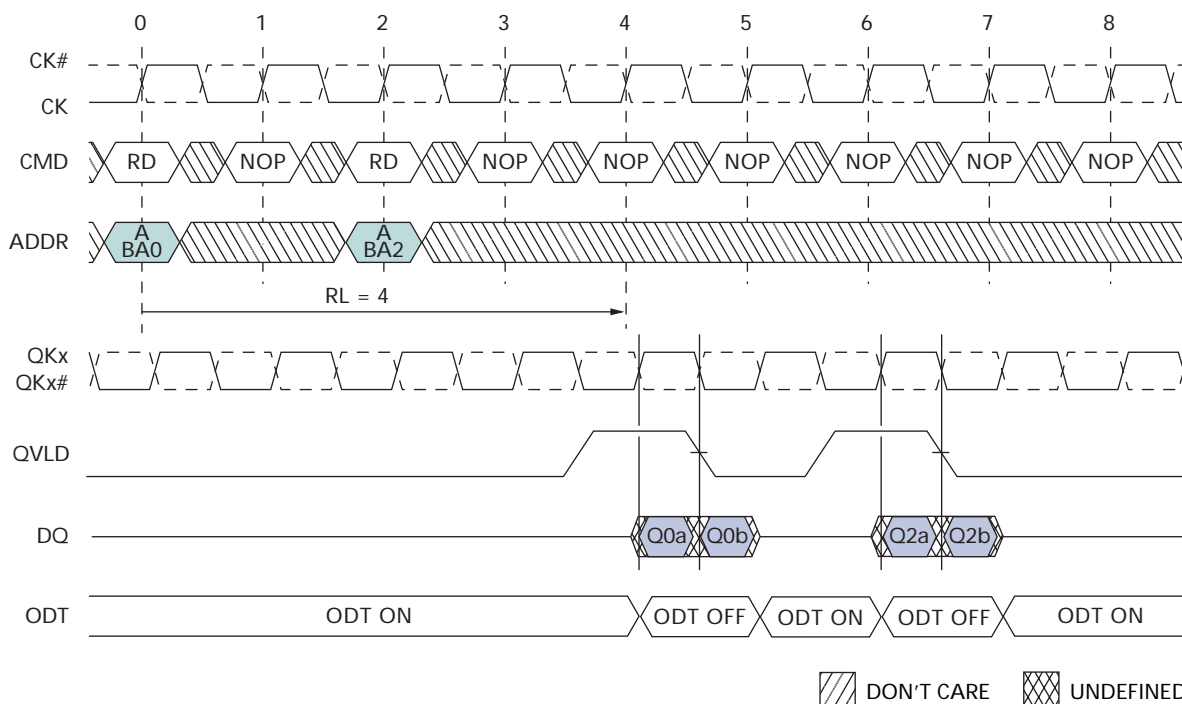


Figure 26: READ NOP NOP READ with ODT: BL = 2, Configuration 1

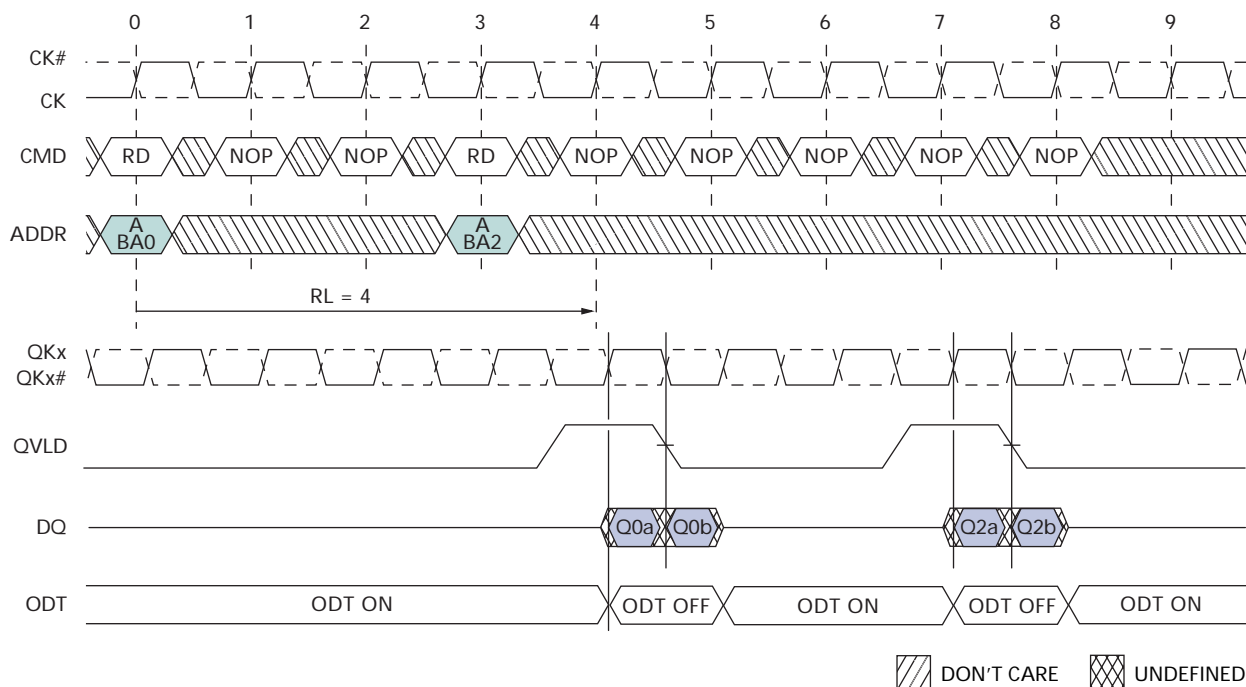




Figure 27: READ followed by WRITE with ODT: BL = 2, Configuration 1

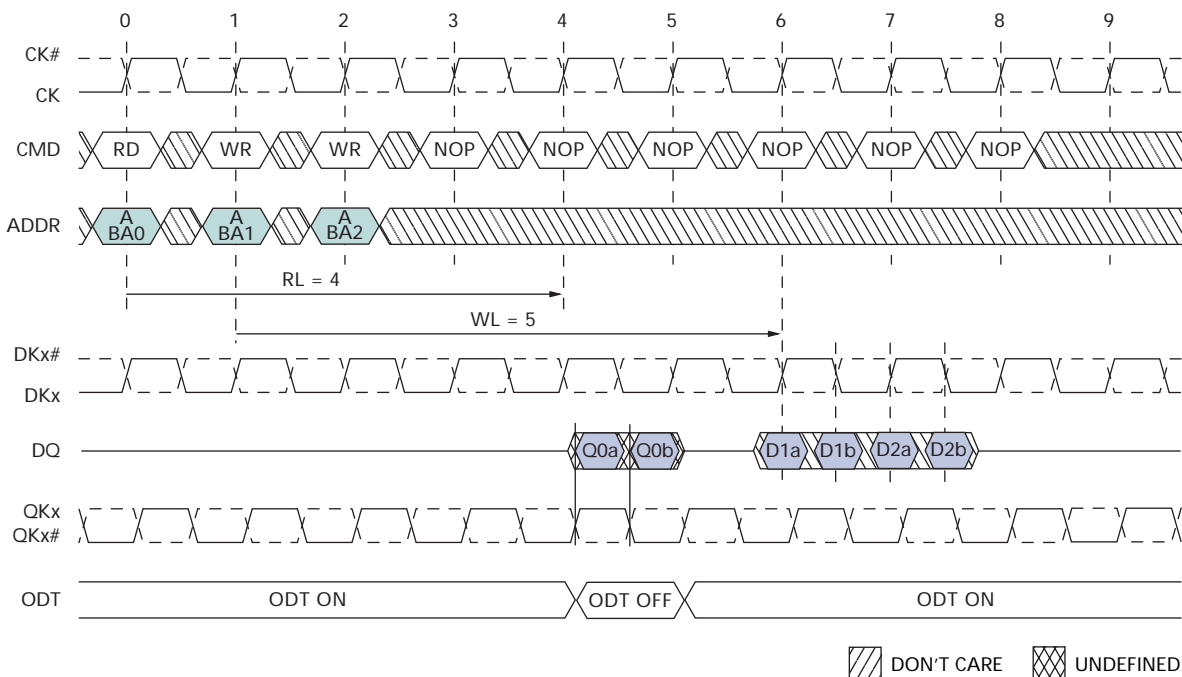
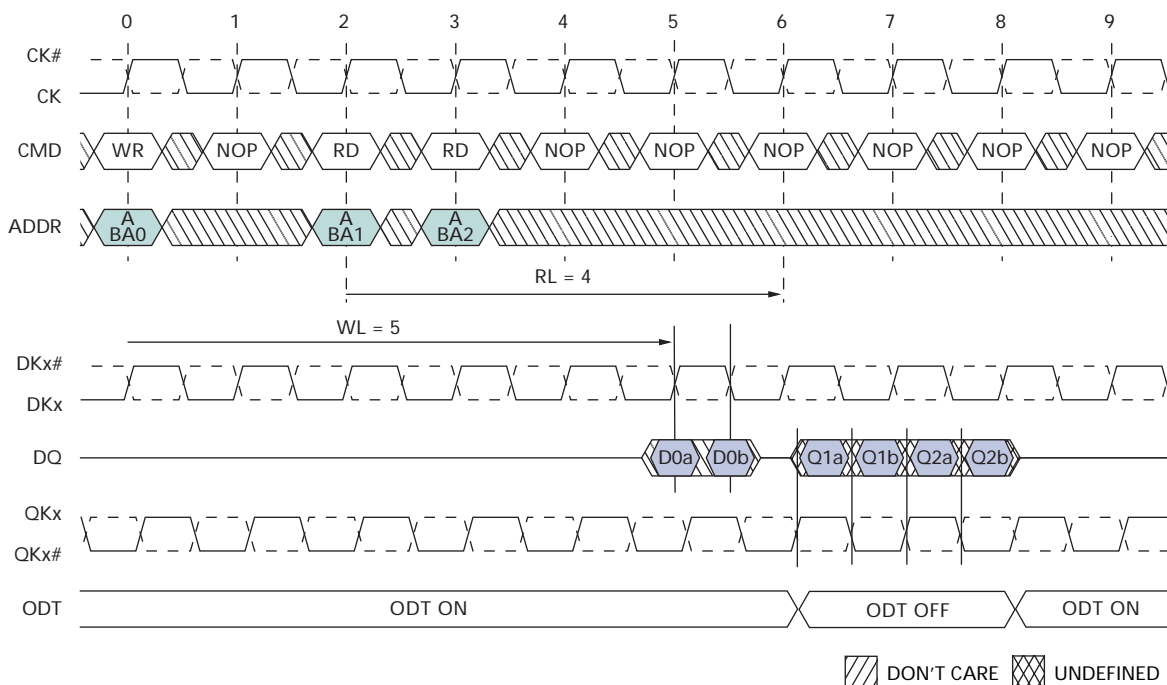


Figure 28: WRITE followed by READ with ODT: BL = 2, Configuration 1



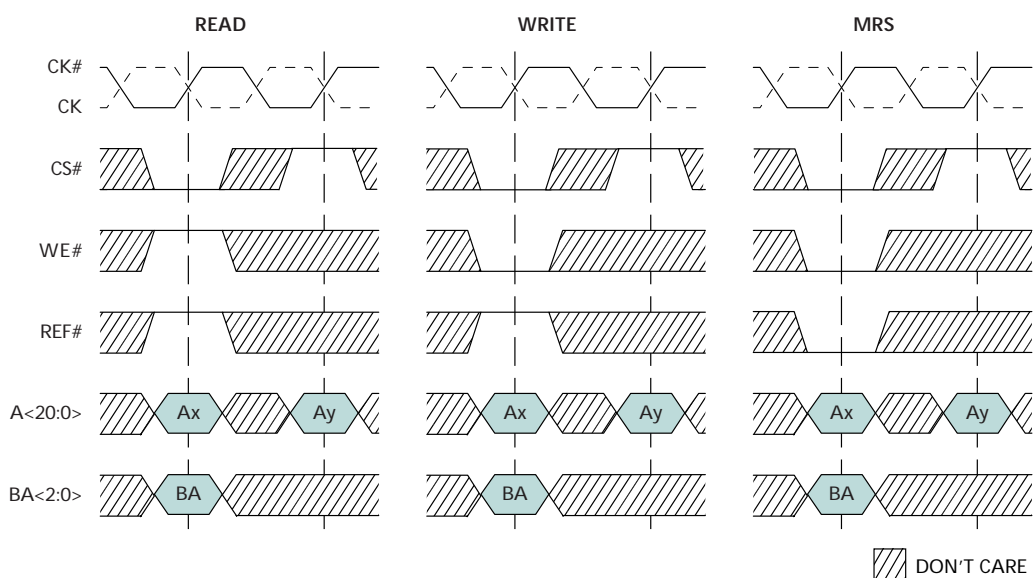


Operation with Multiplexed Addresses

In multiplexed address mode, the address can be provided to the RLDRAM in two parts that are latched into the memory with two consecutive rising clock edges. This provides the advantage that a maximum of 11 address balls are required to control the RLDRAM, reducing the number of balls on the controller side. The data bus efficiency in continuous burst mode is not affected for BL = 4 and BL = 8 since at least two clocks are required to read the data out of the memory. The bank addresses are delivered to the RLDRAM at the same time as the write command and the first address part, Ax.

This option is available by setting bit A5 to “1” in the mode register. Once this bit is set, the READ, WRITE, and MRS commands follow the format described in Figure 29. See Figure 31 on page 33 for the power-up sequence.

Figure 29: Command Description in Multiplexed Address Mode

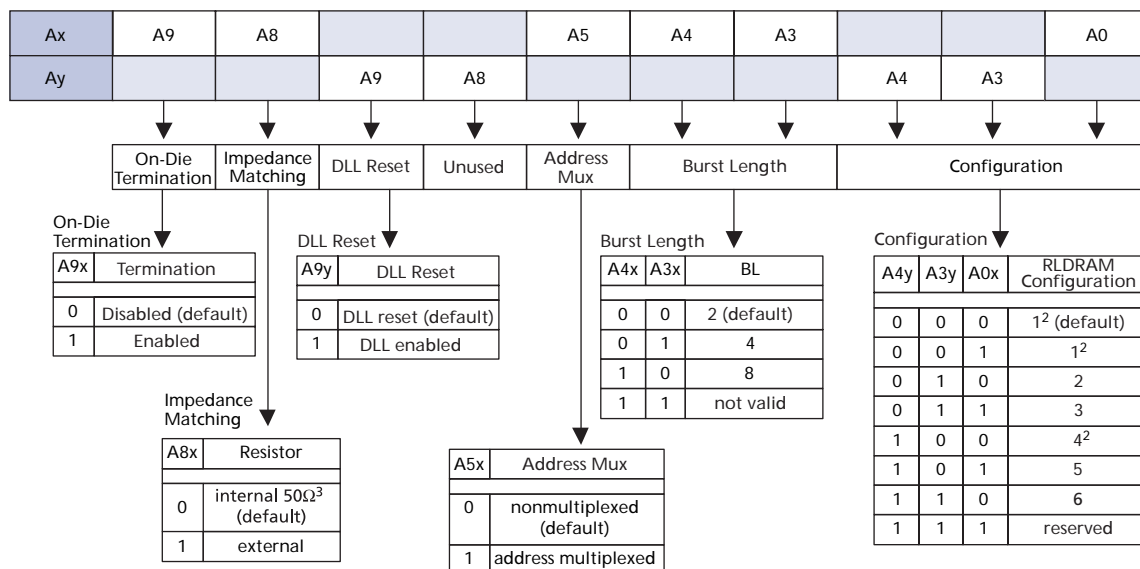


Notes: 1. The minimum setup and hold times of the two address parts are defined t_{AS} and t_{AH} .



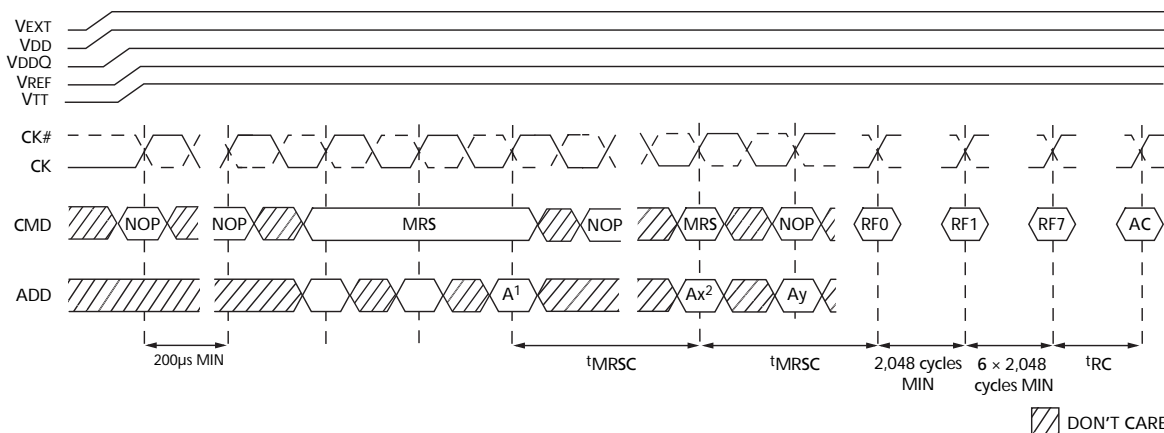
576Mb: x36, x18, x9 2.5V V_{EXT}, 1.8V V_{DD}, HSTL, RLD_{RAM} II Operation with Multiplexed Addresses

Figure 30: Mode Register Set Command in Multiplexed Address Mode



- Notes:
1. The addresses A0, A3, A4, A5, A8, and A9 must be set as follows in order to activate the mode register in the multiplexed address mode
 2. Bits A(17:10) *must* be set to zero.
 3. BL = 8 is not available for configuration 1.
 4. ±15% temperature variation.

Figure 31: Power-Up Sequence in Multiplexed Address Mode



- Notes:
1. The above sequence must be respected in order to power-up the RLD_{RAM} in the multiplexed address mode.
 2. Address A5 must be set HIGH (muxed address mode setting when RLD_{RAM} is in normal mode of operation).
 3. Address A5 must be set HIGH (muxed address mode setting when RLD_{RAM} is already in muxed address mode).



Address Mapping

The address mapping is described in Table 14 as a function of data width and burst length.

Table 14: Address Mapping in Multiplexed Address Mode

Note 1

Data Width	Burst Length	Ball	Address										
			A0 ²	A3	A4	A5 ³	A8	A9	A10	A13	A14	A17	A18
x36	BL = 2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	BL = 4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
	BL = 8	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	X
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
x18	BL = 2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	A20	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	BL = 4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	BL = 8	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
x9	BL = 2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	A20	A1	A2	A21	A6	A7	A19	A11	A12	A16	A15
	BL = 4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	A20	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	BL = 8	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15

- Notes: 1. X means "Don't Care."
 2. Reserved for A20 expansion in multiplexed mode.
 3. Reserved for A21 expansion in multiplexed mode.



Configuration Table

In multiplexed address mode, the read and write latencies are increased by one clock cycle. The RLD RAM cycle time remains the same, as described in Table 15.

Table 15: Configuration Table In Multiplexed Address Mode (Calculating ^tRC Based Off of Clock Frequency)

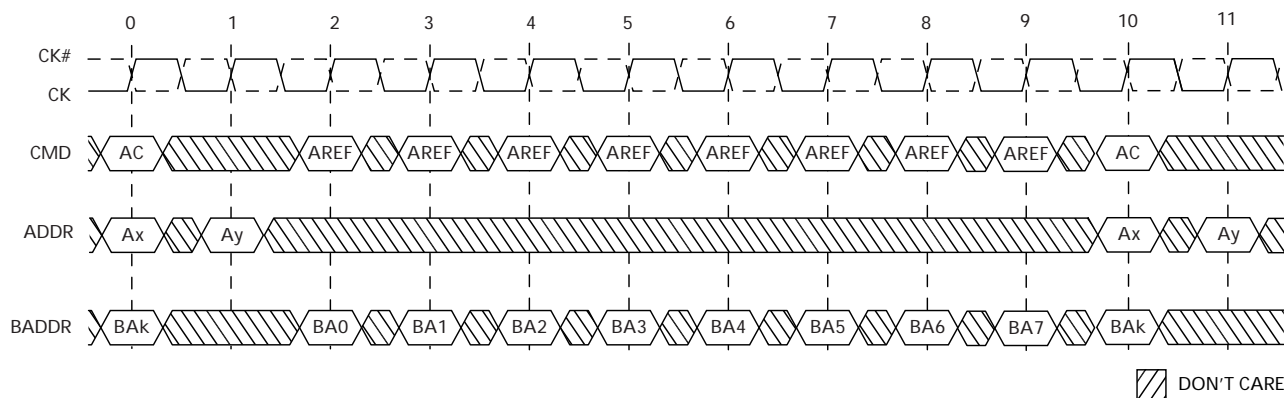
Frequency	Symbol	Configuration						Unit
		1 ¹	2	3	4 ¹	5	6	
	^t RC	4	6	8	3	5	7	cycles
	^t RL	5	7	9	4	6	8	cycles
	^t WL	6	8	10	5	7	9	cycles
533 MHz	^t RC			15.0				ns
	^t RL			16.875				ns
	^t WL			18.75				ns
400 MHz	^t RC		15.0	20.0			17.5	ns
	^t RL		17.5	22.5			20.0	ns
	^t WL		20.0	25.0			22.5	ns
300 MHz	^t RC		20.0	26.7		16.7	23.3	ns
	^t RL		23.3	30.0		20.0	26.7	ns
	^t WL		26.7	33.3		23.3	30.0	ns
200 MHz	^t RC	20.0	30.0	40.0	15.0	25.0	35.0	ns
	^t RL	25.0	35.0	45.0	20.0	30.0	40.0	ns
	^t WL	30.0	40.0	50.0	25.0	35.0	45.0	ns

Notes: 1. BL = 8 is not available for configurations 1 and 4.

REFRESH Command in Multiplexed Address Mode

Similar to other commands, the REFRESH command is executed on the next rising clock edge when in the multiplexed address mode. However, since only bank address is required for AREF, the next command can be applied on the following clock. The operation of the AREF command and any other command is represented in Figure 32.

Figure 32: Burst REFRESH Operation



Note: Ax: First part Ax of address
 Ay: Second part Ay of address
 BAK: Bank k; k is chosen so that ^tRC is met



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REFRESH Command in Multiplexed Address Mode

Figure 33: WRITE Burst Basic Sequence: BL = 4, with Multiplexed Addresses, Configuration 1, WL = 6

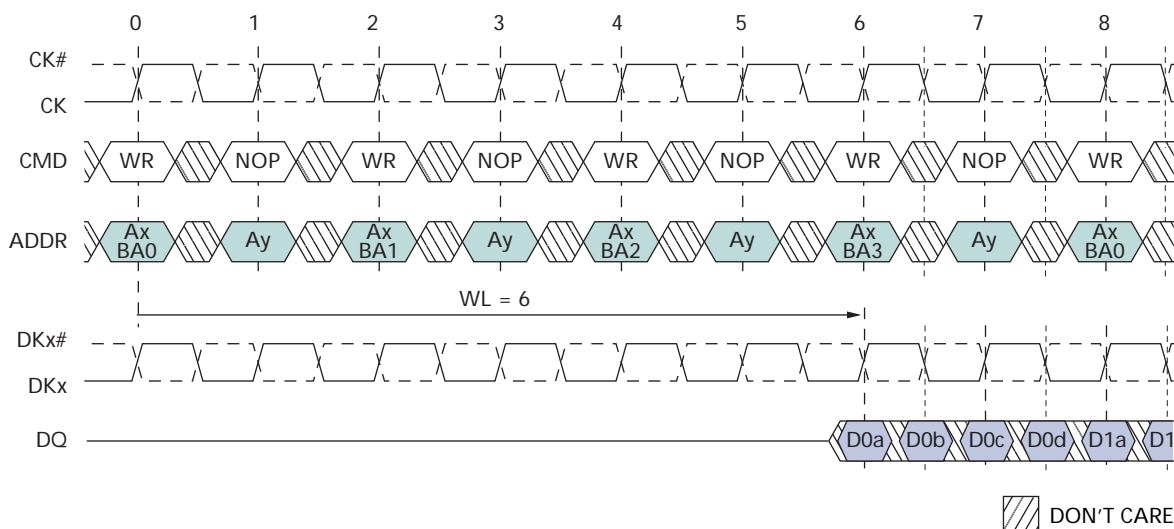
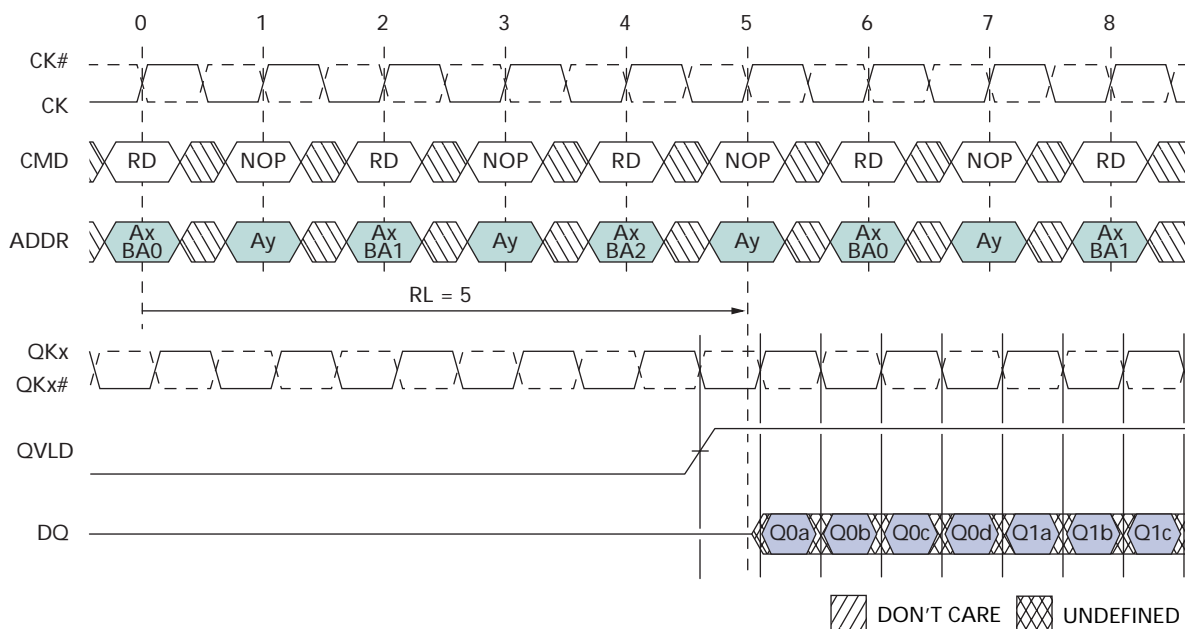


Figure 34: READ Burst Basic Sequence: BL = 4, with Multiplexed Addresses, Configuration 1, RL = 5





IEEE 1149.1 Serial Boundary Scan (JTAG)

RLDRAM incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-2001. The TAP operates using logic levels associated with the VDDQ supply.

RLDRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate RLD_{RAM} without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (VSS) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to VDD through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state, which will not interfere with the operation of the device.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 35 on page 38. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register (see Figure 36 on page 38).

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see Figure 35). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register (see Figure 36).



Figure 35: TAP Controller State Diagram

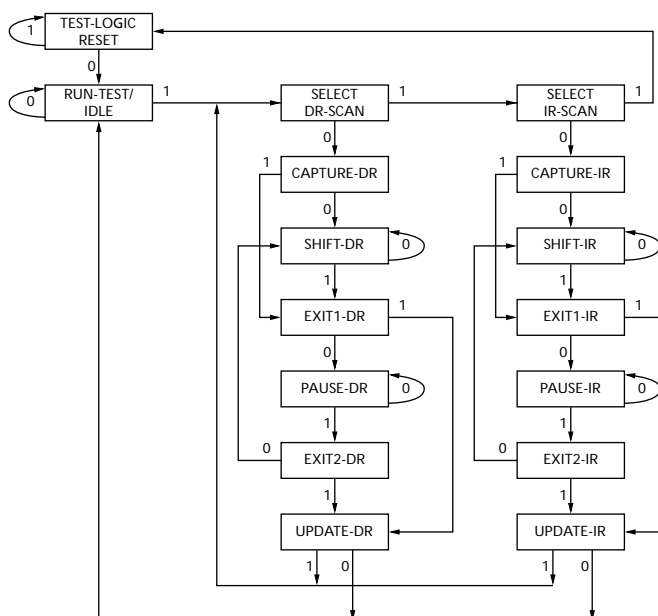
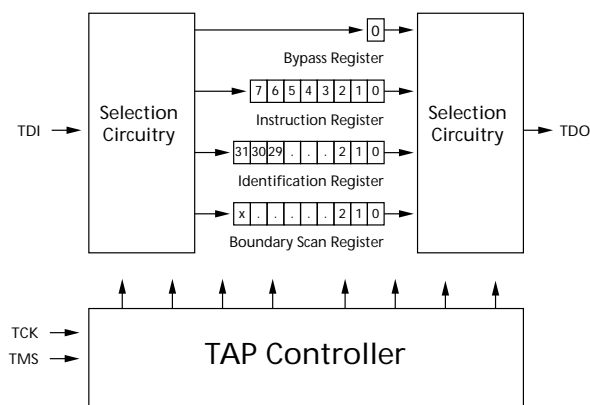


Figure 36: TAP Controller Block Diagram



Note: x = 112 for all configurations.

Performing a TAP RESET

A reset is performed by forcing TMS HIGH (V_{DDQ}) for five rising edges of TCK. This RESET does not affect the operation of the RLDRAM and may be performed while the RLDRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the RLDRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.



Instruction Register

Eight-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls, as shown in Figure 36 on page 38. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the RLDRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the RLDRAM. Several balls are also included in the scan register to reserved balls. The RLDRAM has a 113-bit register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state.

Table 22 on page 44 shows the order in which the bits are connected. Each bit corresponds to one of the balls on the RLDRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hard-wired into the RLDRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in Table 19 on page 43.

TAP Instruction Set

Overview

Many different instructions (2^8) are possible with the 8-bit instruction register. All used combinations are listed in Table 21 on page 43. These six instructions are described in detail below. The remaining instructions are reserved and should not be used.

The TAP controller used in this RLDRAM is fully compliant to the 1149.1 convention.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.



EXTEST

The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output balls are used to apply a test vector, while those at input balls capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the Update-IR state of EXTEST, the output driver is turned on and the PRELOAD data is driven onto the output balls.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

High-Z

The High-z instruction causes the boundary scan register to be connected between the TDI and TDO. This places all RLD RAM outputs into a High-Z state.

CLAMP

When the CLAMP instruction is loaded into the instruction register, the data driven by the output balls are determined from the values held in the boundary scan register.

SAMPLE/PRELOAD

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 50 MHz, while the RLD RAM clock operates significantly faster. Because there is a large difference between the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To ensure that the boundary scan register will capture the correct value of a signal, the RLD RAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (^tCS plus ^tCH). The RLD RAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO balls.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved for Future Use

The remaining 22 instructions are not implemented but are reserved for future use. Do not use these instructions.



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TAP Instruction Set

Figure 37: TAP Timing

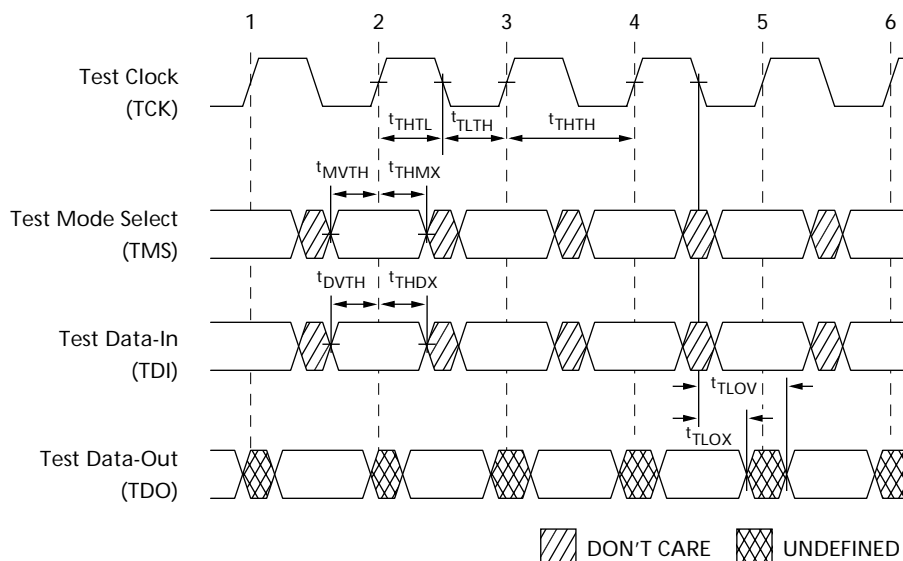


Table 16: TAP AC Electrical Characteristics and Operating Conditions

+0°C ≤ T_C ≤ +95°C; +1.7V ≤ V_{DD} ≤ +1.9V, unless otherwise noted

Description	Symbol	Min	Max	Units	Notes
Input high (Logic 1) voltage	V _{IH}	V _{REF} + 0.3	V _{DD} + 0.3	V	1, 2
Input low (Logic 0) voltage	V _{IL}	V _{SSQ} - 0.3	V _{REF} - 0.3	V	1, 2

- Notes: 1. All voltages referenced to V_{SS} (GND).
 2. Overshoot: V_{IH(AC)} ≤ V_{DD} + 0.7V for t ≤ t_{CK/2}.
 Undershoot: V_{IL(AC)} ≥ -0.5V for t ≤ t_{CK/2}.
 During normal operation, V_{DDQ} must not exceed V_{DD}.



576Mb: x36, x18, x9 2.5V V_{EXT}, 1.8V V_{DD}, HSTL, RLDRAM II TAP Instruction Set

Table 17: TAP AC Electrical Characteristics

 Note 1; +0°C ≤ T_C ≤ +95°C; +1.7V ≤ V_{DD} ≤ +1.9V

Description	Symbol	Min	Max	Units
Clock				
Clock cycle time	t ^T THH	20		ns
Clock frequency	f ^T TF		50	MHz
Clock HIGH time	t ^T HTL	10		ns
Clock LOW time	t ^T LT	10		ns
Output Times				
TCK LOW to TDO unknown	t ^T TLOX	0		ns
TCK LOW to TDO valid	t ^T TLOV		10	ns
TDI valid to TCK HIGH	t ^T DVTH	5		ns
TCK HIGH to TDI invalid	t ^T THDX	5		ns
Setup Times				
TMS setup	t ^T MVTH	5		ns
Capture setup	t ^T CS	5		ns
Hold Times				
TMS hold	t ^T THMX	5		ns
Capture hold	t ^T CH	5		ns

Notes: 1. t^TCS and t^TCH refer to the setup and hold time requirements of latching data from the boundary scan register.

Table 18: TAP DC Electrical Characteristics and Operating Conditions

 +0°C ≤ T_C ≤ +95°C; +1.7V ≤ V_{DD} ≤ +1.9V, unless otherwise noted

Description	Condition	Symbol	Min	Max	Units	Notes
Input high (Logic 1) voltage		V _{IH}	V _{REF} + 0.15	V _{DD} + 0.3	V	1, 2
Input low (Logic 0) voltage		V _{IL}	V _{SSQ} - 0.3	V _{REF} - 0.15	V	1, 2
Input leakage current	0V ≤ V _{IN} ≤ V _{DD}	I _{LI}	-5.0	5.0	μA	
Output leakage current	Output disabled, 0V ≤ V _{IN} ≤ V _{DDQ}	I _{LO}	-5.0	5.0	μA	
Output low voltage	I _{OLC} = 100μA	V _{OL1}		0.2	V	1
Output low voltage	I _{OLT} = 2mA	V _{OL2}		0.4	V	1
Output high voltage	I _{OHC} = 100μA	V _{OH1}	V _{DDQ} - 0.2		V	1
Output high voltage	I _{OHT} = 2mA	V _{OH2}	V _{DDQ} - 0.4		V	1

Notes: 1. All voltages referenced to V_{SS} (GND).
 2. Overshoot: V_{IH(AC)} ≤ V_{DD} + 0.7V for t ≤ t^TCK/2.
 Undershoot: V_{IL(AC)} ≥ -0.5V for t ≤ t^TCK/2.
 During normal operation, V_{DDQ} must not exceed V_{DD}.


Table 19: Identification Register Definitions

Instruction Field	All Devices	Description
Revision number (31:28)	abcd	ab = die revision cd = 10 for x36, 01 for x18, 00 for x9.
Device ID (27:12)	00jkidef10100111	def = 000 for 288M, 001 for 576M, 010 for 1G. i = 0 for common I/O, 1 for separate I/O. jk = 00 for RLD RAM, 01 for RLD RAM II.
Micron JEDEC ID code (11:1)	00000101100	Allows unique identification of RLD RAM vendor.
ID register presence indicator (0)	1	Indicates the presence of an ID register.

Table 20: Scan Register Sizes

Register Name	Bit Size
Instruction	8
Bypass	1
ID	32
Boundary scan	113

Table 21: Instruction Codes

Instruction	Code	Description
Extest	0000 0000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This operation does not affect RLD RAM operations.
ID Code	0010 0001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect RLD RAM operations.
Sample/Preload	0000 0101	Captures I/O ring contents. Places the boundary scan register between TDI and TDO.
Clamp	0000 0111	Selects the bypass register to be connected between TDI and TDO. Data driven by output balls are determined from values held in the boundary scan register.
High-Z	0000 0011	Selects the bypass register to be connected between TDI and TDO. All outputs are forced into High-Z state.
Bypass	1111 1111	Places the bypass register between TDI and TDO. This operation does not affect RLD RAM operations.


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TAP Instruction Set**
Table 22: Boundary Scan (Exit) Order

Bit#	μBGA Ball	Bit#	μBGA Ball	Bit#	μBGA Ball
1	K1	39	R11	77	C11
2	K2	40	R11	78	C11
3	L2	41	P11	79	C10
4	L1	42	P11	80	C10
5	M1	43	P10	81	B11
6	M3	44	P10	82	B11
7	M2	45	N11	83	B10
8	N1	46	N11	84	B10
9	P1	47	N10	85	B3
10	N3	48	N10	86	B3
11	N3	49	P12	87	B2
12	N2	50	N12	88	B2
13	N2	51	M11	89	C3
14	P3	52	M10	90	C3
15	P3	53	M12	91	C2
16	P2	54	L12	92	C2
17	P2	55	L11	93	D3
18	R2	56	K11	94	D3
19	R3	57	K12	95	D2
20	T2	58	J12	96	D2
21	T2	59	J11	97	E2
22	T3	60	H11	98	E2
23	T3	61	H12	99	E3
24	U2	62	G12	100	E3
25	U2	63	G10	101	F2
26	U3	64	G11	102	F2
27	U3	65	E12	103	F3
28	V2	66	F12	104	F3
29	U10	67	F10	105	E1
30	U10	68	F10	106	F1
31	U11	69	F11	107	G2
32	U11	70	F11	108	G3
33	T10	71	E10	109	G1
34	T10	72	E10	110	H1
35	T11	73	E11	111	H2
36	T11	74	E11	112	J2
37	R10	75	D11	113	J1
38	R10	76	D10	-	-

Notes: 1. Any unused balls that are in the order will read as a logic "0."



Electrical Characteristics

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Figure 38: Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
Storage temperature	-55	+150	°C	
I/O voltage	-0.3V	V _{DDQ} + 0.3	V	
Voltage on V _{EXT} supply relative to V _{SS}	-0.3	+2.8	V	
Voltage on V _{DD} supply relative to V _{SS}	-0.3	+2.1	V	
Voltage on V _{DDQ} supply relative to V _{SS}	-0.3	+2.1	V	
Junction temperature	110		°C	1

Notes: 1. Junction temperature depends upon package type, cycle time, loading, ambient temperature, and airflow.

Table 23: DC Electrical Characteristics and Operating Conditions

+0°C ≤ T_C ≤ +95°C; +1.7V ≤ V_{DD} ≤ +1.9V, unless otherwise noted

Description	Condition	Symbol	Min	Max	Units	Notes
Supply voltage		V _{EXT}	2.38	2.63	V	1
Supply voltage		V _{DD}	1.7	1.9	V	1, 4
DLL supply		V _{DDL}	1.7	V _{DD}	V	4
Isolated output buffer supply		V _{DDQ}	1.4	V _{DD}	V	1, 4, 5
Reference voltage		V _{REF}	0.49 × V _{DDQ}	0.51 × V _{DDQ}	V	1–3, 8
Termination voltage		V _{TT}	0.95 × V _{REF}	1.05 × V _{REF}	V	9, 10
Input high (Logic 1) voltage		V _{IH}	V _{REF} + 0.1	V _{DDQ} + 0.3	V	1, 4
Input low (Logic 0) voltage		V _{IL}	V _{SSQ} - 0.3	V _{REF} - 0.1	V	1, 4
Output high current	V _{OH} = V _{DDQ} /2	I _{OH}	(V _{DDQ} /2) / (1.15 × R _O /5)	(V _{DDQ} /2) / (0.85 × R _O /5)	mA	6, 7, 11
Output low current	V _{OL} = V _{DDQ} /2	I _{OL}	(V _{DDQ} /2) / (1.15 × R _O /5)	(V _{DDQ} /2) / (0.85 × R _O /5)	mA	6, 7, 11
Clock input leakage current	0V ≤ V _{IN} ≤ V _{DD}	I _{LC}	-5	5	μA	
Input leakage current	0V ≤ V _{IN} ≤ V _{DD}	I _{LI}	-5	5	μA	
Output leakage current	0V ≤ V _{IN} ≤ V _{DDQ}	I _{LO}	-5	5	μA	
Reference voltage current		I _{REF}	-5	5	μA	

- Notes: 1. All voltages referenced to V_{SS} (GND).
 2. Typically the value of V_{REF} is expected to be 0.5 × V_{DDQ} of the transmitting device. V_{REF} is expected to track variations in V_{DDQ}.
 3. Peak-to-peak AC noise on V_{REF} must not exceed ±2% V_{REF}(DC).
 4. Overshoot: V_{IH}(AC) ≤ V_{DD} + 0.7V for t ≤ t_{CK}/2.
 Undershoot: V_{IL}(AC) ≥ -0.5V for t ≤ t_{CK}/2.
 During normal operation, V_{DDQ} must not exceed V_{DD}.
 Control input signals may not have pulse widths less than t_{CK}/2 or operate at frequencies exceeding t_{CK} (MAX).
 5. V_{DDQ} can be set to a nominal 1.5V + 0.1V or 1.8V + 0.1V supply.



576Mb: x36, x18, x9 2.5V V_{EXT}, 1.8V V_{DD}, HSTL, RLD RAM II Electrical Characteristics

6. I_{OH} and I_{OL} are defined as absolute values and are measured at V_{DDQ}/2. I_{OH} flows from the device, I_{OL} flows into the device.
7. If MRS bit A8 is 0, use R_Q = 250Ω in the equation in lieu of presence of an external impedance matched resistor.
8. V_{REF} is expected to equal V_{DDQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±2% of the DC value. Thus, from V_{DDQ}/2, V_{REF} is allowed ±2%V_{DDQ}/2 for DC error and an additional ±2%V_{DDQ}/2 for AC noise. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
9. V_{TT} is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
10. On-die termination may be selected using mode register bit 9 (see Figure 8 on page 19). A resistance R_{TT} from each data input signal to the nearest V_{TT} can be enabled. R_{TT} = 150Ω (±10%) at +70°C T_C.
11. For V_{OL} and V_{OH}, refer to the RLD RAM II HSpice or IBIS driver models.

Table 24: AC Electrical Characteristics and Operating Conditions

+0°C ≤ T_C ≤ +95°C; +1.7V ≤ V_{DD} ≤ +1.9V, unless otherwise noted

Description	Conditions	Symbol	Min	Max	Units
Input high (Logic 1) voltage	Matched impedance mode	V _{IH}	V _{REF} + 0.2	V _{DDQ} + 0.3	V
Input low (Logic 0) voltage	Matched impedance mode	V _{IL}	V _{SSQ} - 0.3	V _{REF} - 0.2	V

Table 25: Capacitance

Description	Conditions	Symbol	Min	Max	Units
Address/Control input capacitance	T _A = 25°C; f = 1 MHz	C _I	1.5	2.5	pF
I/O capacitance (DQ, DM, QK)		C _O	3.5	5.0	pF
Clock capacitance		C _{CK}	2.0	3.0	pF

Figure 39: Output Test Conditions

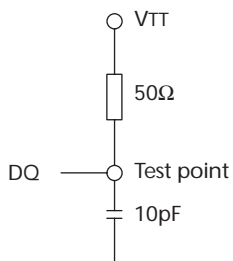
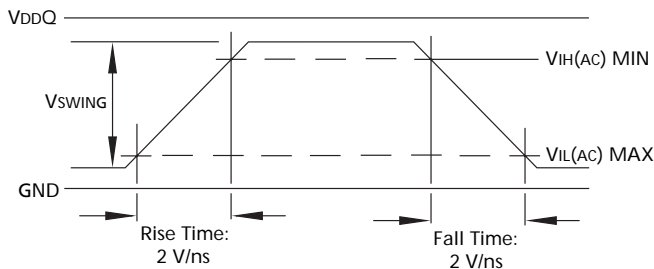


Figure 40: Input Waveform





576Mb: x36, x18, x9 2.5V V_{EXT}, 1.8V V_{DD}, HSTL, RLD_{RAM} II Electrical Characteristics

Table 26: IDD Operating Conditions and Maximum Limits

Notes 1–6 on page 48

Description	Condition	Symbol	Max						Units
			-18E	-25E	-25Z	-25	-33	-33	
Standby current	t _{CK} = Idle All banks idle, no inputs toggling	ISB1 (V _{DD}) x36	48	48	48	48	48	48	mA
		ISB1 (V _{DD}) x18/x9	48	48	48	48	48	48	
		ISB1 (V _{EXT})	26	26	26	26	26	26	
Active standby current	CS# = 1 No commands, half bank/address/ data change once every four clock cycles	ISB2 (V _{DD}) x36	288	233	233	233	189	189	mA
		ISB2 (V _{DD}) x18/x9	288	233	233	233	189	189	
		ISB2 (V _{EXT})	26	26	26	26	26	26	
Operational current	BL = 2, sequential bank access, bank transitions once every t _{RC} , half address transitions once every t _{RC} , read followed by write sequence, continuous data during WRITE commands	IDD1 (V _{DD}) x36	374	343	343	343	292	292	mA
		IDD1 (V _{DD}) x18/x9	348	305	305	305	255	255	
		IDD1 (V _{EXT})	41	36	36	36	32	32	
Operational current	BL = 4, sequential bank access, bank transitions once every t _{RC} , half address transitions once every t _{RC} , read followed by write sequence, continuous data during WRITE commands	IDD 2 (V _{DD}) x36	418	389	389	389	339	339	mA
		IDD2 (V _{DD}) x18/x9	362	319	269	362	319	269	
		IDD2 (V _{EXT})	48	42	42	42	39	39	
Operational current	BL = 8, sequential bank access, bank transitions once every t _{RC} , half address transitions once every t _{RC} , read followed by write sequence, continuous data during WRITE commands	IDD 3 (V _{DD}) x36	454	411	411	411	347	347	mA
		IDD3 (V _{DD}) x18/x9	408	368	368	368	286	286	
		IDD3 (V _{EXT})	55	48	48	48	41	41	
Burst refresh current	Eight bank cyclic refresh, continuous address/data, command bus remains in refresh for all eight banks	IREF1 (V _{DD}) x36	685	545	545	545	375	375	mA
		IREF1 (V _{DD}) x18/x9	680	530	530	530	367	367	
		IREF1 (V _{EXT})	133	111	111	111	105	105	
Distributed refresh current	Single bank refresh, sequential bank access, half address transitions once every t _{RC} , continuous data	IREF2 (V _{DD}) x36	326	281	281	281	227	227	mA
		IREF2 (V _{DD}) x18/x9	325	267	367	367	221	221	
		IREF2 (V _{EXT})	48	42	42	42	39	39	
Operating burst write current example	BL = 2, cyclic bank access, half of address bits change every clock cycle, continuous data, measurement is taken during continuous WRITE	IDD2W (V _{DD}) x36	990	914	914	914	676	676	mA
		IDD2W (V _{DD}) x18/x9	970	819	819	819	597	597	
		IDD2W (V _{EXT})	100	90	90	90	69	69	
Operating burst write current example	BL = 4, cyclic bank access, half of address bits change every two clocks, continuous data, measurement is taken during continuous WRITE	IDD4W (V _{DD}) x36	882	790	567	882	790	567	mA
		IDD4W (V _{DD}) x18/x9	779	609	439	779	609	439	
		IDD4W (V _{EXT})	88	77	77	77	63	63	
Operating burst write current example	BL = 8, cyclic bank access, half of address bits change every four clock cycles, continuous data, measurement is taken during continuous WRITE	IDD8W (V _{DD}) x36	737	617	617	617	461	461	mA
		IDD8W (V _{DD}) x18/x9	668	525	525	525	364	364	
		IDD8W (V _{EXT})	60	51	51	51	40	40	



576Mb: x36, x18, x9 2.5V V_{EXT}, 1.8V V_{DD}, HSTL, RLDRAM II Electrical Characteristics

Table 26: IDD Operating Conditions and Maximum Limits (continued)

Notes 1–6 on page 48

Description	Condition	Symbol	Max						Units
			-18E	-25E	-25Z	-25	-33	-33	
Operating burst read current example	BL = 2, cyclic bank access, half of address bits change every clock cycle, measurement is taken during continuous READ	IDD2R (VDD) x36	920	850	850	850	628	628	mA
		IDD2R (VDD) x18/x9	902	761	761	761	555	555	
		IDD2R (VEXT)	100	90	90	90	69	69	
Operating burst read current example	BL = 4, cyclic bank access, half of address bits change every two clocks, measurement is taken during continuous READ	IDD4R (VDD) x36	764	734	734	734	527	527	mA
		IDD4R (VDD) x18/x9	724	566	566	566	408	408	
		IDD4R (VEXT)	88	77	77	77	63	63	
Operating burst read current example	BL = 8, cyclic bank access, half of address bits change every four clock cycles, measurement is taken during continuous READ	IDD8R(VDD) x36	680	593	593	593	462	462	mA
		IDD8R (VDD) x18/x9	621	488	488	488	338	338	
		IDD8R (VEXT)	60	51	51	51	40	40	

- Notes:
1. IDD specifications are tested after the device is properly initialized. $+0^{\circ}\text{C} \leq T_C \leq +95^{\circ}\text{C}$; $+1.7\text{V} \leq V_{DD} \leq +1.9\text{V}$, $+2.38\text{V} \leq V_{EXT} \leq +2.63\text{V}$, $+1.4\text{V} \leq V_{DDQ} \leq +1.6\text{V}$, $V_{REF} = V_{DDQ}/2$.
 2. $t_{CK} = t_{DK} = \text{MIN}$, $t_{RC} = \text{MIN}$.
 3. Input slew rate is specified in Table 23 on page 45.
 4. Definitions for IDD conditions:
 - a. LOW is defined as $V_{IN} \leq V_{IL(AC)} \text{ MAX}$.
 - b. HIGH is defined as $V_{IN} \leq V_{IH(AC)} \text{ MAX}$.
 - c. Stable is defined as inputs remaining at a HIGH or LOW level.
 - d. Floating is defined as inputs at $V_{REF} = V_{DDQ}/2$.
 - e. Continuous data is defined as half the DQ signals changing between HIGH and LOW every half clock cycle (twice per clock).
 - f. Continuous address is defined as half the address signals changing between HIGH and LOW every clock cycle (once per clock).
 - g. Sequential bank access is defined as the bank address incrementing by one every t_{RC} .
 - h. Cyclic bank access is defined as the bank address incrementing by one for each command access. For BL = 4 this is every other clock.
 5. CS# is HIGH unless a READ, WRITE, AREF, or MRS command is registered. CS# never transitions more than once per clock cycle.
 6. IDD parameters are specified with ODT disabled.

