# GRAPHICS DDR3 SDRAM

## MT44H8M32 – 2 MEG x 32 x 4 BANKS

*For the latest data sheet, please refer to the Micron Web site: www.micron.com/datasheets*

### Features

- VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V
- Single ended READ Strobe (RDQS) per byte
- Single ended WRITE Strobe (WDQS) per byte
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Calibrated output drive
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- RDQS edge-aligned with data for READs
- WDQS center-aligned with data for WRITEs
- Four internal banks for concurrent operation
- Data mask (DM) for masking WRITE data
- 4*n* prefetch
- Programmable burst lengths: 4 and 8
- 32ms, 4K-cycle auto refresh
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- 1.8V Pseudo Open Drain Logic I/O
- Concurrent Auto Precharge support
- $^{t}$RAS lockout support
- On-die termination (ODT)
- Programmable write latency (1, 2, 3, or 4)

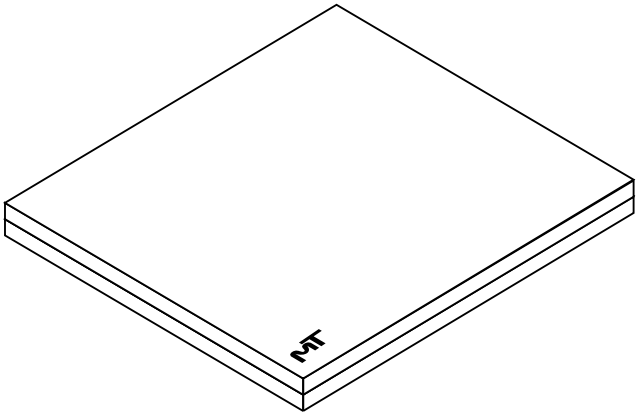
### Options — Marking

- Configuration
  - 8 Meg x 32 (2 Meg x 32 x 4 banks) — 8M32
- CK and CK# On-Die Termination
  - Enabled [1,2] — F1
  - Disabled — F2
- Package
  - 12mm x 13mm 135-ball FBGA — FW
- Timing – Cycle Time
  - 600 MHz @ CL = 8 — -16
  - 550 MHz @ CL = 7 — -18
  - 500 MHz @ CL = 6 — -2

NOTE:

1. ODT values subject to change.
2. Contact Micron for availability.

**Figure 1: FBGA Package**




### Table 1: Addressing

| | 8 MEG x 32 |
|---|---|
| Configuration | 2 Meg x 32 x 4 banks |
| Refresh Count | 4,096 |
| Row Addressing | 4,096 (A0–A11) |
| Bank Addressing | 4 (BA0, BA1) |
| Column Addressing | 512 (A0–A7,A9) |

### Table 2: Key Timing Parameters

CL = CAS (Read) latency

| SPEED GRADE | CLOCK RATE | | | |
|---|---|---|---|---|
| | CL = 8 | CL = 7 | CL = 6 | CL = 5 |
| -16 | 600 MHz | 550 MHz | 500 MHz | 450 MHz |
| -18 | – | 550 MHz | 500 MHz | 400 MHz |
| -2 | – | – | 500 MHz | 400 MHz |

*Part Number Example*

**MT44H8M32F2FW-16**

NOTE: Due to space limitations, FBGA-packaged components have an abbreviated part mark that is different from the part number. See our Web site for more information on abbreviated component marks.

## General Description

The 256Mb (x32) graphics DDR3 (GDDR3) DRAM is a high-speed CMOS, dynamic random access memory containing 268,435,456 bits. It is internally configured as a quad-bank DRAM.

The 256Mb GDDR3 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer four data bits every two clock cycles at the I/O pins. A single read or write access for the 256Mb GDDR3 SDRAM effectively consists of a single 4*n*-bit-wide, data transfer at the internal DRAM core.

The single-ended WRITE data strobes (WDQS 0–3) are transmitted externally, along with data, for use in data capture at the GDDR3 SDRAM input receiver. WDQS is center-aligned with data for WRITEs. The READ data is transmitted by the GDDR3 SDRAM edge-aligned to the READ strobes (RDQS 0–3).

The 256Mb GDDR3 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on first rising edge of WDQS after the one-half cycle WRITE preamble, and output data is referenced on the first rising edge of RDQS after the one-half cycle READ preamble.

Read and write accesses to the GDDR3 SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a specified sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The GDDR3 SDRAM provides for programmable read or write burst lengths of four and eight locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAMs, the pipelined, multibank architecture of GDDR3 SDRAMs allows for concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode.

NOTE: Throughout the data sheet, the various figures and text refer to DQs as “DQ.” The DQ term is to be interpreted as any and all DQs collectively, unless specifically stated otherwise.

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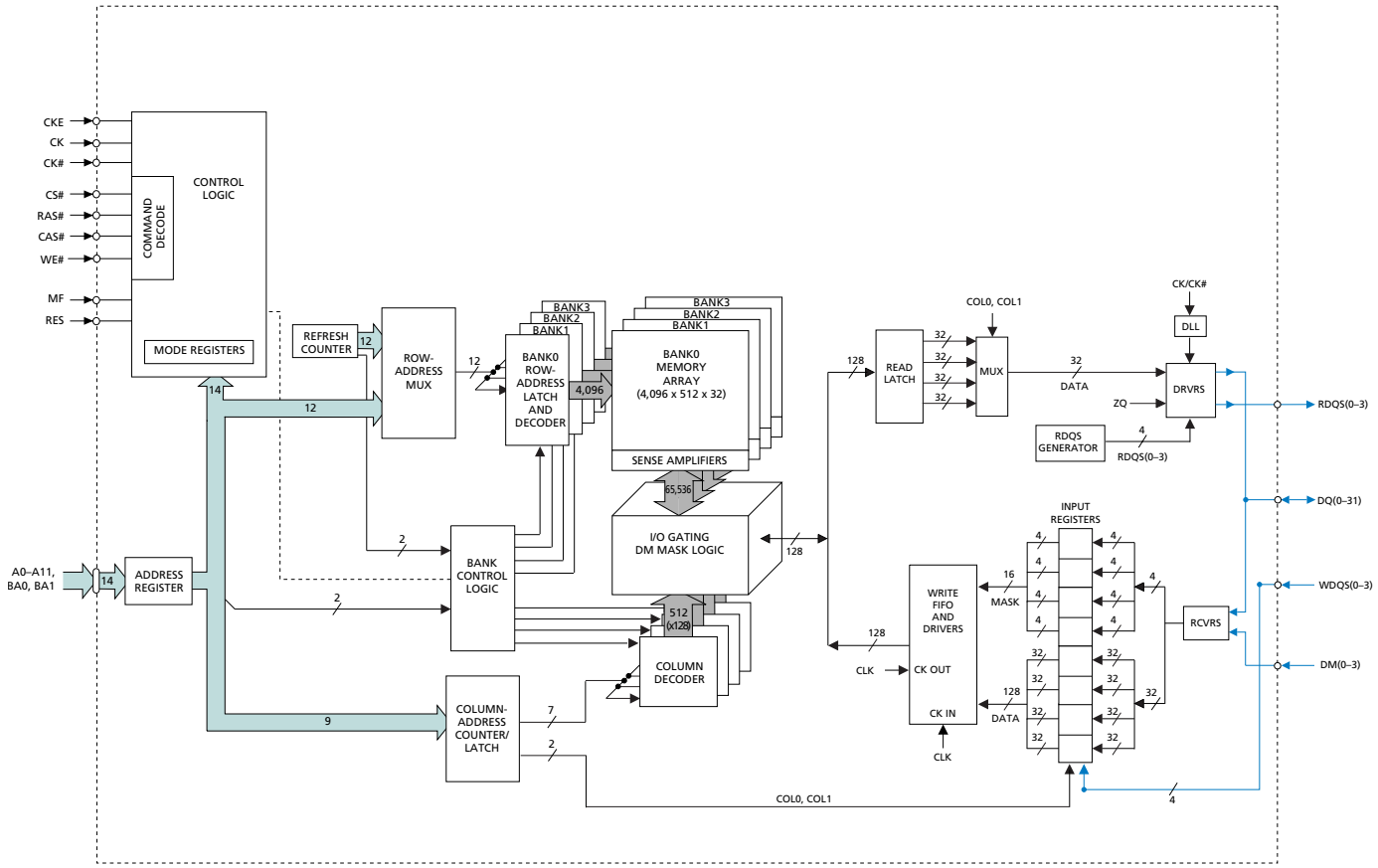
## Figure 2: Functional Block Diagram (8 Meg x 32)



## Table 3: 135 Ball/Pin Descriptions

| FBGA BALL-OUT | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|
| J6, H6 | CK, CK# | Input | Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. |
| G2 | CKE | Input | Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK#, and CKE) are disabled during POWER- DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. |
| F10 | CS# | Input | Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code. |
| G1, F2, G10 | RAS#, CAS#,WE# | Input | Command Inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered. |
| D4, D8, M8, M4 | DM0–DM3 | Input | Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a write access. DM is sampled on the rising and falling edges of WDQS. |
| F1, F11 | BA0, BA1 | Input | Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. |
| H(1, 2, 10, 11), J(1–4, 8–11) | A0–A11 | Input | Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A8) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A8 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A8 LOW, bank selected by BA0, BA1) or all banks (A8 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command. |
| A2–4, B2–4, C2, D3, | DQ0–7 | I/O | Data Input/Output: Bidirectional data bus. |
| A8–10, B8–10, C10, D9 | DQ8–15 | I/O | Data Input/Output: Bidirectional data bus. |
| M9, N10, P8–10, R8–10 | DQ16–23 | I/O | Data Input/Output: Bidirectional data bus. |
| M3, N2, P2–4, R2–4 | DQ24–31 | I/O | Data Input/Output: Bidirectional data bus. |
| C3, C9, N8, N4 | RDQS(0–3) | Output | READ Data Strobe: Output with read data. RDQS is edge-aligned with read data. |
| C4, C8, N9, N3 | WDQS(0–3) | Input | WRITE Data strobe: Input with write data. WDQS is center-aligned to the input data. |
| K(1, 2, 10, 11),G11 | NC/RFU | | Reserved for Future Use. |
| A(1, 11), C(1, 11), E(1, 2, 10, 11), F(4, 8), K(4, 8), L(1, 2, 10, 11), N(1, 11), R(1, 11) | $V_{DDQ}$ | Supply | DQ Power Supply: +1.8V ±0.1V. Isolated on the die for improved noise immunity. |

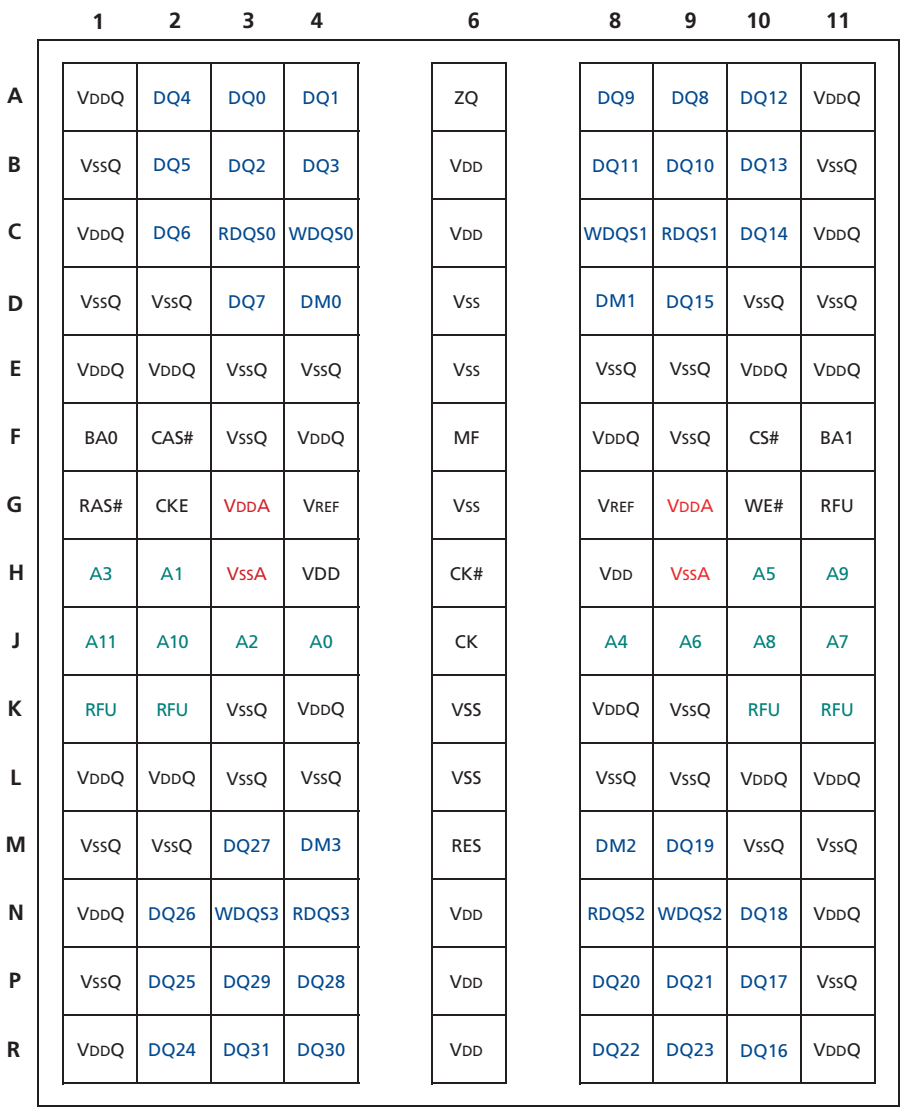
## Table 3: 135 Ball/Pin Descriptions (Continued)

| FBGA BALL-OUT | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|
| B(1, 11), D(1, 2, 10, 11), F(3, 9), E(3, 4, 8, 9), M(1,2,10,11), L(3, 4, 8, 9), P(1, 11), K(3,9) | VSSQ | Supply | DQ Ground: Isolated on the die for improved noise immunity. |
| B6, C6, H(4, 8), N6, P6, R6 | VDD | Supply | Power Supply: +1.8V ±0.1V. |
| D6, E6, G6, K6, L6 | VSS | Supply | Ground. |
| G(4, 8) | VREF | Supply | Reference Voltage. |
| G(3, 9) | VDDA | Supply | DLL Power Supply. |
| H(3, 9) | VSSA | Supply | DLL Ground. |
| F6 | MF | Reference | Mirror Pin. |
| A6 | ZQ | Reference | External Reference Pin for the Output Drive. |
| M6 | RES | Input | Reset Pin. |

NOTE:

1. RFU pins not listed may also be reserved for other uses now or in the future. This table simply defines specific RFU pins deemed to be of importance.

## Figure 3: 135 FBGA Ballout



| | 1 | 2 | 3 | 4 | 6 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|
| A | VDDQ | DQ4 | DQ0 | DQ1 | ZQ | DQ9 | DQ8 | DQ12 | VDDQ |
| B | VSSQ | DQ5 | DQ2 | DQ3 | VDD | DQ11 | DQ10 | DQ13 | VSSQ |
| C | VDDQ | DQ6 | RDQS0 | WDQS0 | VDD | WDQS1 | RDQS1 | DQ14 | VDDQ |
| D | VSSQ | VSSQ | DQ7 | DM0 | VSS | DM1 | DQ15 | VSSQ | VSSQ |
| E | VDDQ | VDDQ | VSSQ | VSSQ | VSS | VSSQ | VSSQ | VDDQ | VDDQ |
| F | BA0 | CAS# | VSSQ | VDDQ | MF | VDDQ | VSSQ | CS# | BA1 |
| G | RAS# | CKE | VDDA | VREF | VSS | VREF | VDDA | WE# | RFU |
| H | A3 | A1 | VSSA | VDD | CK# | VDD | VSSA | A5 | A9 |
| J | A11 | A10 | A2 | A0 | CK | A4 | A6 | A8 | A7 |
| K | RFU | RFU | VSSQ | VDDQ | VSS | VDDQ | VSSQ | RFU | RFU |
| L | VDDQ | VDDQ | VSSQ | VSSQ | VSS | VSSQ | VSSQ | VDDQ | VDDQ |
| M | VSSQ | VSSQ | DQ27 | DM3 | RES | DM2 | DQ19 | VSSQ | VSSQ |
| N | VDDQ | DQ26 | WDQS3 | RDQS3 | VDD | RDQS2 | WDQS2 | DQ18 | VDDQ |
| P | VSSQ | DQ25 | DQ29 | DQ28 | VDD | DQ20 | DQ21 | DQ17 | VSSQ |
| R | VDDQ | DQ24 | DQ31 | DQ30 | VDD | DQ22 | DQ23 | DQ16 | VDDQ |

NOTE:

RFU pins not listed may also be reserved for other uses now or in the future. This table simply defines specific RFU pins deemed to be of importance.

## Functional Description

The 256Mb GDDR3 SDRAM is a high-speed CMOS, dynamic random access memory containing 268,435,456 bits. The 256Mb GDDR3 SDRAM is internally configured as a quad-bank DRAM.

The 256Mb GDDR3 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 256Mb GDDR3 SDRAM consists of a 4*n* data transfer every two clock cycles at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the GDDR3 SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the GDDR3 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

## Initialization

GDDR3 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to $V_{DD}$ and $V_{DD}Q$ simultaneously, and then to $V_{REF}$. $V_{REF}$ can be applied any time after $V_{DD}Q$. Inputs are not recognized as valid until after $V_{REF}$ is applied. Once power has been applied, the GDDR3 device requires 100µs for the power supplies to stabilize before the RES pin transitions to HIGH. Upon power-up, the on-die termination value for the address and control pins will be set, based on the state of CKE when the RES pin transitions from LOW to HIGH. The on-die termination for CK and CK# will also be set for the T1 version of the die at this time. On the rising edge of RES, the CKE pin is latched to determine the on-die termination value for the address and control lines. In a single-rank system, CKE is sampled at a logic LOW with the on-die termination set to one-half of ZQ, and for a dual-rank system, CKE is sampled logic HIGH to set the on-die termination to the same value as ZQ. CKE must meet $^{t}$ATS and $^{t}$ATH on the rising edge of RES to set the on-die termination for either a single- or dual-rank system. Once $^{t}$ATH is met, CKE needs to be brought LOW while the on-die termination and output drivers calibrate.

RES must be maintained at a logic LOW level value during the first stage of power-up to ensure that the DQ outputs will be in a predefined state, where they will remain until the RES pin is brought HIGH. After the RES pin is brought HIGH, all outputs will be pulled HIGH by the on-die termination until driven by a READ command.

After all power supplies and reference voltages are stable, and the clock is stable, the GDDR3 SDRAM requires a 200µs delay prior to applying an executable command.

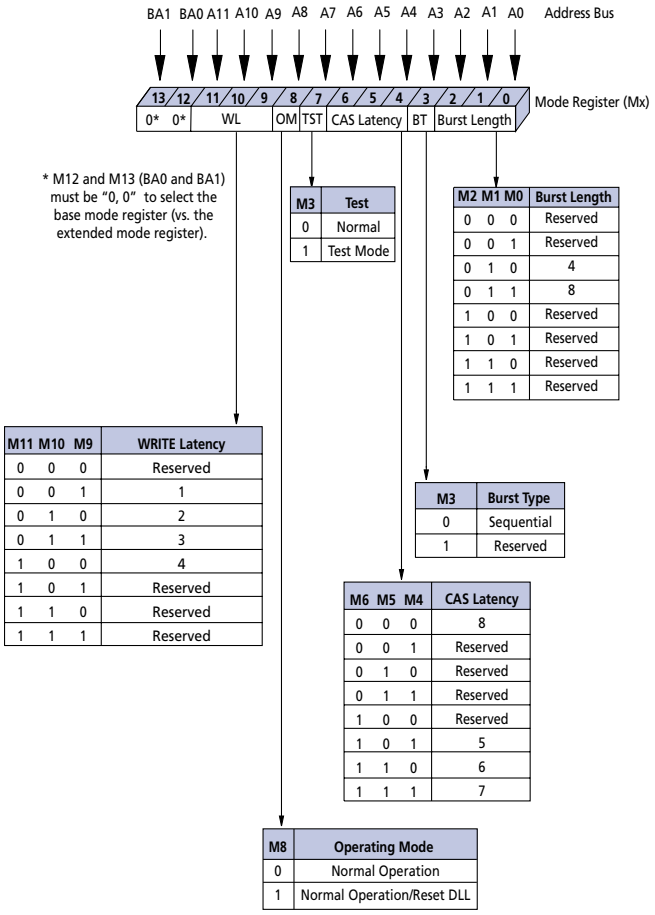
Once the 200µs delay has been satisfied, a DESELECT or NOP command should be applied, CKE should be brought HIGH, followed by a NOP command, and a PRECHARGE ALL command should be applied. Next, a LOAD MODE REGISTER command should be issued for the extended mode register (BA1 LOW and BA0 HIGH) to activate the DLL and set operating parameters, followed by a LOAD MODE REGISTER command (BA0/BA1 both LOW) to reset the DLL and to program the rest of the operating parameters. 200 clock cycles are required between the DLL reset and any READ command to allow the DLL to lock for Micron's device. The standard requires 20K clock cycles. A PRECHARGE ALL command should then be applied, placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed to update the driver impedance and calibrate the output drivers. Following these requirements, the GDDR3 SDRAM is ready for normal operation.

## Mode Register Definition

The mode register is used to define the specific mode of operation of the GDDR3 SDRAM. This definition includes the selection of a burst length, CAS latency, WRITE latency, and operating mode, as shown in Figure 4, Mode Register Definition, on page 11. The mode register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

## Figure 4: Mode Register Definition




## Table 4: Burst Definition

| BURST[1, 2] LENGTH | STARTING COLUMN ADDRESS | | | ORDER OF ACCESSES WITHIN A BURST |
|---|---|---|---|---|
| | | | | TYPE = SEQUENTIAL |
| 4 | | A1 | A0 | |
| | | 0 | 0 | 0-1-2-3 |
| 8 | A2 | A1 | A0 | |
| | 0 | 0 | 0 | 0-1-2-3-4-5-6-7 |
| | 1 | 0 | 0 | 4-5-6-7-0-1-2-3 |

NOTE:

1. For a burst length of four, A2–A7 select the block of four burst; A0–A1 select the starting column within the block and must be set to zero.
2. For a burst length of eight, A3–A7 select the of eight burst; A0–A2 select the starting column within the block.

Reprogramming the mode register will not alter the contents of the memory. The mode register must be loaded (reloaded) when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits M0–M2 specify the burst length; M3 specifies the type of burst (sequential); M4–M6 specify the CAS latency; M7 is a test mode; M8 specifies the operating mode; and M9–M11 specify the WRITE latency.

### Burst Length

Read and write accesses to the GDDR3 SDRAM are burst-oriented, with the burst length being programmable, as shown in Figure 4, Mode Register Definition. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 4 or 8 locations are available for the sequential burst type.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A2–A*i* when the burst length is set to four and by A3–A*i* when the burst length is set to eight (where A*i* is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

### Burst Type

Accesses within a given burst must be programmed to be sequential; this is referred to as the burst type and is selected via bit M3. This device does not support the interleaved burst mode found in DDR SDRAM devices.

The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table 4: Burst Definition.

### CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 5–8 clocks, as shown in Figure 5, CAS Latency, on page 12.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*. Table 6 indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

### Write Latency

The WRITE latency (WL) is the delay, in clock cycles, between the registration of a WRITE command and the availability of the first bit of input data as shown in Figure 6. The latency can be set from 1 to 4 clocks depending on the operating frequency and desired current draw. When the write latencies are set to 1 or 2 clocks, the input receivers never turn off, in turn, raising the operating power. When the WRITE latency is set to 3 or 4 clocks the input receivers turn on when the WRITE command is registered.

If a WRITE command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

### Table 5: CAS Latency

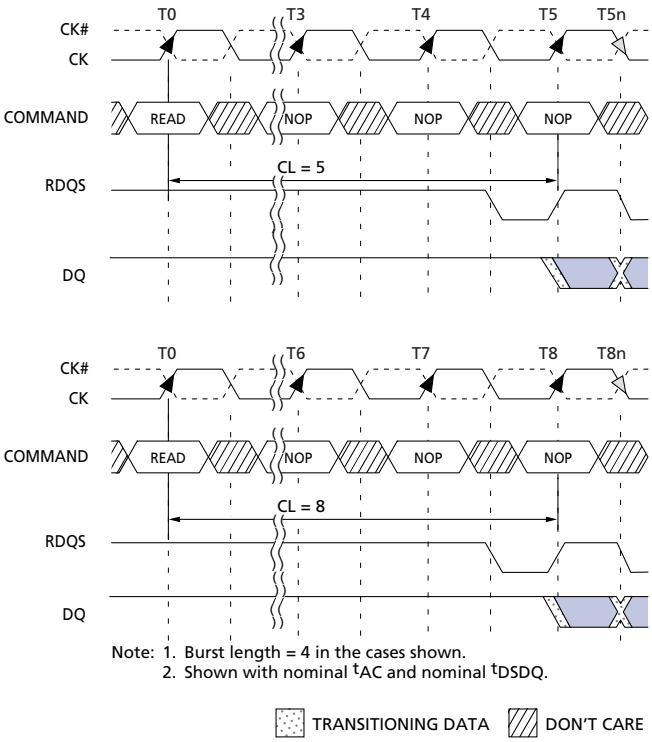
| | ALLOWABLE OPERATING FREQUENCY (MHZ) | | |
|---|---|---|---|
| SPEED | CL = 8 | CL = 7 | CL = 6 |
| -16 | ≤ 600 | ≤ 550 | ≤ 500 |
| -18 | - | ≤ 550 | ≤ 500 |
| -2 | - | - | ≤ 500 |

### Operating Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bit A8 set to zero, and bits M0–M6 and M9–M11 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bit A8 set to one, and bits M0–M7 and M9–M11 set to the desired values.

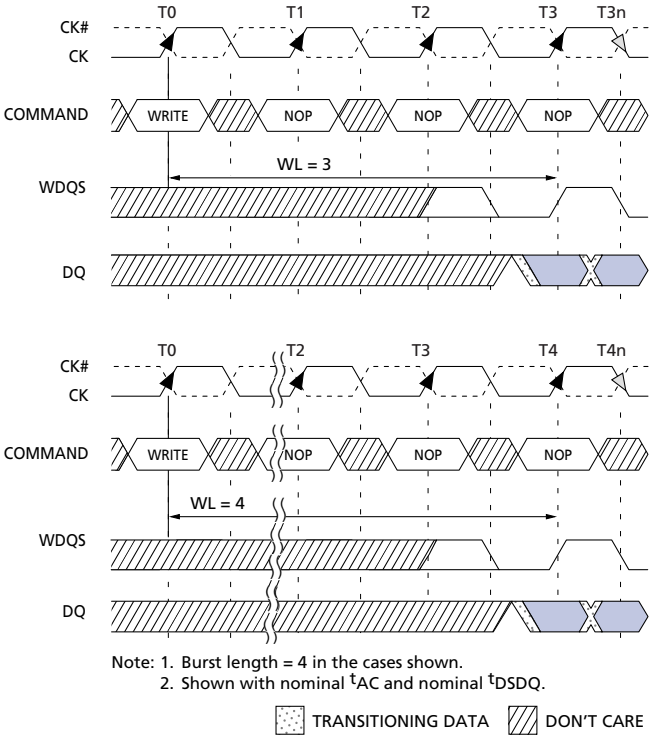
All other combinations of values for M7–M11 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

### Figure 5: CAS Latency



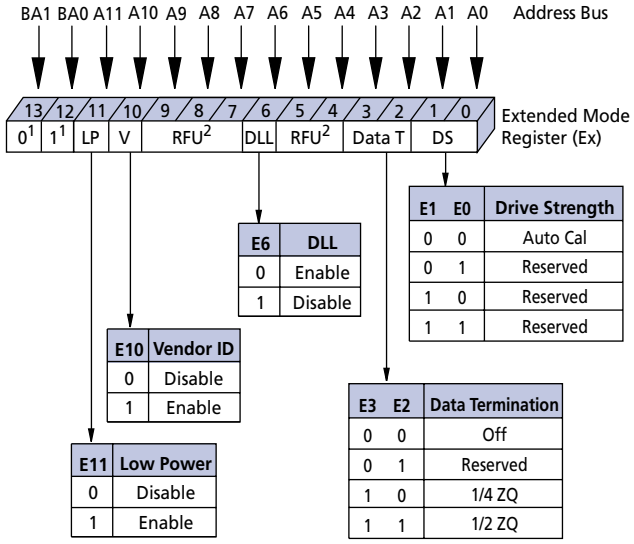

Note: 1. Burst length = 4 in the cases shown.
2. Shown with nominal $^{t}$AC and nominal $^{t}$DSDQ.

## Figure 6: WRITE Latency




Note: 1. Burst length = 4 in the cases shown.
2. Shown with nominal $^{t}$AC and nominal $^{t}$DSDQ.

## Figure 7: Extended Mode Register Definition




NOTE: 1. E12 and E13 (BA0 and BA1) must be "1, 0" to select the extended mode register (vs. the base mode register).
2. Reserved for future use. Set values to "0."

## Extended Mode Register

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, drive strength, data termination, vendor ID, and low-power mode. These functions are controlled via the bits shown in Figure 7, Extended Mode Register Definition. The extended mode register is programmed via the LOAD MODE REGISTER command to the mode register (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a LOAD MODE REGISTER command to the mode register (BA0/BA1 both LOW) to reset the DLL.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

## Programmable Impedance Output Buffer

The GDDR3 SDRAM uses a programmable impedance output buffer. This enables a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ pin and $V_{SS}$. The value of the resistor must be six times the desired driver impedance. For example, a 240Ω resistor is required for an output impedance of 40Ω. To ensure that output impedance is one-sixth the value of RQ (within 10 percent), the range of RQ is 210Ω to 270Ω (35Ω–45Ω output impedance). RES, CK and CK# are not internally terminated. CK and CK# need to be terminated on the system using external one percent resistors to $V_{DD}$ for the T2 version of the die. The T1 version of the die includes the on-die termination on CK and CK# and is set to the same value as the address and control pins.

The output impedance is updated during all AUTO REFRESH commands to compensate for variations in supply voltage and temperature. The output impedance updates are transparent to the system. Impedance updates do not affect device operation, and all data sheet timing and current specifications are met during an update.

The device will power up with an output impedance set at 40Ω. To guarantee optimum output driver impedance after power-up, the GDDR3 SDRAM needs 350 cycles after the clock is applied and stable to calibrate the impedance. The user can operate the part with fewer than 350 clock cycles, but optimal output impedance is not guaranteed.

### DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after disabling the DLL for debugging or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

### Low-Power Mode

The low-power mode is set through bit E11 in the extended mode register. When E11 = 1 during the EMRS command the GDDR3 power-down mode uses less power but takes more time to exit power-down. This mode of operation requires 10 clock cycles to exit power down in comparison to the four cycles needed during normal operation.

### Vendor ID

The vendor ID (V) is selected through bit E10 in the extended mode register. When bit E10 = 1 during an EMRS command the GDDR3 device will drive the vendor ID on DQ [0:3] and the die revision on DQ [4:7]. The ID code will start to drive *x* clocks, where *x* equals the set CAS latency plus two clocks, after the EMRS command is initiated through bit E10 and continue to drive the code until another EMRS command is issued with the E10 bit set to "0." After the E10 bit is set to "0," the DQ pins will stop driving *x* clock cycles after the EMRS command, where *x* equals burst length times two. The vendor ID for Micron is 0xF, and the die revision for the this device is 0xF.

### Data Termination

The data termination value is used to define the value for the on-die termination for the DQ, DM, and WDQS pins. The GDDR3 device supports one-quarter ZQ and one-half ZQ termination for a nominal 60Ω or 120Ω set with bit E3 and E2 during an EMRS command for a single- or dual-loaded system.

## Commands

Table 6 provides a quick reference of available commands, followed by a description of each command. Two additional truth tables appear following the Operation section; these tables provide current state/next state information.

### Table 6: Truth Table – Commands

Note: 1

| NAME (FUNCTION) | CS# | RAS# | CAS# | WE# | ADDR | NOTES |
|---|---|---|---|---|---|---|
| DESELECT (NOP) | H | X | X | X | X | 8 |
| NO OPERATION (NOP) | L | H | H | H | X | 8 |
| ACTIVE (Select bank and activate row) | L | L | H | H | Bank/Row | 3 |
| READ (Select bank and column, and start READ burst) | L | H | L | H | Bank/Col | 4 |
| WRITE (Select bank and column, and start WRITE burst) | L | H | L | L | Bank/Col | 4 |
| PRECHARGE (Deactivate row in bank or banks) | L | L | H | L | Code | 5 |
| AUTO REFRESH or SELF REFRESH (Enter self refresh mode) | L | L | L | H | X | 6, 7 |
| LOAD MODE REGISTER | L | L | L | L | Op-Code | 2 |
| DATA TERMINATOR DISABLE | X | H | L | H | X | 10 |

### Table 7: Truth Table 2 – DM Operation

| NAME (FUNCTION) | DM | DQS | NOTES |
|---|---|---|---|
| Write Enable | L | Valid | 9 |
| Write Inhibit | H | X | 9 |

NOTE:

1. CKE is HIGH for all commands shown except SELF REFRESH.
2. BA0–BA1 select either the mode register or the extended mode register (BA0 = 0, BA1 = 0 select the mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA0–BA1 are reserved). A0–A11 provide the op-code to be written to the selected mode register.
3. BA0–BA1 provide bank address and A0–A11provide row address.
4. BA0–BA1 provide bank address; A0–A7 and A9 provide column address; A8 HIGH enables the auto precharge feature (nonpersistent), and A8 LOW disables the auto precharge feature.
5. A8 LOW: BA0–BA1 determine which bank is precharged.
   A8 HIGH: all banks are precharged and BA0–BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. DESELECT and NOP are functionally interchangeable.
9. Used to mask write data; provided coincident with the corresponding data.
10. Used for bus snooping when the DQ termination is set to 120 ohms in the EMR and cannot be used during power-down or self refresh.

### DESELECT

The DESELECT function (CS# HIGH) prevents new commands from being executed by the GDDR3 SDRAM. The GDDR3 SDRAM is effectively deselected. Operations already in progress are not affected.

### NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected GDDR3 SDRAM to perform a NOP (CS# LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

### LOAD MODE REGISTER

The mode registers are loaded via inputs A0–A11. See mode register descriptions in the Register Definition section. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until $^{t}$MRD is met.

### ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A11 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

### READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A7, A9 selects the starting column location. The value on input A8 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

### WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A7, A9 selects the starting column location. The value on input A8 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored and a write will not be executed to that byte/column location.

### PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time ($^{t}$RP) after the precharge command is issued. Input A8 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise, BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging.

## Auto Precharge

Auto precharge is a feature that performs the same individual-bank precharge function described above but without requiring an explicit command. This is accomplished by using A8 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual Read or WRITE command.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This "earliest valid stage" is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating $^{t}RAS_{min}$, as described for each burst type in the Operation section of this data sheet. The user must not issue another command to the same bank until the precharge time ($^{t}RP$) is completed.

## AUTO REFRESH

AUTO REFRESH is used during normal operation of the GDDR3 SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) refresh in FPM/EDO DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an AUTO REFRESH command. The 256Mb x32 GDDR3 SDRAM requires AUTO REFRESH cycles at an average interval of 7.8µs (maximum).

A maximum of eight AUTO REFRESH commands can be posted to any given GDDR3 SDRAM, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 9 x 7.8µs (70.2µs). This maximum absolute interval allows GDDR3 SDRAM output drivers to automatically recalibrate to compensate for voltage and temperature changes.

## SELF REFRESH

The SELF REFRESH command can be used to retain data in the GDDR3 SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the GDDR3 SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH and is automatically enabled and reset upon exiting SELF REFRESH. The on-die termination is also disabled upon entering SELF REFRESH except for CKE and enabled upon exiting SELF REFRESH. (Two hundred clock cycles must then occur before a READ command can be issued.) Input signals except CKE are "Don't Care" during SELF REFRESH.

The procedure for exiting self refresh requires a sequence of commands. First, CK and CK# must be stable prior to CKE going back HIGH. Once CKE is HIGH, the GDDR3 SDRAM must have NOP commands issued for $^{t}XSNR$ because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements and output calibration is to apply NOPs for 200 clock cycles before applying any other command to allow the DLL to lock and the output drivers to recalibrate.

If the GDDR3 device enters SELF REFRESH with the DLL disabled the GDDR3 device will exit SELF REFRESH with the DLL disabled.

## On Die Termination

Bus snooping for READ commands other than CS# is used to control the on-die termination in the dual load configuration. The GDDR3 SDRAM will disable the on-die termination when a READ command is detected, regardless of the state of CS#, when the ODT for the DQ pins are set for dual loads (120Ω).The on-die termination is disabled *x* clocks after the READ command where *x* equals CL - 1 and stay off for a duration of BL + 2, as shown in Figure 8, Data Termination Disable Timing, on page 19. In a two-rank system, both DRAM devices snoop the bus for READ commands to either device and both will disable the on-die termination if a READ command is detected. The on-die termination for all other pins on the device are always on for both a single-rank system and a dual-rank system.

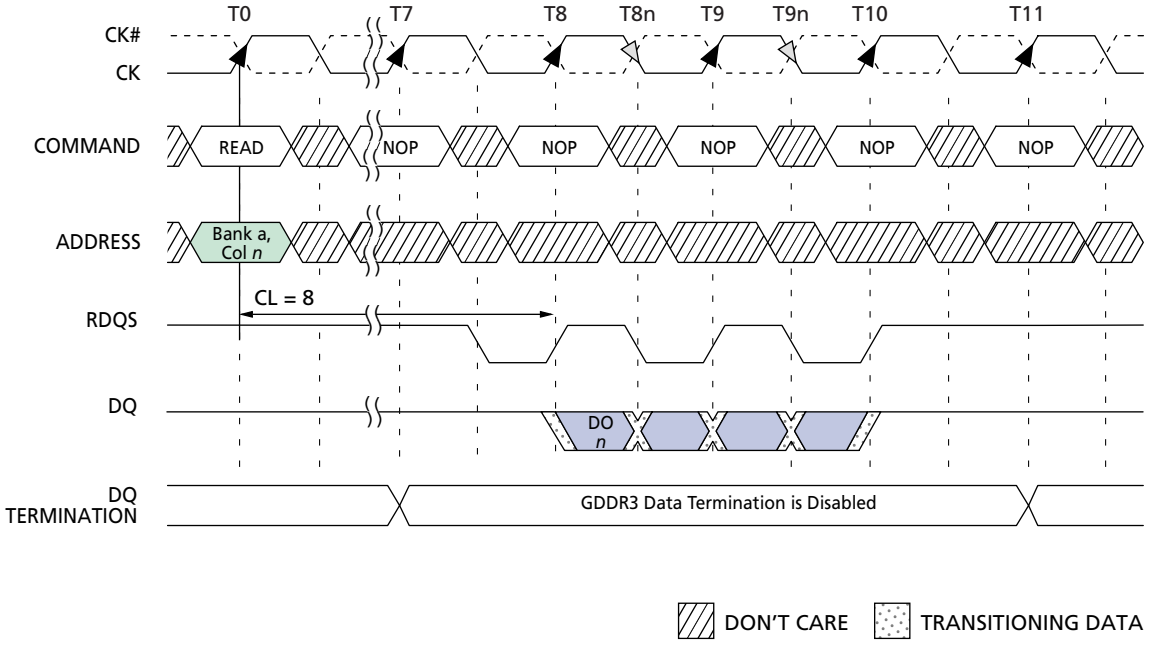
The on-die termination value on address and control pins is determined during power-up in relation to the state of CKE on the first transition of RES. On the rising edge of RES, if CKE is sampled LOW, then the configuration is determined to be a single-rank system. The on-die termination is then set to one-half ZQ for the address pins. On the rising edge of RES, if CKE is sampled HIGH, then the configuration is determined to be a dual-bank system. The T1 version of the die also sets the on-die termination to the CK and CK# pins at this time to the same value as the address and control pins. The on-die termination is then set to ZQ for the address pins. The on-die termination for the DQs, WDQS, and DM pins is set in the EMR.

## Mirror Function

The GDDR3 SDRAM provides a mirror function (MF) ball to change the physical location of the control lines and all address lines assisting in routing devices back to back. The MF ball will affect RAS#, CAS#, WE#, CS#, and CKE on balls G1, F2, G10, F10, and G2, respectively and A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, BA0, and BA1 on balls J4, H2, J3, H1, J8, H10, J9, J11, J10, H11, J2, J1, F1, and F11, respectively, and will only detect a DC input. The MF ball should be tied directly to VSS or VDD, depending on the control line orientation desired. The mirror function is only supported on the 135-ball package.

When the MF ball is tied LOW, the ball orientation is as follows: RAS# - G1, CAS# - F2, WE# - G10, CS# - F10, CKE - G2, A0 - J4, A1 - H2, A2 - J3, A3 - H1, A4 - J8, A5 - H10, A6 - J9, A7 - J11, A8 - J10, A9 - H11, A10 - J2, A11 - J1, BA0 - F1, and BA1 - F11. The high condition on the MF ball will change the location of the control balls as follows: RAS# - G11, CAS# - F10, WE# - G2, CS# - F2, CKE - G10, A0 - J8, A1- H10, A2 - J9, A3 - H11, A4 - J4, A5 - H2, A6 - J3, A7 - J1, A8 - J2, A9 - H1, A10 - J10, A11 - J11, BA0 - F11, and BA1 - F1.

**Figure 8: Data Termination Disable Timing**




NOTE:

1. DO *n* = data-out from column *n*.
2. Burst length = 4.
3. Three subsequent elements of data-out appear in the specified order following DO *n*.
4. Shown with nominal $^{t}$AC and $^{t}$DQSQ.
5. RDQS will start driving high one-half clock cycle prior to the first falling edge.
6. The Data Terminators are disabled starting at CL - 1 and the duration is BL + 2.
7. READS to either rank disable both ranks' termination regardless of the logic level of CS#.

## Operations

### *Bank/Row Activation*

Before any READ or WRITE commands can be issued to a bank within the GDDR3 device, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated, as shown in Figure 9, Activating a Specific Row in a Specific Bank.

After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the $^{t}$RCD specification. $^{t}RCD_{MIN}$ should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a $^{t}$RCD specification of 16ns with a 450 MHz clock (2.2ns period) results in 7.2 clocks rounded to 8. This is reflected in Figure 10, Example: Meeting $^{t}$RCD, which covers any case where $7 < {}^{t}RCD_{MIN}/{}^{t}CK \leq 8$. The same procedure is used to convert other specification limits from time units to clock cycles).

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by $^{t}$RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by $^{t}$RRD.

**Figure 9: Activating a Specific Row in a Specific Bank**

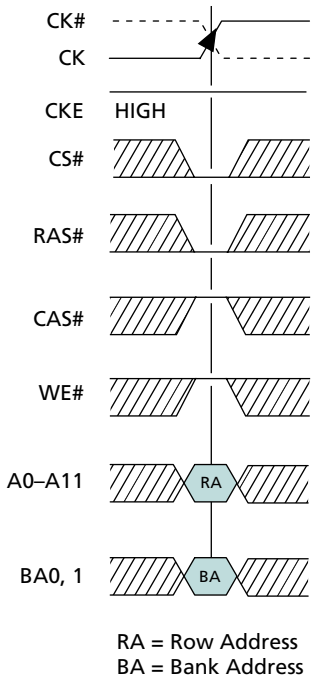
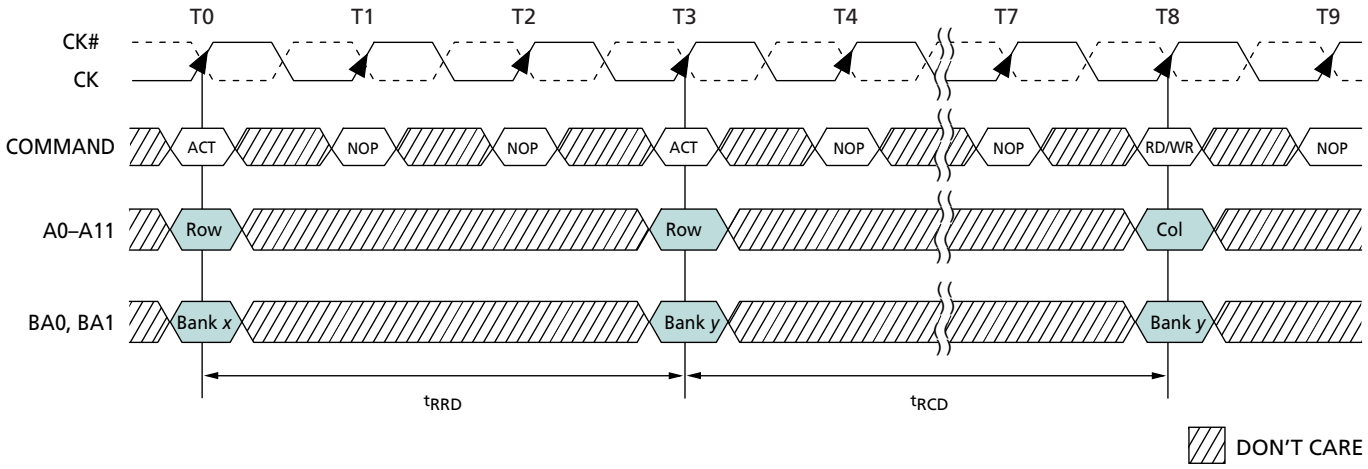



**Figure 10: Example: Meeting $^{t}$RCD**



## READS

READ bursts are initiated with a READ command, as shown in Figure 11.

The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst after $^{t}RAS_{MIN}$ has been met. For the generic READ commands used in the following illustrations, auto precharge is disabled.

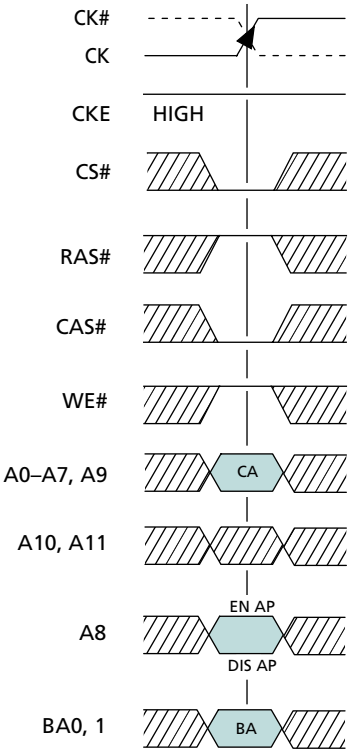
During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative strobe edges. Figure 12, shows general timing for two of the possible CAS latency settings. The GDDR3 SDRAM drives the output data edge-aligned to the crossing of CK and CK# and to RDQS. The initial HIGH transitioning LOW of RDQS is known as the read preamble; the half cycle coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go to $V_{DD}$ do to the on-die termination. A detailed explanation of $^{t}DQSQ$ (valid data-out skew), $^{t}DV$ (data-out window hold), and the valid data window are shown in Figure 38. A detailed explanation of $^{t}AC$ (DQS and DQ transition skew to CK) is shown in Figure 39 on page 56.

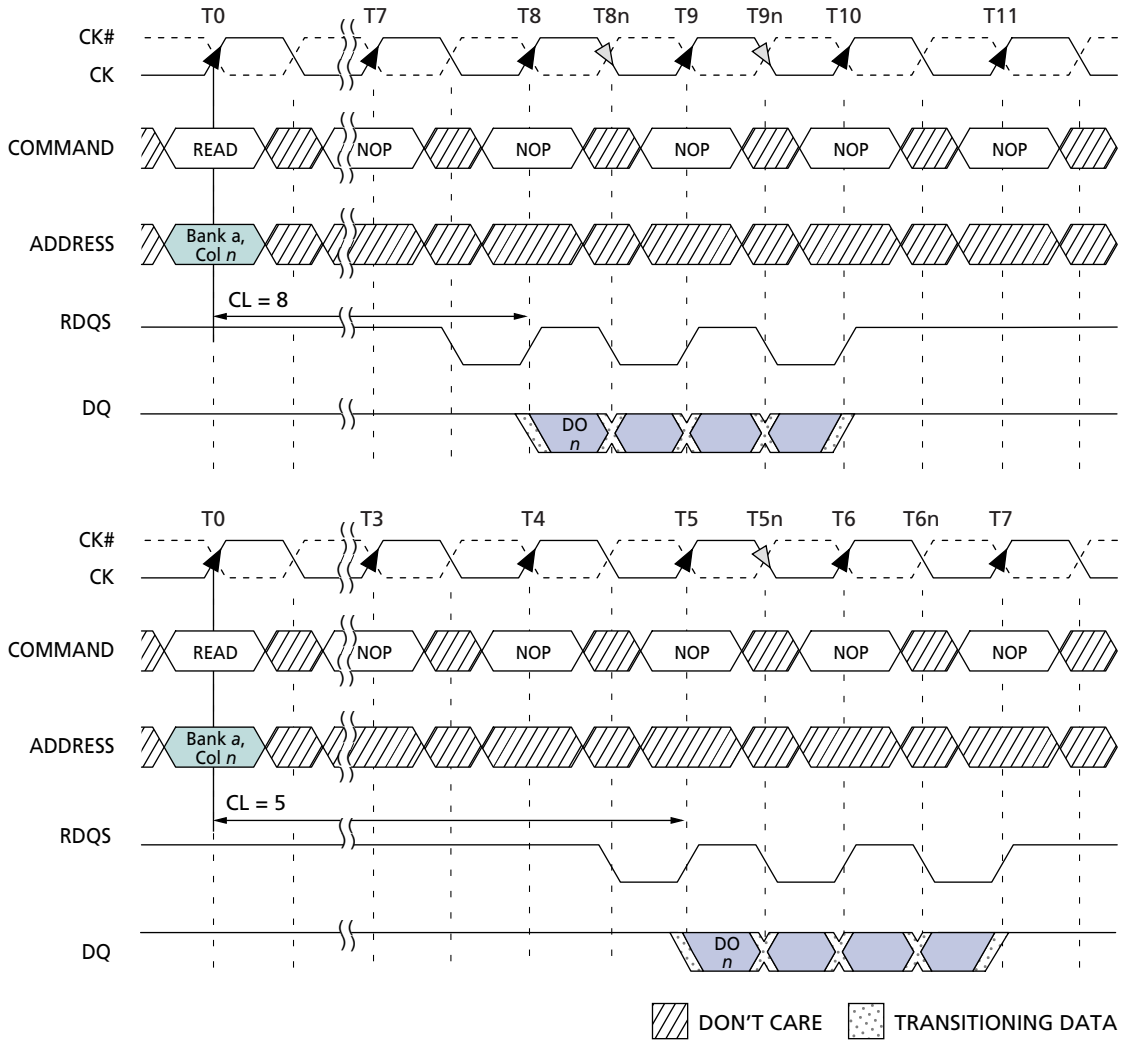
Data from any READ burst may be concatenated with data from a subsequent READ command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued $x$ cycles after the first READ command, where $x$ equals $2x$ the number of data element nibbles (nibbles are required by the $4n$-prefetch architecture) depending on the burst length. This is shown in Figure 13, Consecutive READ Bursts, on page 23. Non-consecutive read data is shown in Figure 14. Full-speed, random read accesses within a page (or pages) can be performed as shown in Figure 15, Random Read Accesses, on page 25. Data from a READ burst cannot be terminated or truncated.

During READ commands the GDDR3 SDRAM disables its on-die termination when data is valid on the bus.

**Figure 11: READ Command**



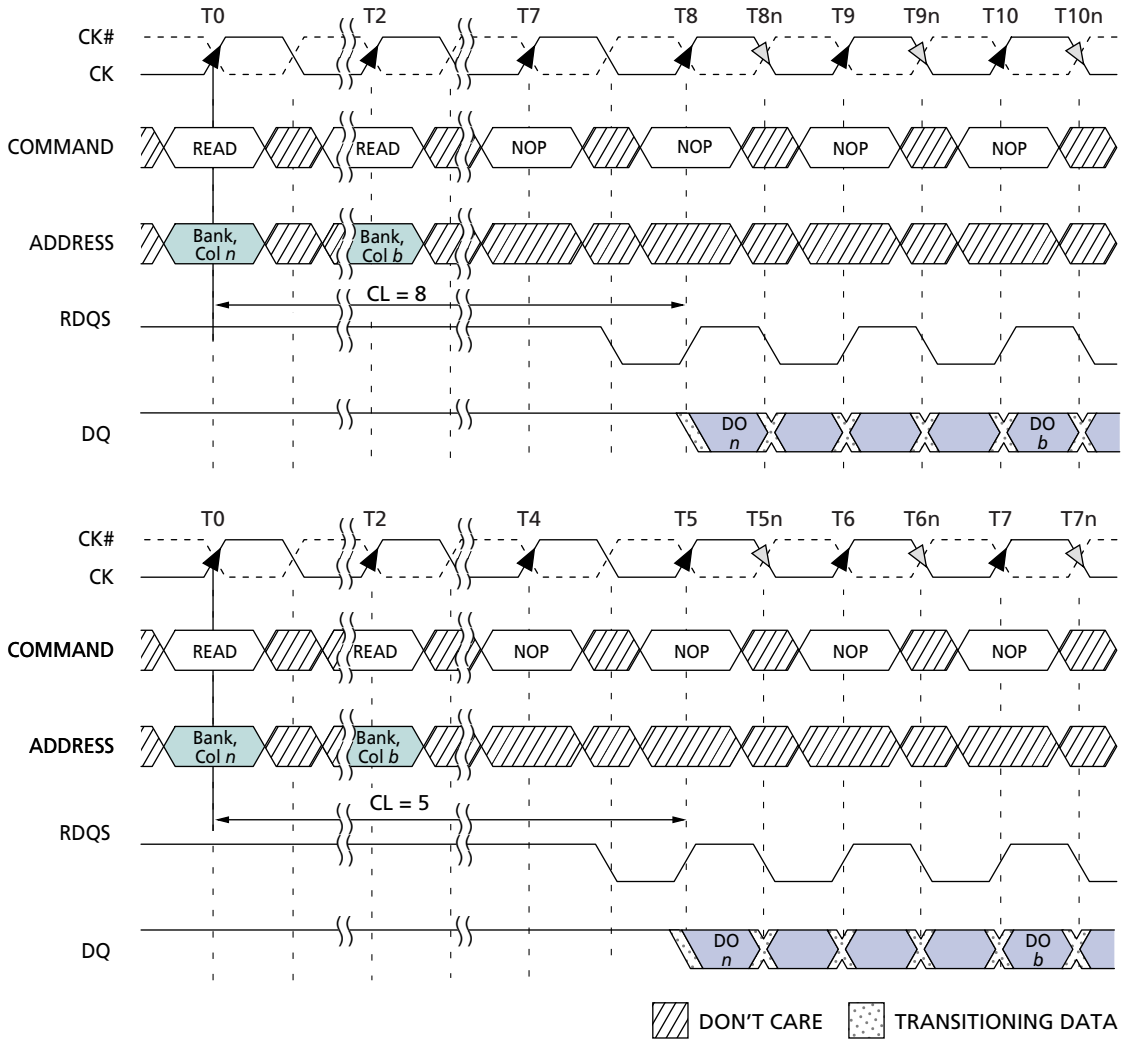
## Figure 12: READ Burst




NOTE:

1. DO *n* = data-out from column *n*.
2. Burst length = 4.
3. Three subsequent elements of data-out appear in the specified order following DO *n*.
4. Shown with nominal $^{t}$AC and $^{t}$DQSQ.
5. RDQS will start driving high one-half clock cycle prior to the first falling edge.

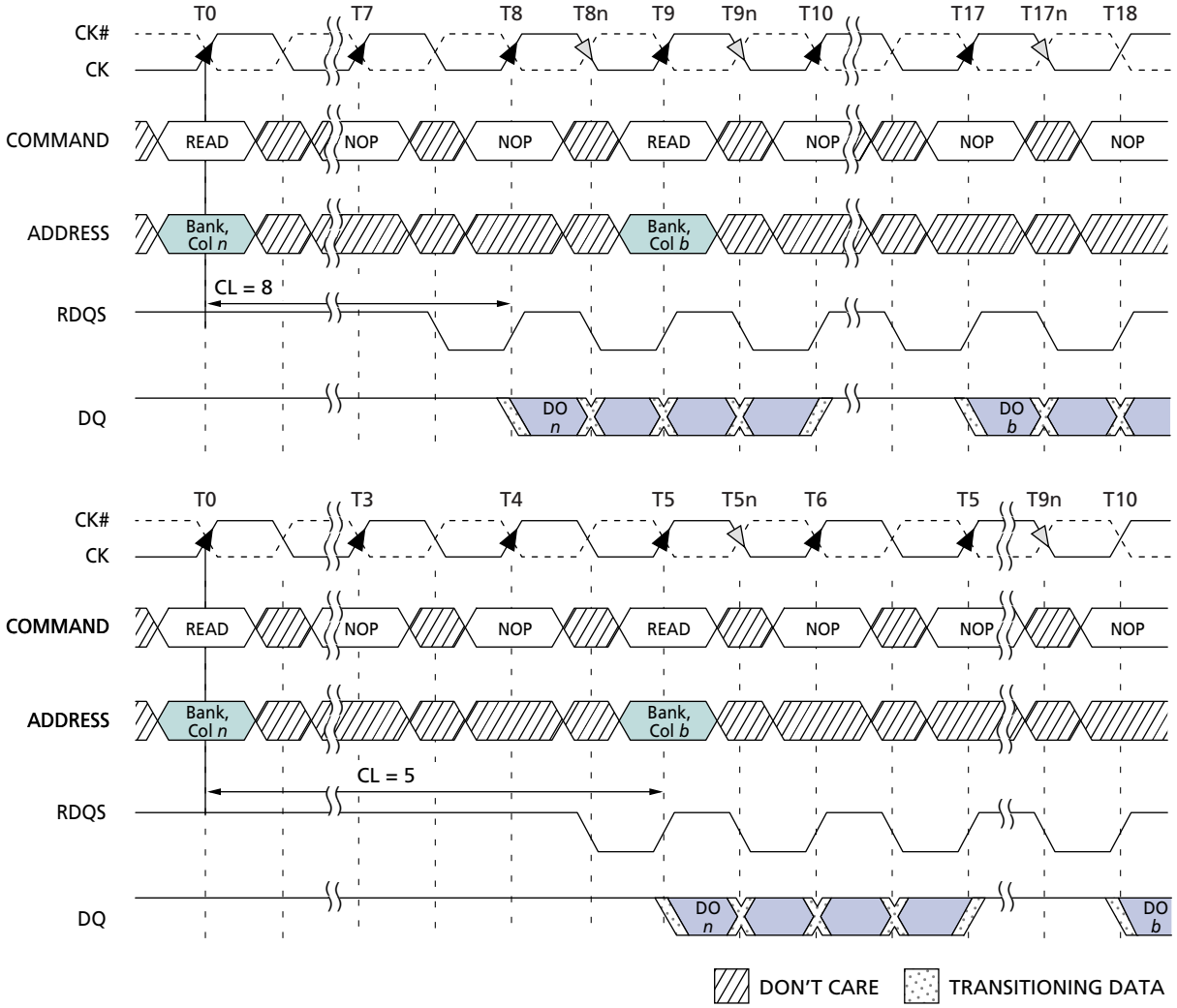
## Figure 13: Consecutive READ Bursts




NOTE:

1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. Burst length = 4
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Three subsequent elements of data-out appear in the programmed order following DO *b*.
5. Shown with nominal $^{t}$AC, and $^{t}$DQSQ.
6. Example applies only when READ commands are issued to same device.
7. RDQS will start driving high one half clock cycle prior to the first falling edge of RDQS.

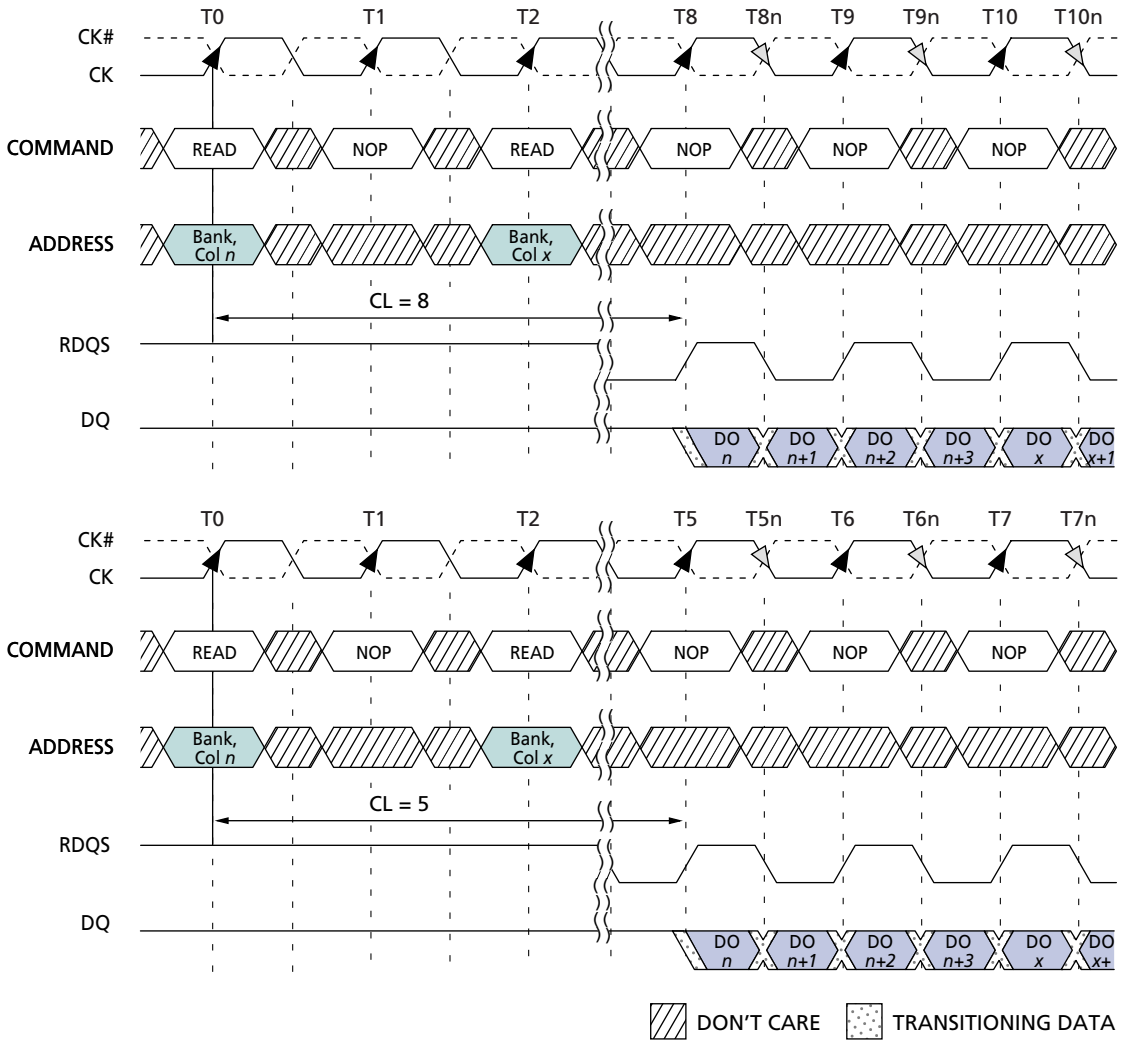
## Figure 14: Non-Consecutive READ Bursts




NOTE:

1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. Burst length = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Three subsequent elements of data-out appear in the programmed order following DO *b*.
5. Shown with nominal $^{t}$AC and $^{t}$DQSQ.
6. Example applies when READ commands are issued to different devices or nonconsecutive READs.
7. RDQS will start driving high one-half clock cycle prior to the first falling edge of RDQS.

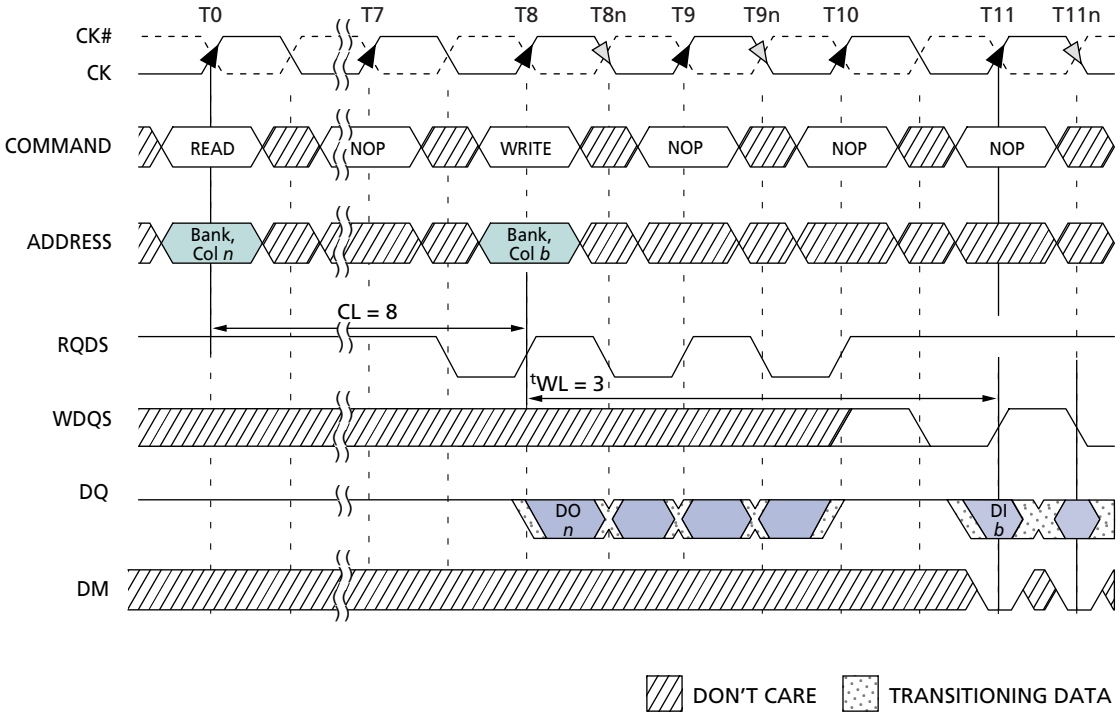
## Figure 15: Random Read Accesses




NOTE:

1. DO *n* (or *x* or *b* or *g*) = data-out from column *n* (or column *x* or column *b* or column *g*).
2. Burst length = 4.
3. READs are to an active row in any bank.
4. Shown with nominal $^{t}$AC and $^{t}$DQSQ.
5. RDQS will start driving high one-half clock cycle prior to the first falling edge of RDQS.

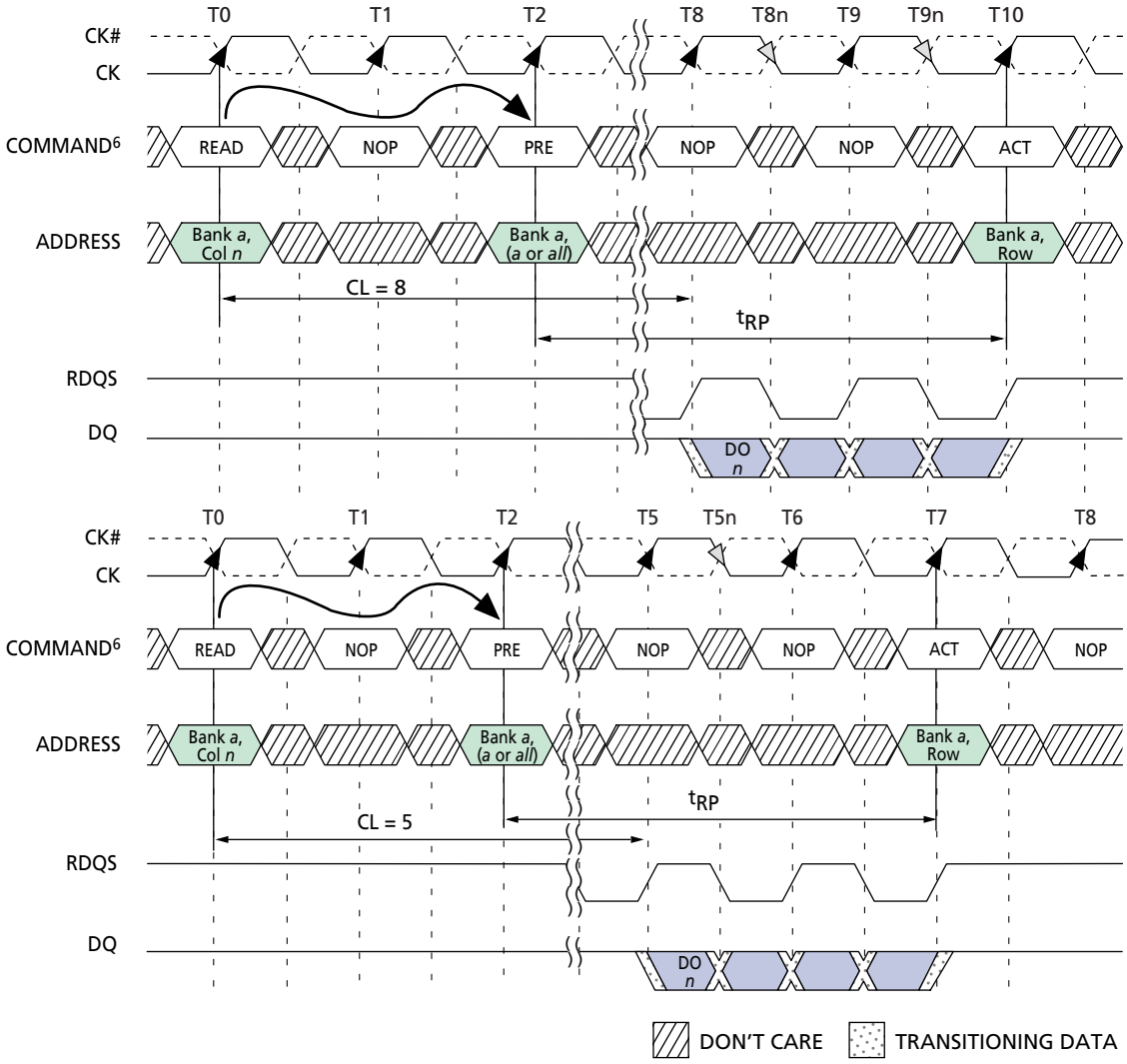
## Figure 16: READ to WRITE




NOTE:

1. DO *n* = data-out from column *n*.
2. DI *b* = data-in from column *b*.
3. Burst length = 4.
4. Three subsequent elements of data-out appear in the programmed order following DO *n*.
5. Data-in elements are applied following DI *b* in the programmed order.
6. Shown with nominal $^{t}$AC and $^{t}$DQSQ.
7. $^{t}$DQSS in nominal case.
8. RDQS will start driving HIGH one-half clock cycle prior to the first falling edge of RDQS.

## Figure 17: READ to PRECHARGE




NOTE:

1. DO *n* = data-out from column *n*.
2. Burst length = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Shown with nominal $^{t}$AC and $^{t}$DQSQ.
5. READ to PRECHARGE equals two clocks, which enables two data pairs of data-out.
6. PRE = PRECHARGE command; ACT = ACTIVE command.
7. RDQS will start driving HIGH one-half clock cycle prior to the first falling edge of RDQS.

## WRITEs

WRITE bursts are initiated with a WRITE command, as shown in Figure 18, WRITE Command.

The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered on a rising edge of WDQS following the write latency set in the mode register, and subsequent data elements will be registered on successive edges of WDQS. Prior to the first valid WDQS edge, a half cycle is needed and specified as the WRITE preamble. There cannot be a LOW-to-HIGH transition in the half cycle before the preamble; the half cycle on WDQS following the last data-in element is known as the write postamble and must be driven HIGH by the controller. It cannot be left to float HIGH using the on-die termination.

The time between the WRITE command and the first valid edge of WDQS ($^{t}$DQSS) is specified relative to the write latency (WL - 0.25CK and WL + 0.25CK). All of the WRITE diagrams show the nominal case, and where the two extreme cases (i.e., $^{t}DQSS_{MIN}$ and $^{t}DQSS_{MAX}$) might not be intuitive, they have also been included. Figure 19, WRITE Burst, shows the nominal case and the extremes of $^{t}$DQSS for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs terminate and any additional input data will be ignored.

Data for any WRITE burst cannot be truncated with a subsequent WRITE command. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command, assuming the previous burst has completed. The new WRITE command should be issued *x* cycles after the first WRITE command, where *x* equals the number of desired nibbles x2 (nibbles are required by 4*n*-prefetch architecture).

An example of nonconsecutive WRITEs is shown in Figure 21 on page 31. Full-speed, random write accesses within a page or pages can be performed as shown in Figure 22 on page 32.

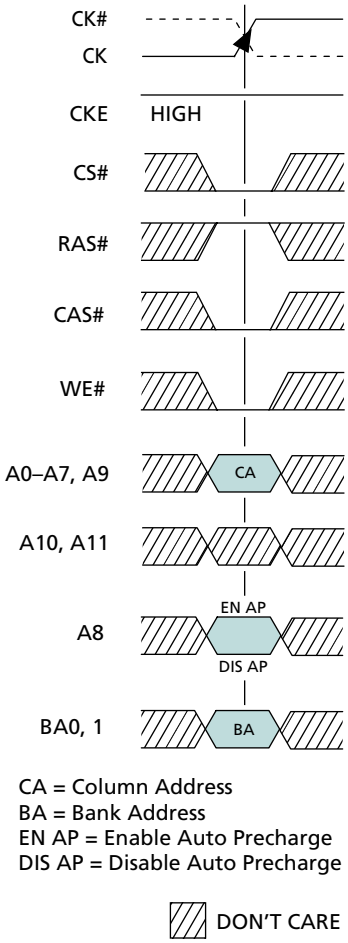
Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE, $^{t}$WTR should be met as shown in Figure 23, WRITE to READ, on page 33.

Data for any WRITE burst cannot be truncated by a subsequent READ command.

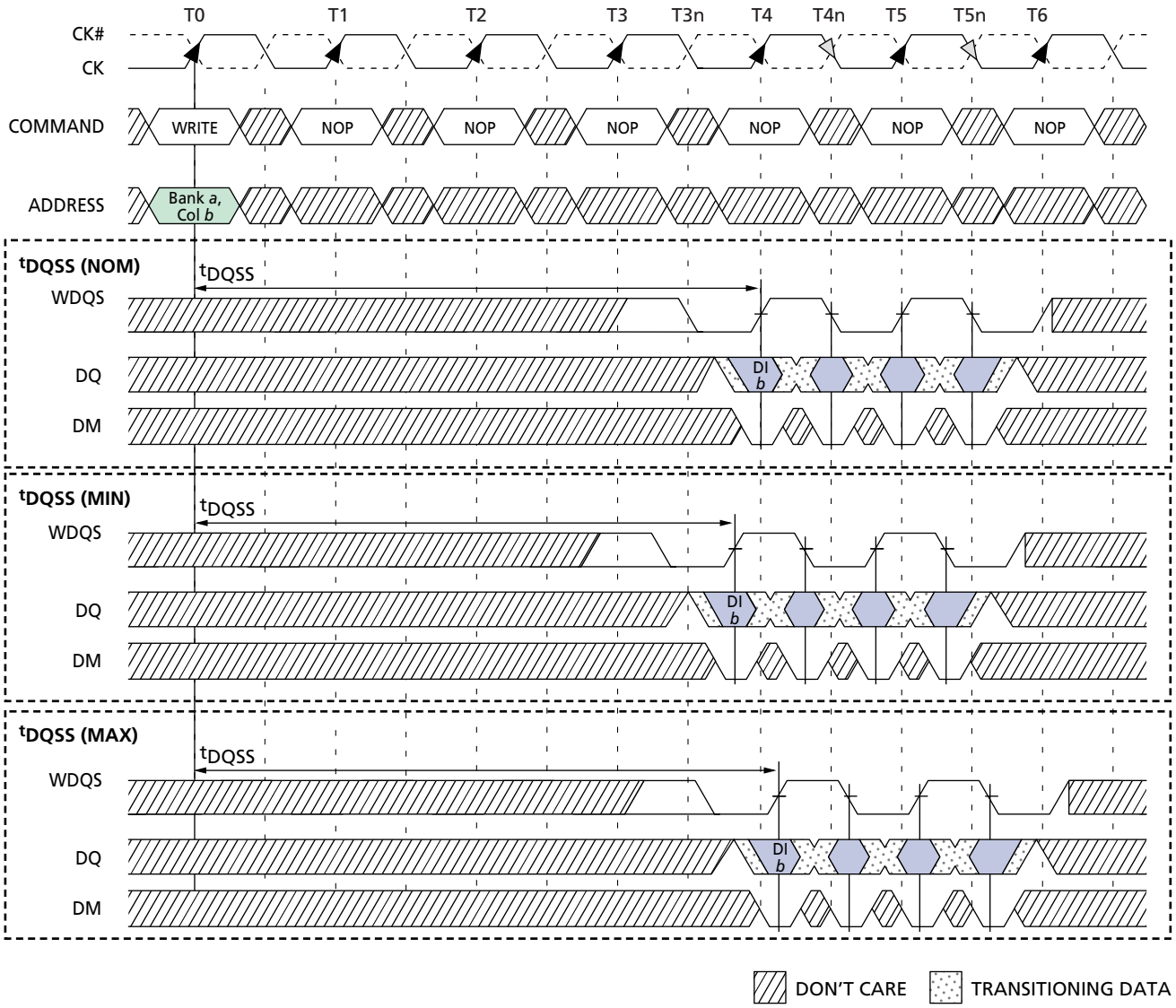
Data for any WRITE burst may be followed by a subsequent PRECHARGE command, but $^{t}$WR needs to be met as shown in Figure 26, WRITE to PRECHARGE, on page 36.

Data for any WRITE burst cannot be truncated by a subsequent PRECHARGE command. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until $^{t}$RP is met.

**Figure 18: WRITE Command**



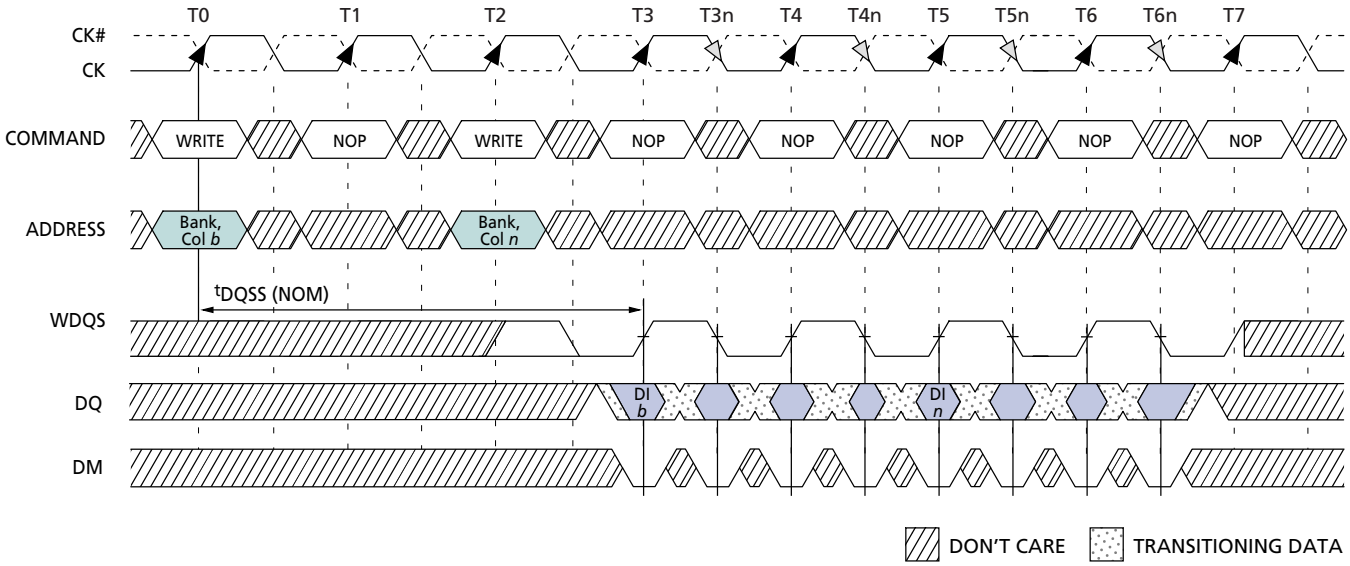
## Figure 19: WRITE Burst




NOTE:

1. DI *b* = data-in for column *b*.
2. Three subsequent elements of data-in are applied in the specified order following DI *b*.
3. A burst of 4 is shown.
4. A8 is LOW with the WRITE command (auto precharge is disabled).
5. Write latency is set to 4.

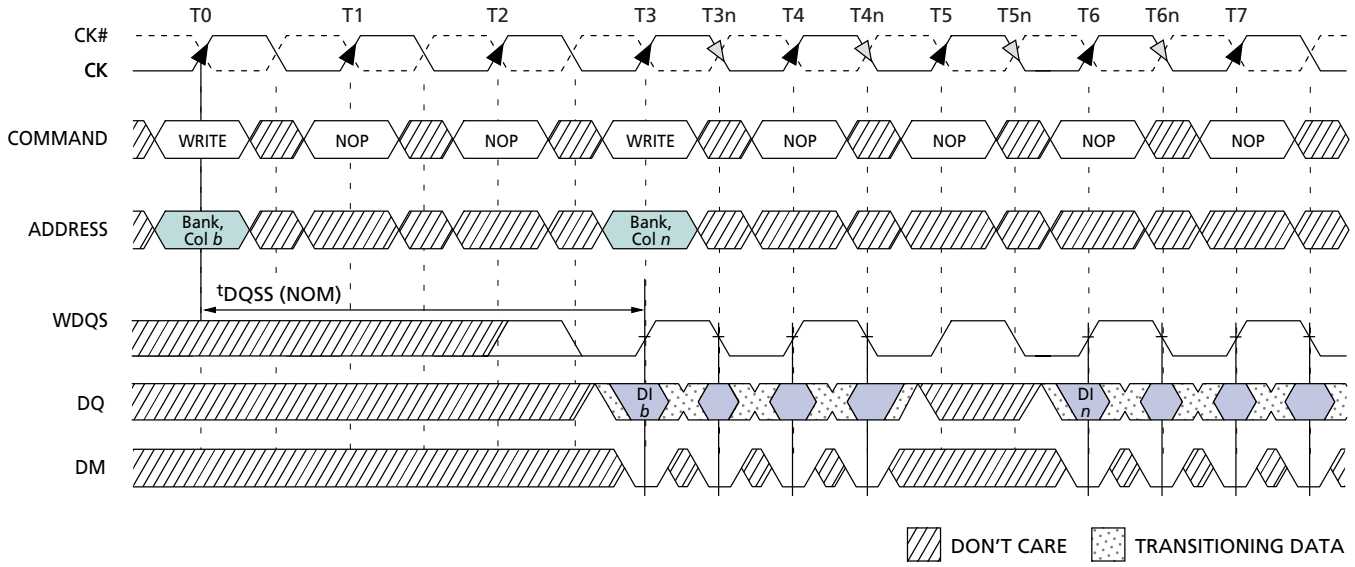
## Figure 20: Consecutive WRITE to WRITE




NOTE:

1. DI *b*, etc. = data-in for column *b*, etc.
2. Three subsequent elements of data-in are applied in the specified order following DI *b*.
3. Three subsequent elements of data-in are applied in the specified order following DI *n*.
4. Burst of 4 is shown.
5. Each WRITE command may be to any bank of the same device.
6. WRITE latency is set to 3.

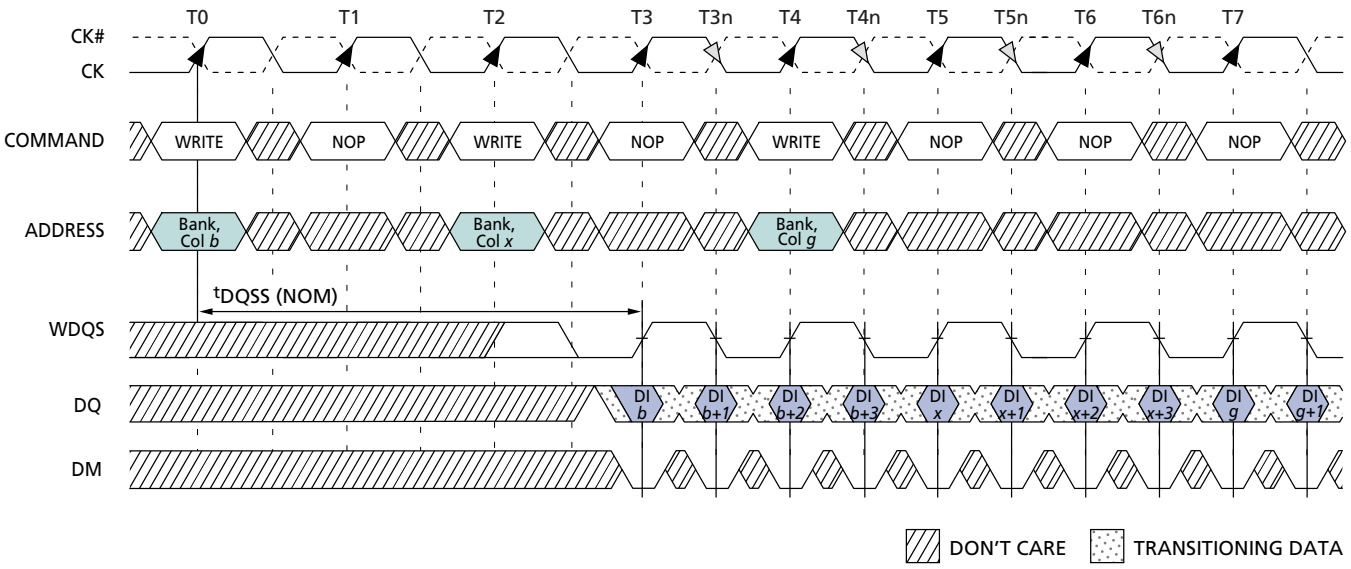
## Figure 21: Nonconsecutive WRITE to WRITE




NOTE:

1. DI *b*, etc. = data-in for column *b*, etc.
2. Three subsequent elements of data-in are applied in the specified order following DI *b*.
3. Three subsequent elements of data-in are applied in the specified order following DI *n*.
4. A burst of 4 is shown.
5. Each WRITE command may be to any bank.
6. WRITE latency set to 3.

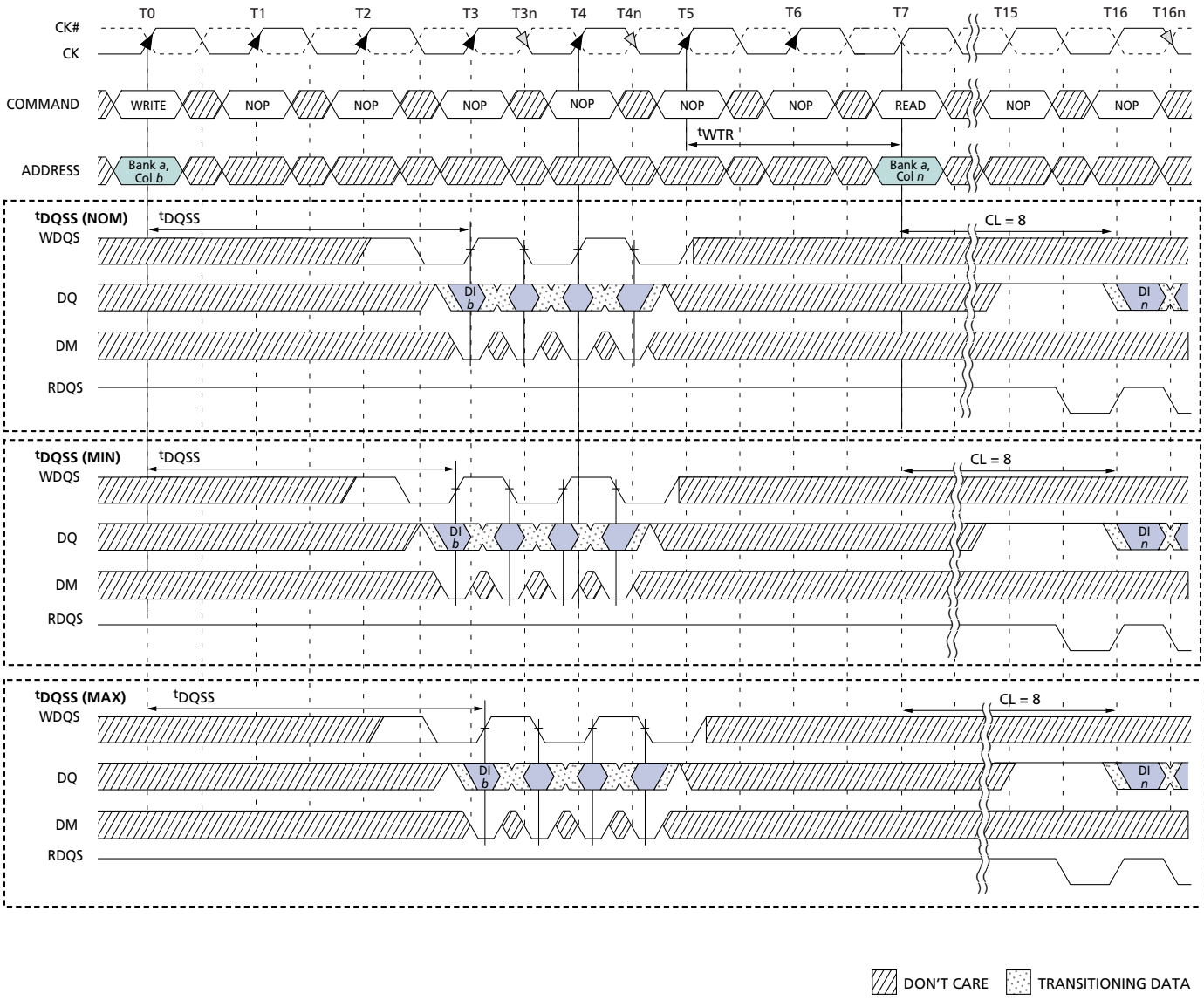
## Figure 22: Random WRITE Cycles




NOTE:

1. DI *b*, etc. = data-in for column *b*, etc.
2. *b*', etc. = the next data-in following DI *b*, etc., according to the specified burst order.
3. Programmed burst length = 4 cases shown.
4. Each WRITE command may be to any bank.
5. Last write command will have the rest of the nibble on T8 and T8*n*.
6. WRITE latency is set to 3.

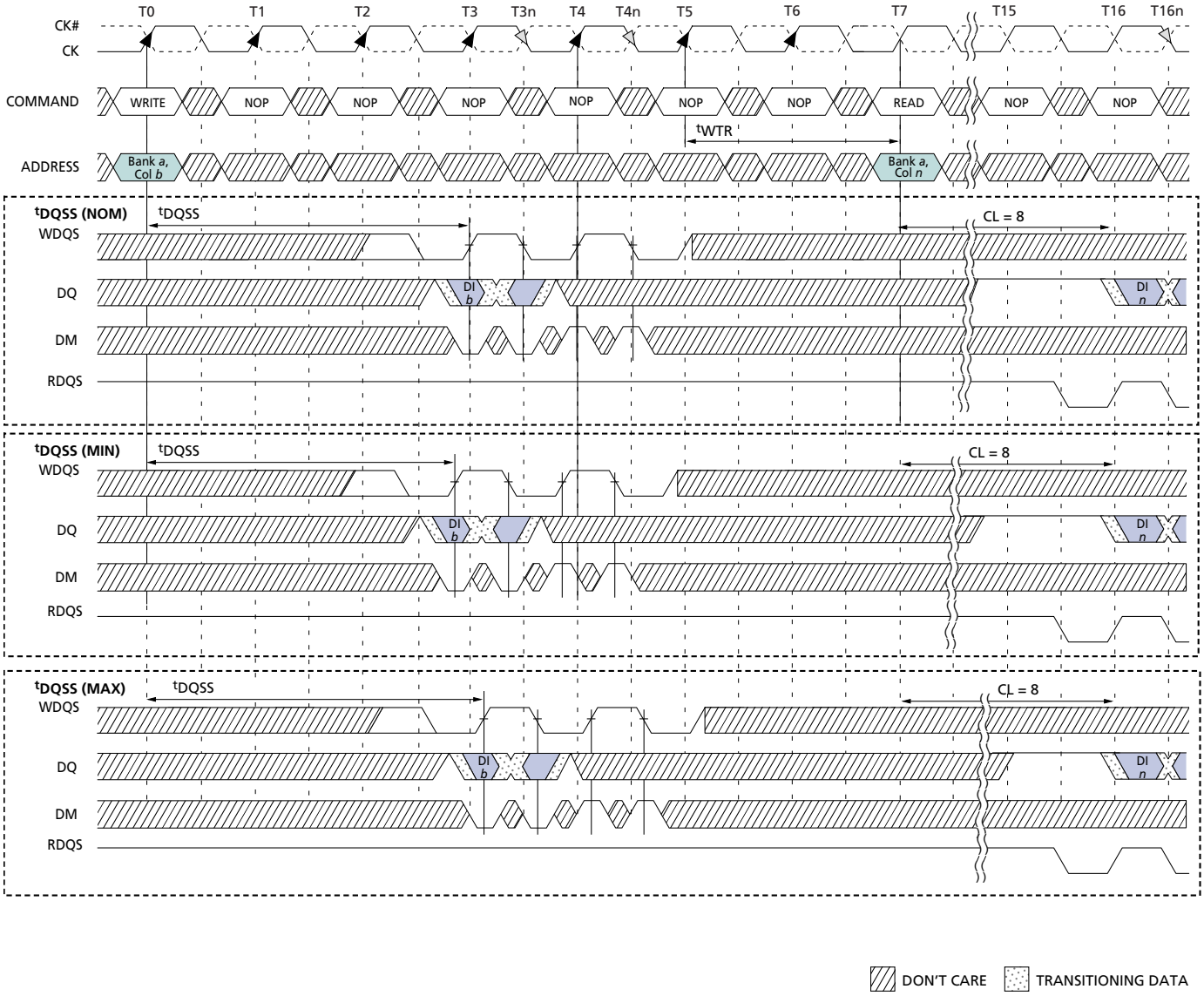
## Figure 23: WRITE to READ




NOTE:

1. DI *b* = data-in for column *b*.
2. Three subsequent elements of data-in are applied in the specified order following DI *b*.
3. A burst of 4 is shown.
4. $^{t}$WTR is referenced from the first positive CK edge after the last nibble.
5. The READ and WRITE commands are to the same device. However, the READ and WRITE commands may be to different devices, in which case, $^{t}$WTR is not required and the READ command could be applied earlier.
6. A8 is LOW with the WRITE command (auto precharge is disabled).
7. WRITE latency is set to 3.
8. The 4*n* prefetch architecture requires a 2-clock WRITE-to-READ turnaround time ($^{t}$WTR).

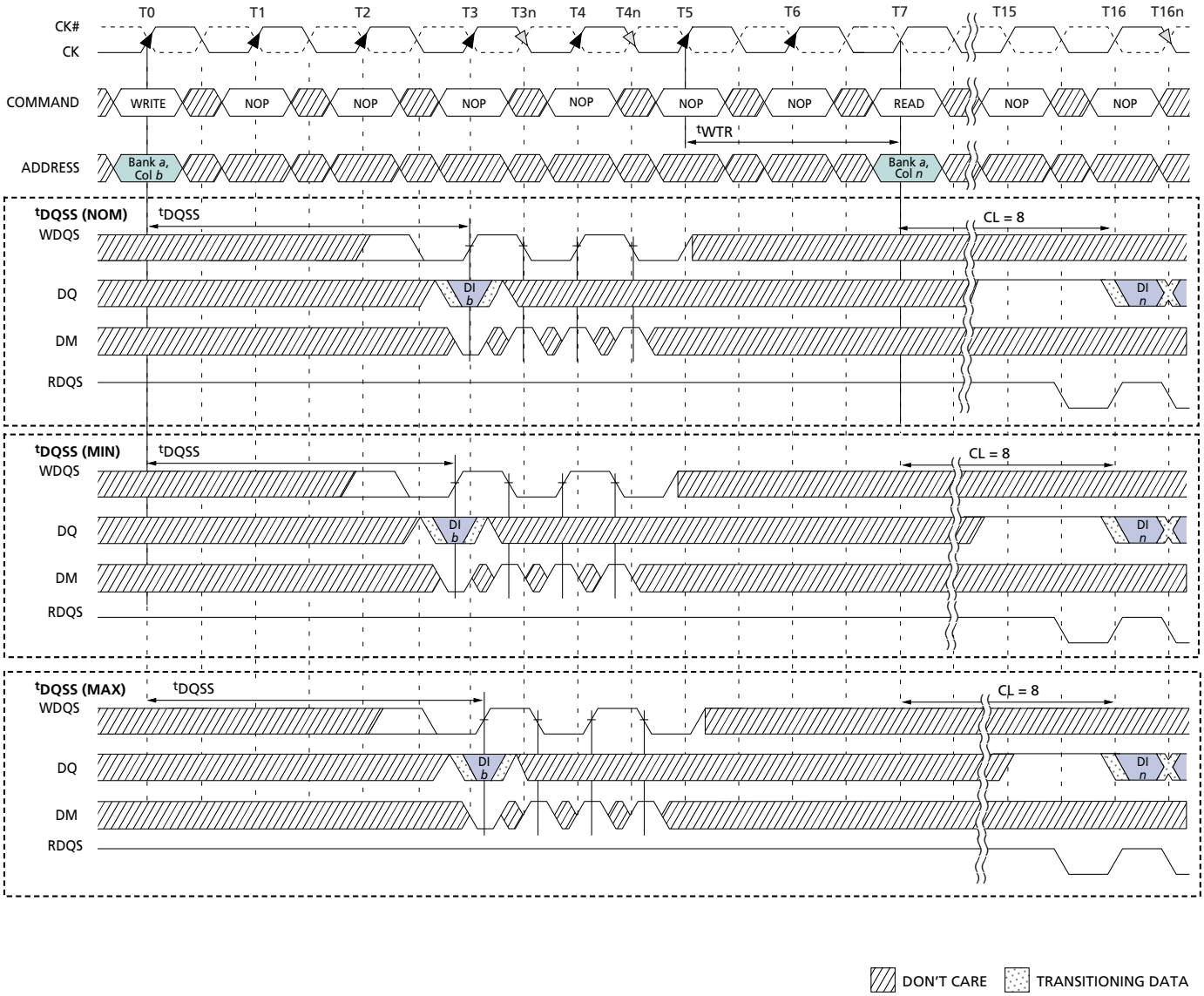
## Figure 24: WRITE to READ with Data Masking




NOTE:

1. DI *b* = data-in for column *b*.
2. One subsequent elements of data-in is applied in the specified order following DI *b*.
3. A burst of 4 is shown.
4. $^{t}$WTR is referenced from the first positive CK edge after the last nibble (as if the whole nibble is being written).
5. The READ and WRITE commands are to the same device. However, the READ and WRITE commands may be to different devices, in which case, $^{t}$WTR is not required and the READ command could be applied earlier.
6. A8 is LOW with the WRITE command (auto precharge is disabled).
7. WRITE latency is set to 3.
8. The 4*n* prefetch architecture requires a 2-clock WRITE-to-READ turnaround time ($^{t}$WTR).

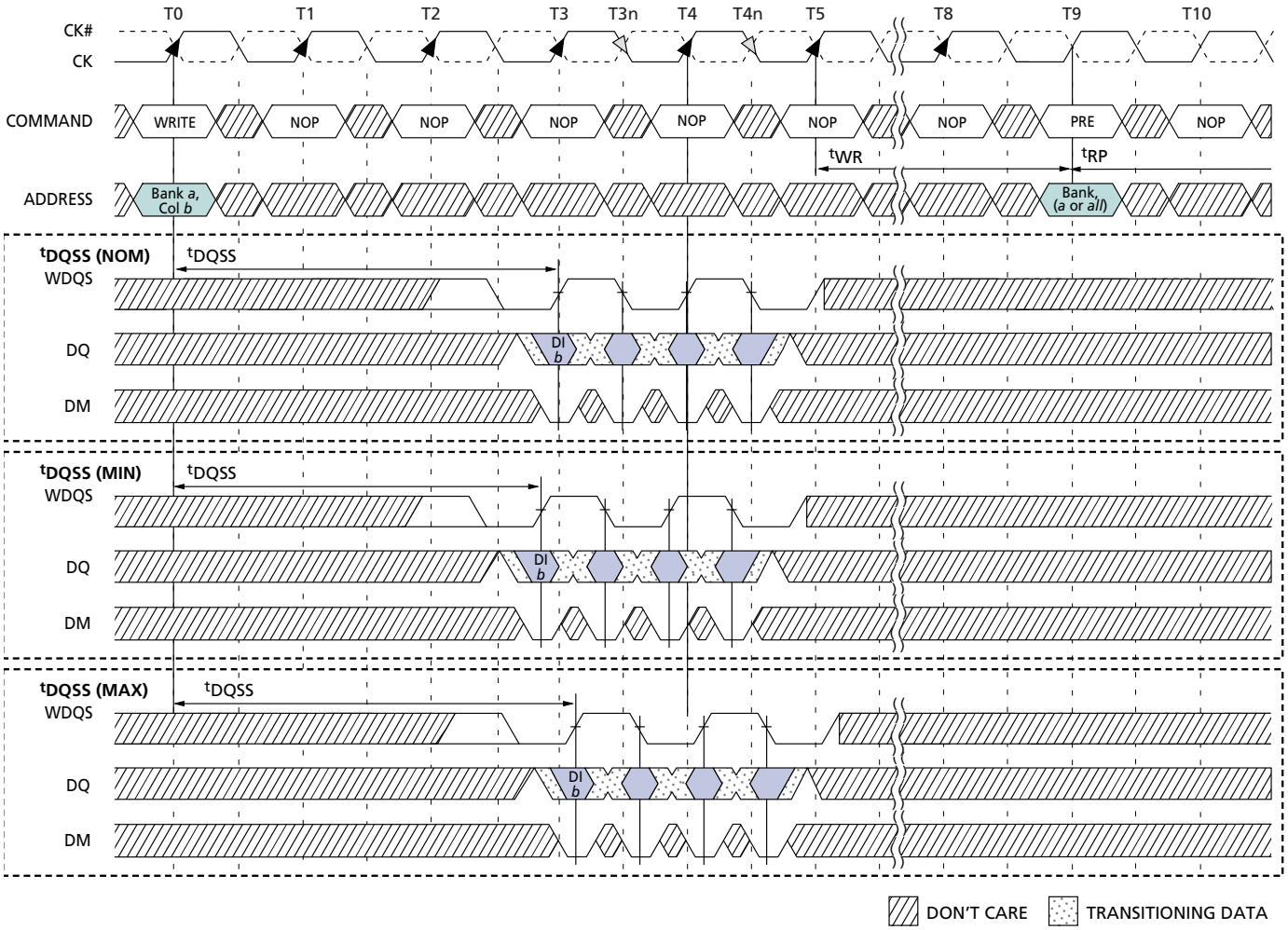
## Figure 25: WRITE to READ–Odd Number of Data Masking




NOTE:

1. DI *b* = data-in for column *b*.
2. A burst of 4 is shown.
3. $^{t}$WTR is referenced from the first positive CK edge after the last nibble (as if the whole nibble is being written).
4. The READ and WRITE commands are to the same device. However, the READ and WRITE commands may be to different devices, in which case, $^{t}$WTR is not required and the READ command could be applied earlier.
5. A8 is LOW with the WRITE command (auto precharge is disabled).
6. WRITE latency is set to 3.
7. The 4*n* prefetch architecture requires a 2-clock WRITE-to-READ turnaround time ($^{t}$WTR).

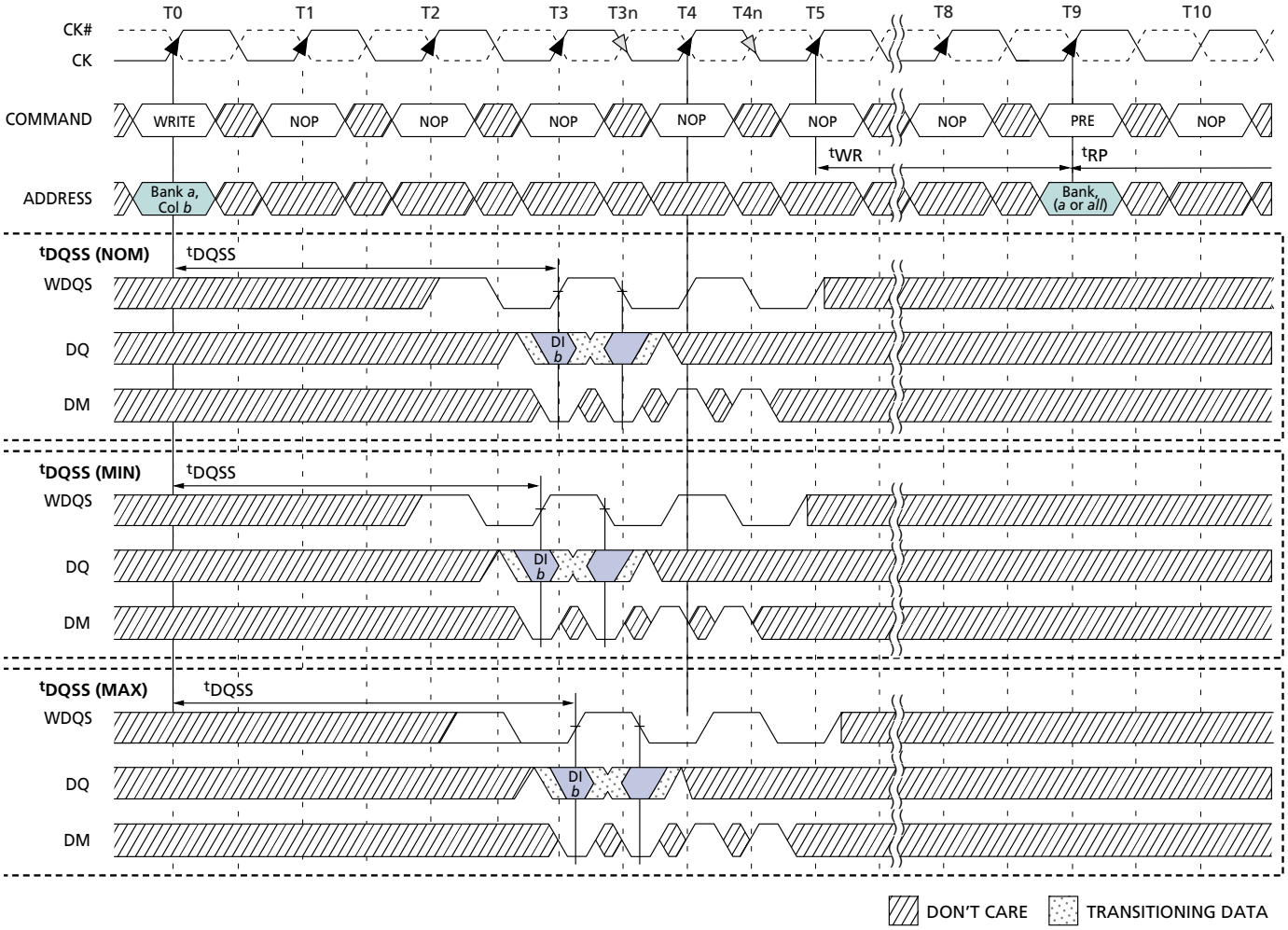
## Figure 26: WRITE to PRECHARGE




NOTE:

1. DI *b* = data-in for column *b*.
2. Three subsequent elements of data-in are applied in the specified order following DI *b*.
3. A burst of 4 is shown.
4. A8 is LOW with the WRITE command (auto precharge is disabled).
5. WRITE latency is set to 3.
6. The 4*n* prefetch architecture requires a 2-clock WRITE-to-READ turnaround time ($^{t}$WTR).

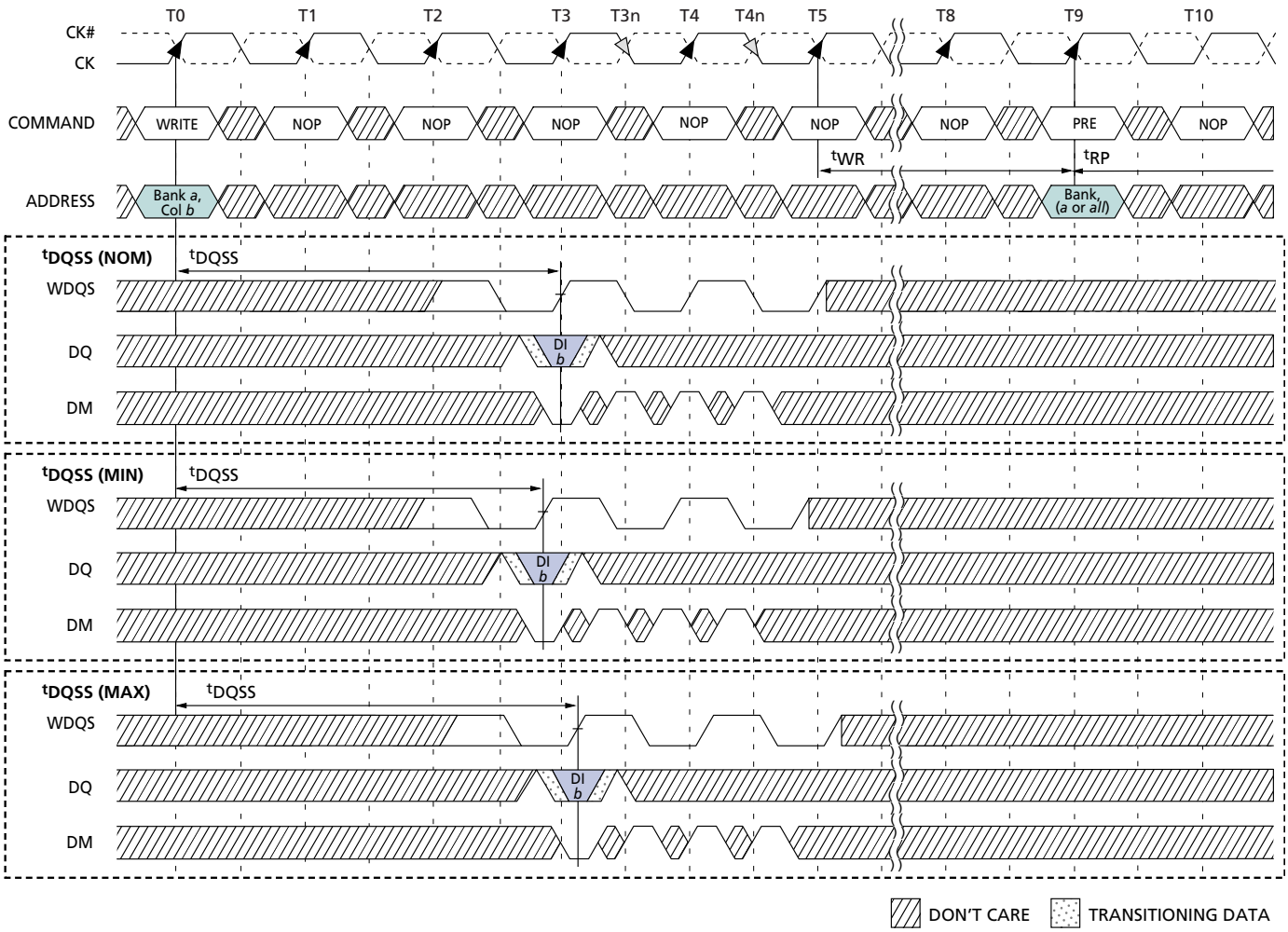
## Figure 27: WRITE to PRECHARGE – With Data Masking




NOTE:

1. DI *b* = data-in for column *b*.
2. One subsequent element of data-in is applied in the specified order following DI *b*.
3. A burst of 4 is shown.
4. $^{t}$WR is referenced from the first positive CK edge after the last nibble (as if the whole nibble is being written).
5. A8 is LOW with the WRITE command (auto precharge is disabled).
6. WRITE latency is set to 3.
7. The 4*n* prefetch architecture requires a 2-clock WRITE-to-READ turnaround time ($^{t}$WTR).

## Figure 28: WRITE to PRECHARGE – Odd Number of Data Masking




NOTE:

1. DI *b* = data-in for column *b*.
2. A burst of 4 is shown.
3. $^{t}$WTR is referenced from the first positive CK edge after the last nibble (as if the whole nibble is being written).
4. A8 is LOW with the WRITE command (auto precharge is disabled).
5. WRITE latency is set to 3.

## PRECHARGE

The PRECHARGE command (shown in Figure 29, PRECHARGE Command) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time ($^{t}$RP) after the PRECHARGE command is issued. Input A8 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

## POWER-DOWN (CKE Not Active)

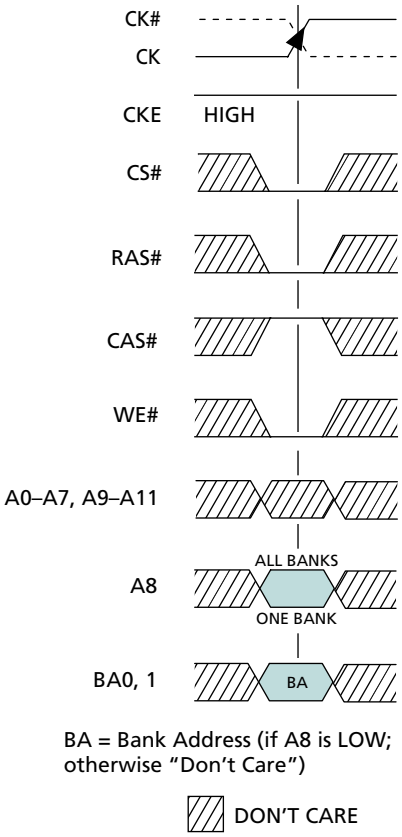
Unlike SDR SDRAMs, GDDR3 SDRAMs require CKE to be active at all times that an access is in progress: from the issuing of a READ or WRITE command until completion of the burst. For READs, a burst completion is defined when the Read Postamble is satisfied; For WRITEs, a burst completion is defined when the write postamble is satisfied.

Power-down (shown in Figure 30, Power-Down, on page 40) is entered when CKE is registered LOW. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, CK# and CKE. For maximum power savings, the user also has the option of disabling the DLL prior to entering power-down. In that case, the DLL must be enabled and reset after exiting power-down, and 200 clock cycles must occur before a READ command can be issued. However, power-down duration is limited by the refresh requirements of the device, so in most applications, the self refresh mode is preferred over the DLL-disabled power-down mode.

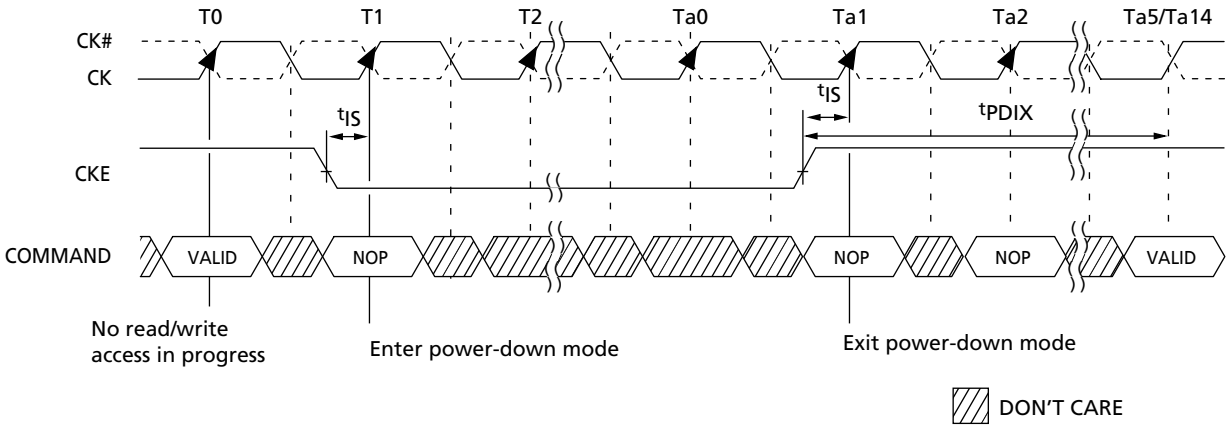
While in power-down, CKE LOW and a stable clock signal must be maintained at the inputs of the GDDR3 SDRAM, while all other input signals are "Don't Care."

The power-down state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command). A valid executable command may be applied four or fourteen clock cycles later.

**Figure 29: PRECHARGE Command**



## Figure 30: Power-Down




## Table 8: Truth Table – CKE

Notes: 1–4

| $CKE_{n-1}$ | $CKE_n$ | CURRENT STATE | $COMMAND_n$ | $ACTION_n$ | NOTES |
|---|---|---|---|---|---|
| L | L | Power-Down | X | Maintain Power-Down | |
| L | L | Self Refresh | X | Maintain Self Refresh | |
| L | H | Power-Down | DESELECT or NOP | Exit Power-Down | |
| L | H | Self Refresh | DESELECT or NOP | Exit Self Refresh | 5 |
| H | L | All Banks Idle | DESELECT or NOP | Precharge Power-Down Entry | |
| H | L | Bank(s) Active | DESELECT or NOP | Active Power-Down Entry | |
| H | L | All Banks Idle | AUTO REFRESH | Self Refresh Entry | |
| H | H | | See Truth Table 3 | | |

NOTE:

1. $CKE_n$ is the logic state of CKE at clock edge *n*; $CKE_{n-1}$ was the state of CKE at the previous clock edge.
2. Current state is the state of the GDDR3 SDRAM immediately prior to clock edge *n*.
3. $COMMAND_n$ is the command registered at clock edge *n*, and $ACTION_n$ is a result of $COMMAND_n$.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT or NOP commands should be issued on any clock edges occurring during the $^tXSR$ period. A minimum of 200 clock cycles is needed for the DLL to lock before applying a READ command if the DLL was disabled.

## Table 9: Truth Table – Current State Bank *n* – Command to Bank *n*

Note: 1–3; notes appear below table

| CURRENT STATE | CS# | RAS# | CAS# | WE# | COMMAND/ACTION | NOTES |
|---|---|---|---|---|---|---|
| Any | H | X | X | X | DESELECT (NOP/continue previous operation) | |
| | L | H | H | H | NO OPERATION (NOP/continue previous operation) | |
| | L | L | H | H | ACTIVE (select and activate row) | |
| Idle | L | L | L | H | AUTO REFRESH | 4 |
| | L | L | L | L | LOAD MODE REGISTER | 4 |
| Row Active | L | H | L | H | READ (select column and start READ burst) | 6 |
| | L | H | L | L | WRITE (select column and start WRITE burst) | 6 |
| | L | L | H | L | PRECHARGE (deactivate row in bank or banks) | 5 |
| Read (Auto Precharge Disabled) | L | H | L | H | READ (select column and start new READ burst) | 6 |
| | L | H | L | L | WRITE (select column and start WRITE burst) | 6, 8 |
| | L | L | H | L | PRECHARGE (only after the READ burst is complete | 5 |
| Write (Auto Precharge Disabled) | L | H | L | H | READ (select column and start READ burst) | 6, 7 |
| | L | H | L | L | WRITE (select column and start new WRITE burst) | 6 |
| | L | L | H | L | PRECHARGE (only after the WRITE burst is complete) | 5, 7 |

NOTE:

1. This table applies when $CKE_{n-1}$ was HIGH and $CKE_n$ is HIGH (see Truth Table 2) and after $^{t}$XSNR has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted (i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
3. All states and sequences not shown are illegal or reserved.
4. Not bank-specific; requires that all banks are idle, and bursts are not in progress.
5. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
6. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
7. Requires appropriate DM masking.
8. A WRITE command may be applied after the completion of the READ burst.
9. Current states with read or write with auto-precharge enabled
   The read with auto precharge enabled or write with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For WRITE with auto precharge, the precharge period begins when $^{t}$WR ends, with $^{t}$WR measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or $^{t}$RP) begins.
   During the precharge period of the read with auto precharge enabled or write with auto precharge enabled states, ACTIVE, PRECHARGE, READ, and WRITE commands to the other bank may be applied. In either case, all other related limitations apply (e.g., contention between read data and write data must be avoided).
   The minimum delay from a READ or WRITE command with auto precharge enabled to a command to a different bank is shown in Table 10.

## Table 10: Minimum Delay Between Commands to Different Banks with Auto Precharge Enabled

| FROM COMMAND | TO COMMAND | MINIMUM DELAY (WITH CONCURRENT AUTO PRECHARGE) |
|---|---|---|
| WRITE with AUTO PRECHARGE | READ or READ with AUTO PRECHARGE | [WL + (BL/2)] $^{t}$CK + $^{t}$WTR |
| | WRITE or WRITE with AUTO PRECHARGE | (BL/2) $^{t}$CK |
| | PRECHARGE | 1 $^{t}$CK |
| | ACTIVE | 1 $^{t}$CK |
| READ with AUTO PRECHARGE | READ or READ with AUTO PRECHARGE | (BL/2) * $^{t}$CK |
| | WRITE or WRITE with AUTO PRECHARGE | [CL + (BL/2) + 1 - WL] * $^{t}$CK |
| | PRECHARGE | 1 $^{t}$CK |
| | ACTIVE | 1 $^{t}$CK |

NOTE:

CL = CAS latency (CL) rounded up to the next integer.
BL = Burst length.
WL = WRITE latency.

## Current States For Truth Tables: Table 9 and Table 11

### *Idle*

The bank has been precharged, and $^{t}$RP has been met.

### *Row Active*

A row in the bank has been activated, and $^{t}$RCD has been met. No data bursts/accesses and no register accesses are in progress.

### *Read*

A READ burst has been initiated, with auto precharge disabled.

### *Write*

A WRITE burst has been initiated, with auto precharge disabled.

## Same-Bank Noninterruptible States

The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table 3, and according to Truth Table 4.

### *Precharging*

It starts with registration of a PRECHARGE command and ends when $^{t}$RP is met. Once $^{t}$RP is met, the bank will be in the idle state.

### *Row Activating*

It starts with registration of an ACTIVE command and ends when $^{t}$RCD is met. Once $^{t}$RCD is met, the bank will be in the "row active" state.

### *Read with Auto Precharge Enabled*

This starts with registration of a READ command with auto precharge enabled and ends when $^{t}$RP has been met. Once $^{t}$RP is met, the bank will be in the idle state.

### *Write with Auto Precharge Enabled*

This starts with registration of a WRITE command with auto precharge enabled and ends when $^{t}$RP has been met. Once $^{t}$RP is met, the bank will be in the idle state.

## Noninterruptible States

The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.

### *Refreshing*

Starts with registration of an AUTO REFRESH command and ends when $^{t}$RC is met. Once $^{t}$RFC is met, the GDDR3 SDRAM will be in the all banks idle state.

### *Accessing Mode Register*

This starts with registration of a LOAD MODE REGISTER command and ends when $^{t}$MRD has been met. Once $^{t}$MRD is met, the GDDR3 SDRAM will be in the all banks idle state.

### *Precharging All*

It starts with registration of a PRECHARGE ALL command and ends when $^{t}$RP is met. Once $^{t}$RP is met, all banks will be in the idle state.

### *READ or WRITE*

Starts with the registration of the ACTIVE command and ends with the last valid data nibble.

## Table 11: Truth Table – Current State Bank *n* – Command To Bank *m*

Notes: 1–4; notes appear below and on next page

| CURRENT STATE | CS# | RAS# | CAS# | WE# | COMMAND/ACTION | NOTES |
|---|---|---|---|---|---|---|
| Any | H | X | X | X | DESELECT (NOP/continue previous operation) | |
| | L | H | H | H | NO OPERATION (NOP/continue previous operation) | |
| Idle | X | X | X | X | Any Command Otherwise Allowed to Bank *m* | |
| Row Activating, Active, or Precharging | L | L | H | H | ACTIVE (select and activate row) | |
| | L | H | L | H | READ (select column and start READ burst) | 5 |
| | L | H | L | L | WRITE (select column and start WRITE burst) | 5 |
| | L | L | H | L | PRECHARGE | |
| Read (Auto Precharge Disabled) | L | L | H | H | ACTIVE (select and activate row) | |
| | L | H | L | H | READ (select column and start new READ burst) | 5 |
| | L | H | L | L | WRITE (select column and start WRITE burst) | 5 |
| | L | L | H | L | PRECHARGE | |
| Write (Auto Precharge Disabled) | L | L | H | H | ACTIVE (select and activate row) | |
| | L | H | L | H | READ (select column and start READ burst) | 5, 6 |
| | L | H | L | L | WRITE (select column and start new WRITE burst) | 5 |
| | L | L | H | L | PRECHARGE | |
| Read (With Auto Precharge) | L | L | H | H | ACTIVE (select and activate row) | |
| | L | H | L | H | READ (select column and start new READ burst) | 5 |
| | L | H | L | L | WRITE (select column and start WRITE burst) | 5 |
| | L | L | H | L | PRECHARGE | |
| Write (With Auto Precharge) | L | L | H | H | ACTIVE (select and activate row) | |
| | L | H | L | H | READ (select column and start READ burst) | 5 |
| | L | H | L | L | WRITE (select column and start new WRITE burst) | 5 |
| | L | L | H | L | PRECHARGE | |

NOTE:

1. This table applies when $CKE_{n-1}$ was HIGH and $CKE_n$ is HIGH (see Truth Table 2) and after $^{t}$XSNR has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted (i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m*, assuming that bank *m* is in such a state that the given command is allowable).
3. AUTO REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.
4. All states and sequences not shown are illegal or reserved.
5. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
6. Requires appropriate DM masking.

## Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Voltage on $V_{DD}$ Supply
Relative to Vss ..... -0.5V to +2.5V
Voltage on $V_{DD}Q$ Supply
Relative to Vss ..... -0.5V to +2.5V
Voltage on $V_{REF}$ and Inputs
Relative to Vss ..... -0.5V to +2.5V
Voltage on I/O Pins
Relative to Vss ..... -0.5V to $V_{DD}Q$ +0.5V
MAX Junction Temperature, $T_J$ ..... +125°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation..... TBD
Short Circuit Output Current ..... 50mA

## Table 12: DC Electrical Characteristics and Operating Conditions

Notes: 1–5, 16, 40; notes appear on pages 51–53; 0°C ≤ $T_C$ ≤ 85 °C; $V_{DD}$ = +1.8V ±0.100V, $V_{DD}Q$ = +1.8V ±0.100V

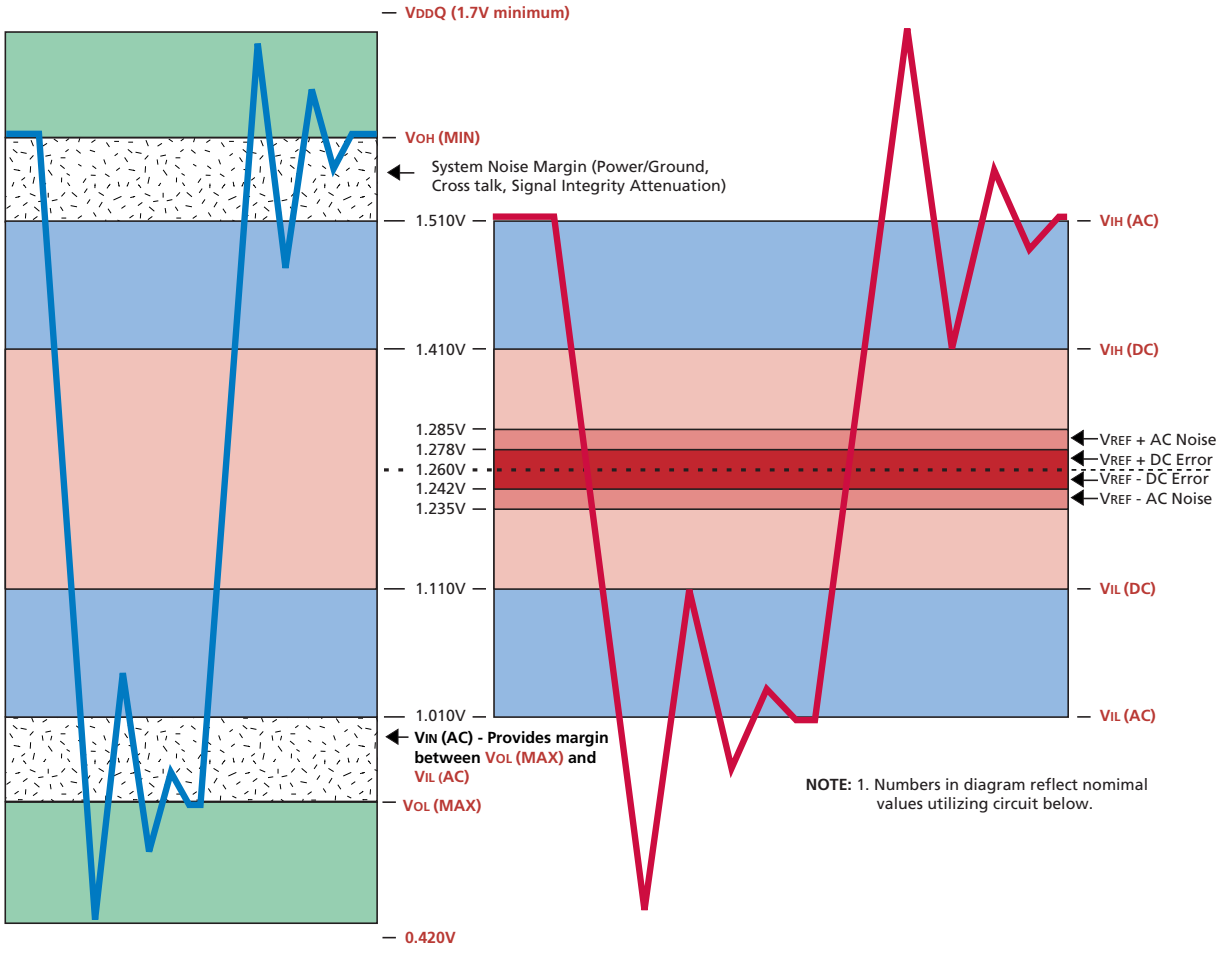
| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 1.7 | 1.9 | V | 32, 45 |
| I/O Supply Voltage | $V_{DD}Q$ | 1.7 | 1.9 | V | 45 |
| I/O Reference Voltage | $V_{REF}$ | 0.69 x $V_{DD}Q$ | 0.71 x $V_{DD}Q$ | V | 6 |
| Input High (Logic 1) Voltage | $V_{IH}$(DC) | $V_{REF}$ + 0.15 | | V | 28 |
| Input Low (Logic 0) Voltage | $V_{IL}$(DC) | | $V_{REF}$ - 0.15 | V | 28 |
| INPUT LEAKAGE CURRENT Any Input 0V ≤ $V_{IN}$ ≤ $V_{DD}$ (All other pins not under test = 0V) | $I_I$ | -5 | 5 | µA | |
| OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ $V_{OUT}$ ≤ $V_{DD}Q$) | $I_{OZ}$ | -5 | 5 | µA | |
| OUTPUT Logic Low | $V_{OL}$(DC) | | 0.76 | V | |

## Table 13: AC Input Operating

Notes: 1–5, 16, 40; notes appear on pages 51–53; 0°C ≤ $T_C$ ≤ 85°C; $V_{DD}$ = +1.8V ±0.100V, $V_{DD}Q$ = +1.8V ±0.100V

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input High (Logic 1) Voltage; DQ | $V_{IH}$(AC) | $V_{REF}$ + 0.250 | – | V | 14, 28, 39 |
| Input Low (Logic 0) Voltage; DQ | $V_{IL}$(AC) | – | $V_{REF}$ - 0.250 | V | 14, 28, 39 |
| Clock Input Differential Voltage; CK and CK# | $V_{ID}$(AC) | 0.5 | $V_{DD}Q$ + 0.5 | V | 8 |
| Clock Input Crossing Point Voltage; CK and CK# | $V_{IX}$(AC) | $V_{REF}$ - 0.15 | $V_{REF}$ + 0.15 | V | 9 |

## Figure 31: VDDQ Input Voltage Waveform

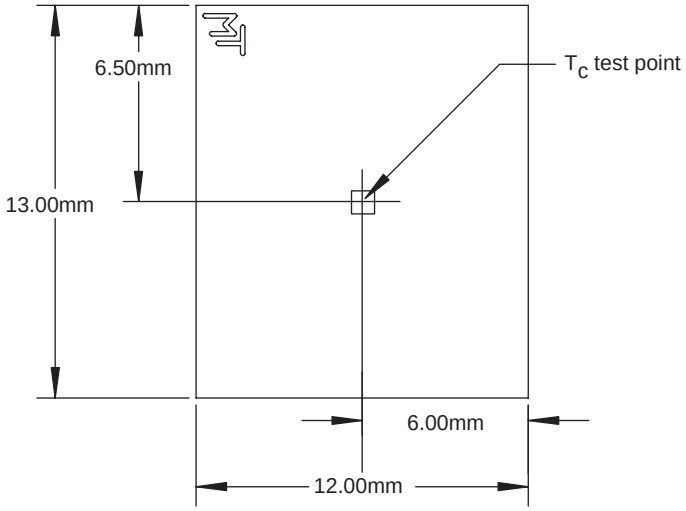


## Table 14: Thermal Characteristics

| PARAMETER/CONDITION | POWER | SYMBOL | VALUE | UNITS | NOTES |
|---|---|---|---|---|---|
| Operating Case Temperature | <1W | $T_C$ | 0–90 | C | 1, 2, 3 |
| | 1W–2W | $T_C$ | 0–85 | C | 1, 2, 3 |
| | 2W–3W | $T_C$ | 0–80 | C | 1, 2, 3 |
| Junction to Case (TOP) | | ΘJC | TBD | C/W | 4 |

NOTE:
1. MAX operating case temperature; $T_C$ is measured in the center of the package, see figure below.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum $T_C$ during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum $T_C$ during operation.
4. The thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number.

### Figure 32: Tc Test Point

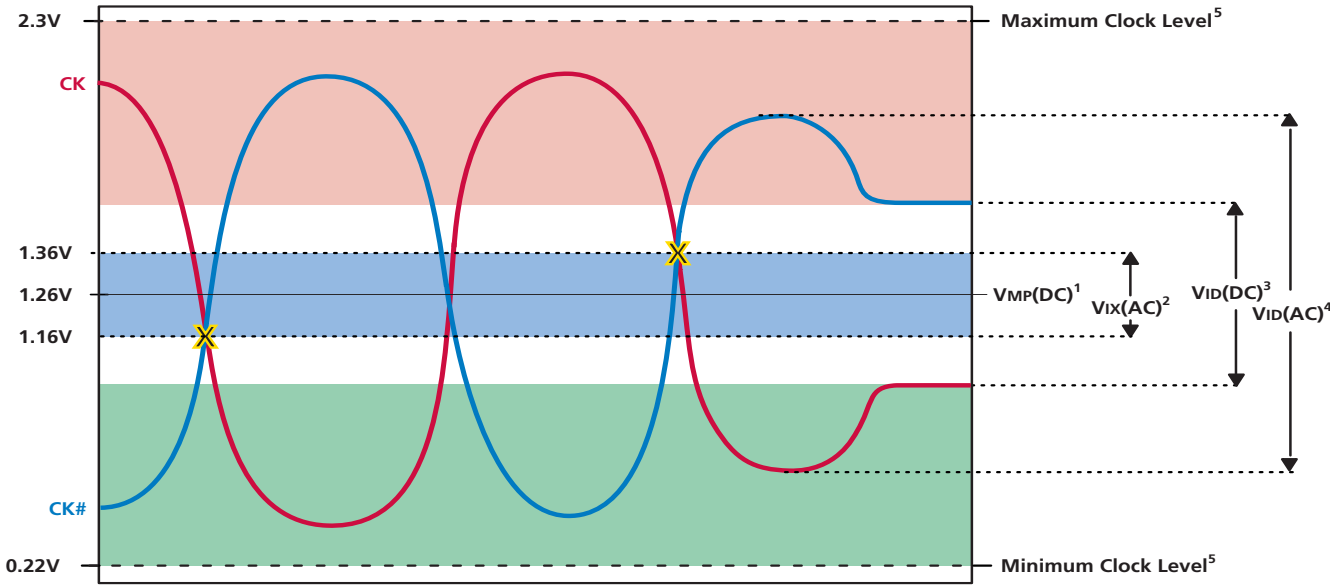



## Table 15: Clock Input Operating Conditions

Notes: 1–5, 15, 16, 30; notes appear on pages 51–53; 0°C ≤ $T_C$ ≤ 85°C; VDD = +1.8V ±0.100V, VDDQ = +1.8V ±0.100V

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Clock Input Midpoint Voltage; CK and CK# | VMP(DC) | 1.16 | 1.36 | V | 6, 9 |
| Clock Input Voltage Level; CK and CK# | VIN(DC) | 0.42 | VDDQ + 0.3 | V | 6 |
| Clock Input Differential Voltage; CK and CK# | VID(DC) | 0.22 | VDDQ | V | 6, 8 |
| Clock Input Differential Voltage; CK and CK# | VID(AC) | 0.5 | VDDQ + 0.5 | V | 8 |
| Clock Input Crossing Point Voltage; CK and CK# | VIX(AC) | VREF - 0.15 | VREF + 0.15 | V | 9 |

## Figure 33: Clock Input




NOTE:
1. This provides a minimum of 1.16V to a maximum of 1.36V, and is always 70% of $V_{DD}Q$.
2. CK and CK# must cross in this region.
3. CK and CK# must meet at least V(DC) MIN when static and is centered around $V_{MP}$(DC).
4. CK and CK# must have a minimum 600mV peak-to-peak swing.
5. CK or CK# may not be more positive than $V_{DD}Q$ + 0.5V or lower than 0.22V.
6. For AC operation, all DC clock requirements must also be satisfied.
7. Numbers in diagram reflect nominal values.

## Table 16: Capacitance

Note: 13; notes appear on pages 51–53

| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Delta Input/Output Capacitance: DQs, DQS, DM | $DC_{IO}$ | – | 0.20 | pF | 24 |
| Delta Input Capacitance: Command and Address | $DC_{I1}$ | – | 0.40 | pF | 29 |
| Delta Input Capacitance: CK, CK# | $DC_{I2}$ | – | 0.20 | pF | 29 |
| Input/Output Capacitance: DQs, DQS, DM | $C_{IO}$ | 3.5 | 4.5 | pF | |
| Input Capacitance: Command and Address | $C_{I1}$ | 3.0 | 4.0 | pF | |
| Input Capacitance: CK, CK# | $C_{I2}$ | 3.0 | 4.0 | pF | |
| Input Capacitance: CKE | $C_{I3}$ | 3.0 | 4.0 | pF | |

## Table 17: IDD Specifications and Conditions

Notes: 1–5, 10, 12, 14, 40; notes on pages 51–53; 0°C ≤ $T_C$ ≤ 85°C; VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V

| | | | MAX | | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER/CONDITION | | SYMBOL | -16 | -18 | -2 | UNITS | NOTES |
| OPERATING CURRENT: One bank; Active Precharge; $^tRC$ = $^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and control inputs changing once per clock cycle; WL = 4 RC (MIN) | | IDD0 | TBD | TBD | TBD | mA | 22, 46 |
| OPERATING CURRENT: One bank; Active Read Precharge; Burst = 4; $^tRC$ (MIN); $^tCK$ = $^tCK$ (MIN); I RC = OUT = 0mA; Address and control inputs changing once per clock cycle; WL = 4 | | IDD1 | TBD | TBD | TBD | mA | 22, 46 |
| PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; $^tCK$ = $^tCK$ MIN; CKE = LOW | | IDD2P | TBD | TBD | TBD | mA | 32 |
| IDLE STANDBY CURRENT: CS# = HIGH; All banks idle; $^tCK$ = $^tCK$ (MIN); CKE = HIGH; inputs changing once per clock cycle | | IDD2N | TBD | TBD | TBD | mA | |
| ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; $^tCK$ = $^tCK$ (MIN); CKE = LOW; WL=4 | | IDD3P | TBD | TBD | TBD | mA | 32 |
| ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One bank; Active Precharge; $^tRC$ = $^tRAS$ (MAX); $^tCK$ = $^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle | | IDD3N | TBD | TBD | TBD | mA | 22 |
| OPERATING CURRENT: Burst = 4; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $^tCK$ = $^tCK$ (MIN); IOUT = 0mA; WL = 4 | | IDD4R | TBD | TBD | TBD | mA | |
| OPERATING CURRENT: Burst = 4; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $^tCK$ = $^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; WL = 4 | | IDD4W | TBD | TBD | TBD | mA | 46 |
| AUTO REFRESH CURRENT | $^tRFC$ (MIN) | IDD5A | TBD | TBD | TBD | mA | 22 |
| | $^tRFC$ = 7.8µs | IDD5B | TBD | TBD | TBD | mA | 27 |
| SELF REFRESH CURRENT: CKE ≤ 0.2V | | IDD6 | TBD | TBD | TBD | mA | 11 |

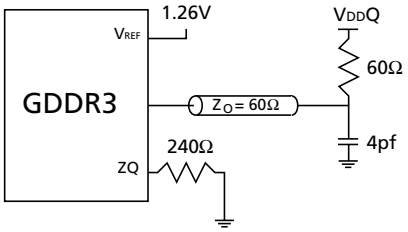
## Table 18: Electrical Characteristics and AC Operating Conditions

Notes: 1-5,14-16, 33, 40; notes on pages 51–53; 0°C ≤ $T_C$ ≤ 85 °C; $V_{DD}$ = +1.8V ±0.1V, $V_{DDQ}$ = +1.8V ±0.1V

| AC CHARACTERISTICS | | -16 | | -18 | | -2 | | | |
|---|---|---|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Access window of RDQS from CK/CK# | $^tAC$ | -0.25 | +0.25 | -0.25 | +0.25 | -0.25 | +0.25 | $^tCK$ | |
| CK high-level width | $^tCH$ | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | $^tCK$ | 30 |
| CK low-level width | $^tCL$ | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | $^tCK$ | 30 |
| Clock cycle time CL = 8 | $^tCK(8)$ | 1.66 | 3.3 | – | – | – | – | ns | 33, 40 |
| Clock cycle time CL = 7 | $^tCK(7)$ | 1.81 | 3.3 | 1.81 | 3.3 | – | – | ns | 33, 40 |
| Clock cycle time CL = 6 | $^tCK(6)$ | 2.00 | 3.3 | 2.00 | 3.3 | 2.00 | 3.3 | ns | 33, 40 |
| Clock cycle time CL = 5 | $^tCK(5)$ | – | – | 2.5 | 3.3 | 2.5 | 3.3 | ns | 33, 40 |
| WRITE Latency | $^tWL$ | 2 | 4 | 2 | 4 | 1 | 4 | $^tCK$ | 43 |
| DQ and DM input hold time relative to DQS | $^tDH$ | 0.225 | | 0.25 | | 0.25 | | ns | 26, 31 |
| DQ and DM input setup time relative to DQS | $^tDS$ | 0.225 | | 0.25 | | 0.25 | | ns | 26, 31 |
| Active termination setup time | $^tATS$ | 10 | | 10 | | 10 | | ns | |
| Active termination hold time | $^tATH$ | 10 | | 10 | | 10 | | ns | |
| DQS input high pulse width | $^tDQSH$ | 0.48 | 0.52 | 0.48 | 0.52 | 0.48 | 0.52 | $^tCK$ | |
| DQS input low pulse width | $^tDQSL$ | 0.48 | 0.52 | 0.48 | 0.52 | 0.48 | 0.52 | $^tCK$ | |
| DQS-DQ skew | $^tDQSQ$ | -0.160 | 0.160 | -0.190 | 0.190 | -0.225 | 0.225 | ns | 25, 26 |
| Write command to first DQS latching transition | $^tDQSS$ | WL - 0.25 | WL + 0.25 | WL - 0.25 | WL + 0.25 | WL - .025 | WL + 0.25 | $^tCK$ | |
| DQS falling edge to CK rising – setup time | $^tDSS$ | 0.25 | | 0.25 | | 0.25 | | $^tCK$ | |
| DQS falling edge from CK rising – hold time | $^tDSH$ | 0.25 | | 0.25 | | 0.25 | | $^tCK$ | |
| Half strobe period | $^tHP$ | $^tDQSH$, $^tDQSL$ | | $^tDQSH$, $^tDQSL$ | | $^tDQSH$, $^tDQSL$ | | ns | 34 |
| Data-out high-impedance window from CK/CK# | $^tHZ$ | -0.3 | | -0.3 | | -0.3 | | ns | 18 |
| Data-out low-impedance window fromCK/CK# | $^tLZ$ | -0.3 | | -0.3 | | -0.3 | | ns | 18 |
| Address and control input hold time | $^tIH$ | 0.45 | | 0.5 | | 0.5 | | ns | 14 |
| Address and control input setup time | $^tIS$ | 0.45 | | 0.5 | | 0.5 | | ns | 14 |
| Address and control input pulse width | $^tIPW$ | 1.2 | | 1.3 | | 1.3 | | ns | |
| LOAD MODE REGISTER command cycle time | $^tMRD$ | 4 | | 4 | | 4 | | $^tCK$ | 44 |
| Data valid output window | $^tDV$ | $^tDQHP$ - 0.32ns | | $^tDQHP$ - 0.38ns | | $^tDQHP$ - 0.45ns | | ns | 25, 26, 34 |
| ACTIVE to PRECHARGE command | $^tRAS$ | 35 | 120,000 | 36 | 120,000 | 36 | 120,000 | ns | 35 |
| ACTIVE to ACTIVE/AUTO REFRESH command period | $^tRC$ | 52 | | 52 | | 52 | | ns | |
| AUTO REFRESH command period | $^tRFC$ | 60 | | 60 | | 60 | | ns | |
| REFRESH to REFRESH command interval` | $^tREFC$ | | 70 | | 70 | | 70 | µs | 23 |
| Average periodic refresh interval | $^tREFI$ | | 7.8 | | 7.8 | | 7.8 | µs | 23 |
| ACTIVE to READ delay | $^tRCDR$ | 16 | | 16 | | 16 | | ns | |
| ACTIVE to WRITE delay | $^tRCDW$ | 12 | | 12 | | 12 | | ns | |
| PRECHARGE command period | $^tRP$ | 14.4 | | 14.4 | | 16 | | ns | |
| DQS read preamble | $^tRPRE$ | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | $^tCK$ | |
| DQS read postamble | $^tRPST$ | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | $^tCK$ | |
| ACTIVE bank *a* to ACTIVE bank *b* command | $^tRRD$ | 6 | | 6 | | 6 | | ns | |
| Exit Power-down | $^tPDIX$ | 4 + $^tIS$ | | 4 + $^tIS$ | | 4 + $^tIS$ | | $^tCK$ | |
| DQS write preamble | $^tWPRE$ | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | $^tCK$ | 47 |
| DQS write preamble setup time | $^tWPRES$ | 0 | | 0 | | 0 | | ns | 20, 21 |
| DQS write postamble | $^tWPST$ | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | $^tCK$ | 19, 37 |
| Write recovery time | $^tWR$ | 4 | | 4 | | 4 | | $^tCK$ | |
| Internal WRITE to READ command delay | $^tWTR$ | 3 | | 3 | | 3 | | $^tCK$ | |
| Exit SELF REFRESH to non-READ command | $^tXSNR$ | 66 | | 66 | | 66 | | $^tCK$ | |
| Exit SELF REFRESH to READ command | $^tXSRD$ | 200 | | 200 | | 200 | | $^tCK$ | |

## Notes

1. All voltages referenced to $V_{SS}$.
2. Tests for AC timing, $I_{DD}$, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:

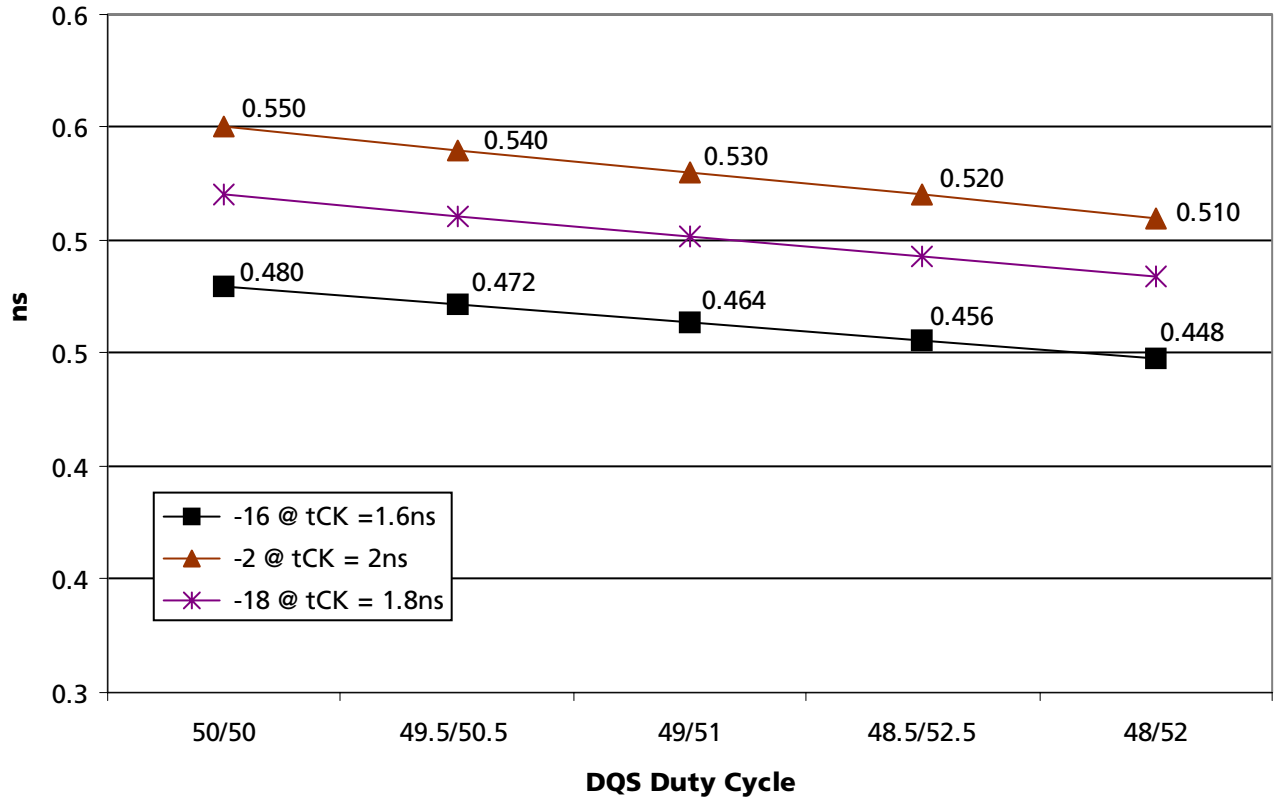



4. AC timing and $I_{DD}$ tests may use a $V_{IL}$-to-$V_{IH}$ swing of up to 1.0V in the test environment, but input timing is still referenced to $V_{REF}$ (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 3 V/ns in the range between $V_{IL}$(AC) and $V_{IH}$(AC).
5. The AC and DC input level specifications are a pseudo open drain design for improved high-speed signaling.
6. $V_{REF}$ is expected to equal 70 percent of $V_{DDQ}$ for the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on $V_{REF}$ may not exceed ±2 percent of the DC value. Thus, from 70% of $V_{DDQ}$, $V_{REF}$ is allowed ±25mV for DC error and an additional ±25mV for AC noise.
7. Reserved for future use.
8. $V_{ID}$ is the magnitude of the difference between the input level on CK and the input level on CK#.
9. The value of $V_{IX}$ is expected to equal 70 percent of $V_{DDQ}$ for the transmitting device and must track variations in the DC level of the same.
10. $I_{DD}$ is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at minimum CAS latency and does not include the on-die termination current. Outputs are open during $I_{DD}$ measurements.
11. Enables on-chip refresh and address counters.
12. $I_{DD}$ specifications are tested after the device is properly initialized.
13. This parameter is sampled. $V_{DD}$ = +1.8V ±0.1V, $V_{DDQ}$ = +1.8V ±0.1V, $V_{REF}$ = $V_{SS}$, f = 500 MHz, $T_A$ = 25°C, $V_{OUT}$(DC) = 0.75V, $V_{DDQ}$, $V_{OUT}$ (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
14. Command/Address input slew rate = 3 V/ns. If the slew rate is less than 3 V/ns, timing is no longer referenced to the midpoint but to the $V_{IL}$(AC) maximum and $V_{IH}$(AC) minimum points.
15. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is $V_{REF}$.
16. Inputs are not recognized as valid until $V_{REF}$ stabilizes. Exception: during the period before $V_{REF}$ stabilizes, MF, CKE ≤ 0.3 x $V_{DDQ}$ is recognized as LOW.
17. Reserved for future use.
18. $^{t}$HZ and $^{t}$LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
19. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
20. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
21. It is recommended that WDQS be valid (HIGH or LOW) on or before the WRITE command.
22. MIN ($^{t}$RC or $^{t}$RFC) for $I_{DD}$ measurements is the smallest multiple of $^{t}$CK that meets the minimum absolute value for the respective parameter. $^{t}$RAS MAX for $I_{DD}$ measurements is the largest multiple of $^{t}$CK that meets the maximum absolute value for $^{t}$RAS.
23. The refresh period is 4K every 32ms. This equates to an average refresh rate of 7.8µs.
24. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.
25. The valid data window is derived by achieving other specifications – $^{t}$DQHP and $^{t}$DQSQ, [$^{t}$DQHP - 0.32ns (-16), $^{t}$DQHP - 0.38ns (-18), $^{t}$DQHP - 0.45ns (-2)]. The data valid window derates in direct proportion to the strobe duty cycle and a practical data valid window can be derived. The strobe is allowed a maximum duty cycle variation of 48:52. Functionality is uncertain when operating beyond a 48:52 ratio. The data valid window derating curves are provided below for duty cycles

ranging between 50:50 and 48:52, based off the optional READ strobe.

26. Referenced to each output group: RDQS0 with DQ0–DQ7, RDQS1 with DQ8–DQ15, RDQS2 with DQ16–DQ23, and RDQS with DQ24–DQ31.
27. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period ($^{t}$RFC [MIN]) else CKE is LOW (e.g., during standby).
28. The DC values define where the input slew rate requirements are imposed, and the input signal must not violate these levels in order to maintain a valid level. The inputs require the AC value to be achieved during signal transition edge, and the driver should achieve the same slew rate through the AC values.
29. The input capacitance per pin group will not differ by more than this maximum amount for any given device.
30. CK and CK# input slew rate must be ≥ 3 V/ns.
31. DQ and DM input slew rates must not deviate from WDQS by more than 10 percent. If the DQ/DM/WDQS slew rate is less than 3 V/ns, timing is no longer referenced to the midpoint but to the $V_{IL}$(AC) maximum and $V_{IH}$(AC) minimum points.
32. $V_{DD}$ must not vary more than 4 percent if CKE is not active while any bank is active.
33. The clock is allowed up to ±90ps of jitter. Each timing parameter is allowed to vary by the same amount.
34. $^{t}$HP (MIN) is the lesser of $^{t}$DQSL minimum and $^{t}$DQSH minimum actually applied to the device CK and CK# inputs, collectively during bank active.
35. For READs and WRITEs with auto precharge the GDDR3 device will hold off the internal PRECHARGE command until $^{t}$RAS (MIN) has been satisfied.

**Figure 34: Derating Data Valid Window ($^{t}$QH - $^{t}$DQSQ)**



36. Programmable Drive Curves 40Ω example:
    a) The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 35, Pull-Down Characteristics.
    b) The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 35, Pull-Down Characteristics.
    c)The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 36, Pull-Up Characteristics.
    d)The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 36, Pull-Up Characteristics.
37. The last rising edge of WDQS after the write postamble must be driven HIGH by the controller. WDQS cannot be pulled HIGH by the on-die termination alone. For the read postamble the GDDR3 will drive the last rising edge of the read postamble.
38. The voltage levels used are derived from the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
39. $V_{IH}$ overshoot: $V_{IH}$ (MAX) = $V_{DD}Q$ + 0.5V for a pulse width ≤ 500ps and the pulse width cannot be greater than 1/3 of the cycle rate. $V_{IL}$ undershoot: $V_{IL}$ (MIN) = 0.0V for a pulse width ≤ 500ps and the pulse width cannot be greater than 1/3 of the cycle rate.
40. The DLL must be reset when changing the frequency, followed by 200 clock cycles.
41. Junction temperature is a function of total device power dissipation and device mounting environment. Measured per SEMI G38-87.
42. The thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number. These parameters are not tested in production.
43. The WRITE latency can be set from 1 to 4 clocks but can never be less than 2ns for latencies of 1 and 2 clocks. When the WRITE latency is set to 1 or 2 clocks, the input buffers are always on, reducing the latency but adding power. When the WRITE latency is set to 3 or 4 clocks the input buffers are turned on during the WRITE commands for lower power operation and can never be less than 5ns.
44. A minimum of 14 clock cycles is required after the LOAD MODE REGISTER (LMR) command before a READ command can be issued.
45. $V_{DD}$, $V_{REF}$, and $V_{DD}Q$ must track.
46. Setting the WRITE latency to 1 or 2 clocks will increase the operating current by XmA.
47. A low-to-high transition on the WDQS line is not allowed in the half clock cycle prior to the write preamble.

**Figure 35: Pull-Down Characteristics**

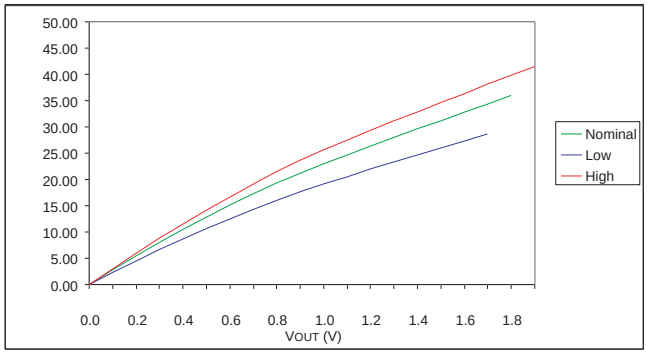
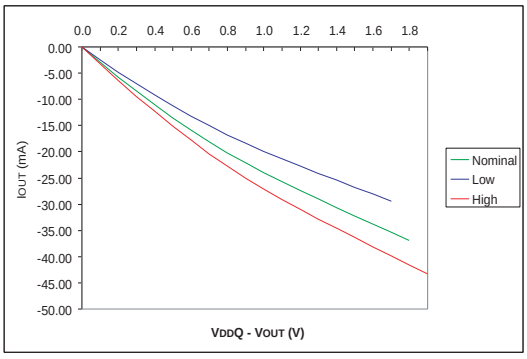



**Figure 36: Pull-Up Characteristics**



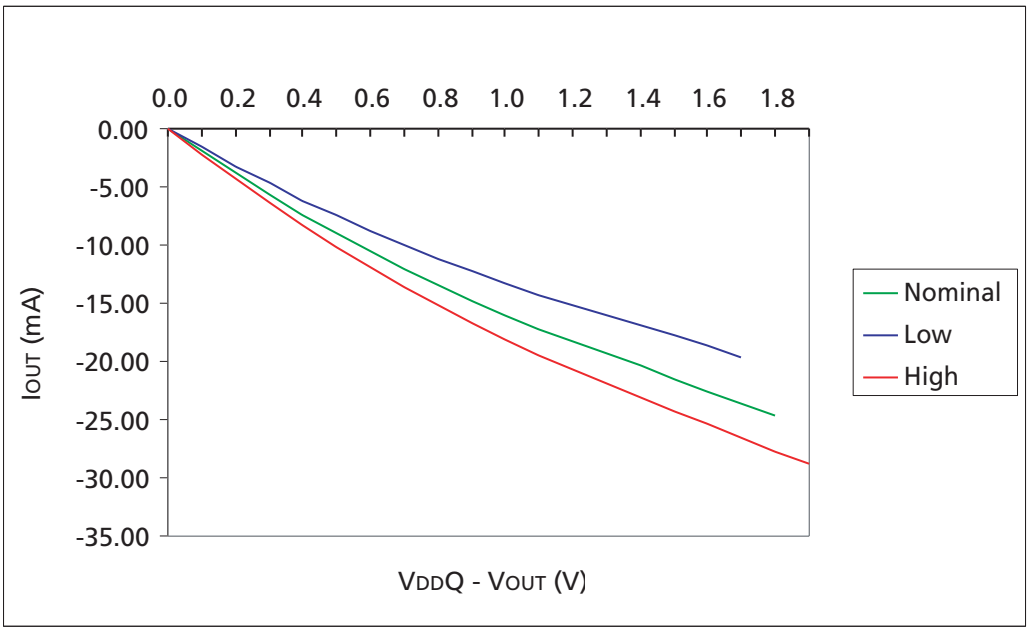
## Table 19: Programmed Drive Characteristics at 40Ω

| VOLTAGE (V) | PULL-DOWN CURRENT (mA) | | | PULL-UP CURRENT (mA) | | |
|---|---|---|---|---|---|---|
| | NOMINAL | MINIMUM | MAXIMUM | NOMINAL | MINIMUM | MAXIMUM |
| 0.1 | 2.77 | 2.32 | 3.04 | -2.93 | -2.44 | -3.27 |
| 0.2 | 5.44 | 4.56 | 5.98 | -5.75 | -4.79 | -6.42 |
| 0.3 | 8.02 | 6.70 | 8.82 | -8.46 | -7.03 | -9.45 |
| 0.4 | 10.49 | 8.75 | 11.56 | -11.05 | -9.18 | -12.37 |
| 0.5 | 12.86 | 10.71 | 14.19 | -13.52 | -11.23 | -15.17 |
| 0.6 | 15.12 | 12.57 | 16.72 | -15.87 | -13.17 | -17.83 |
| 0.7 | 17.27 | 14.35 | 19.14 | -18.10 | -15.01 | -20.37 |
| 0.8 | 19.31 | 16.03 | 21.44 | -20.21 | -16.74 | -22.78 |
| 0.9 | 21.24 | 17.63 | 23.61 | -22.18 | -18.37 | -25.04 |
| 1.0 | 23.04 | 19.13 | 25.66 | -24.03 | -19.90 | -27.17 |
| 1.1 | 24.74 | 20.55 | 27.57 | -25.77 | -21.34 | -29.17 |
| 1.2 | 26.38 | 21.94 | 29.39 | -27.42 | -22.72 | -31.04 |
| 1.3 | 27.99 | 23.31 | 31.16 | -29.03 | -24.07 | -32.85 |
| 1.4 | 29.59 | 24.67 | 32.91 | -30.62 | -25.40 | -34.62 |
| 1.5 | 31.18 | 26.03 | 34.65 | -32.21 | -26.73 | -36.37 |
| 1.6 | 32.77 | 27.38 | 36.38 | -33.78 | -28.06 | -38.11 |
| 1.7 | 34.36 | 28.73 | 38.11 | -35.35 | -29.37 | -39.85 |
| 1.8 | 35.94 | – | 39.83 | -36.92 | – | -41.58 |
| 1.9 | - | – | 41.55 | – | – | -43.30 |

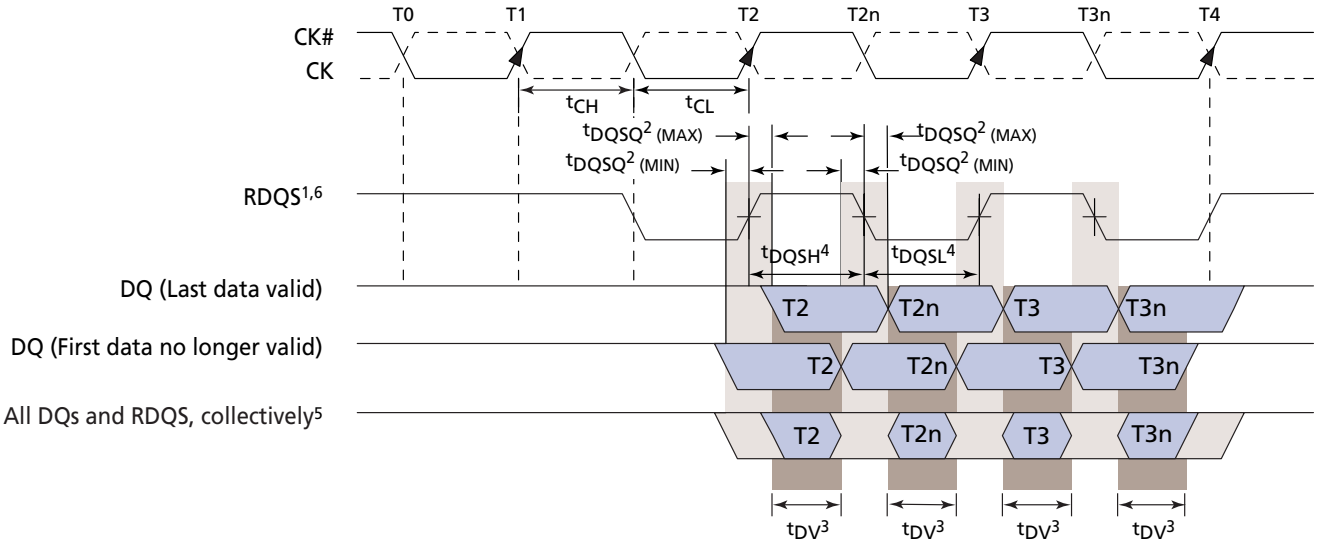
## Table 20: Programmed Drive Characteristics at 60Ω for Active Termination

| VOLTAGE (V) | PULL-UP CURRENT (mA) | | |
|---|---|---|---|
| | NOMINAL | MINIMUM | MAXIMUM |
| 0.1 | -1.95 | -1.63 | -2.18 |
| 0.2 | -3.83 | -3.19 | -4.28 |
| 0.3 | -5.64 | -4.69 | -6.30 |
| 0.4 | -7.36 | -6.12 | -8.25 |
| 0.5 | -9.01 | -7.49 | -10.11 |
| 0.6 | -10.58 | -8.78 | -11.89 |
| 0.7 | -12.07 | -10.01 | -13.58 |
| 0.8 | -13.47 | -11.16 | -15.18 |
| 0.9 | -14.79 | -12.25 | -16.70 |
| 1.0 | -16.02 | -13.27 | -18.12 |
| 1.1 | -17.18 | -14.23 | -19.44 |
| 1.2 | -18.28 | -15.14 | -20.70 |
| 1.3 | -19.35 | -16.04 | -21.90 |
| 1.4 | -20.41 | -16.94 | -23.08 |
| 1.5 | -21.47 | -17.82 | -24.25 |
| 1.6 | -22.52 | -18.70 | -25.41 |
| 1.7 | -23.57 | -19.58 | -26.56 |
| 1.8 | -24.61 | – | -27.72 |
| 1.9 | – | – | -28.87 |

## Figure 37: Active Termination Characteristics



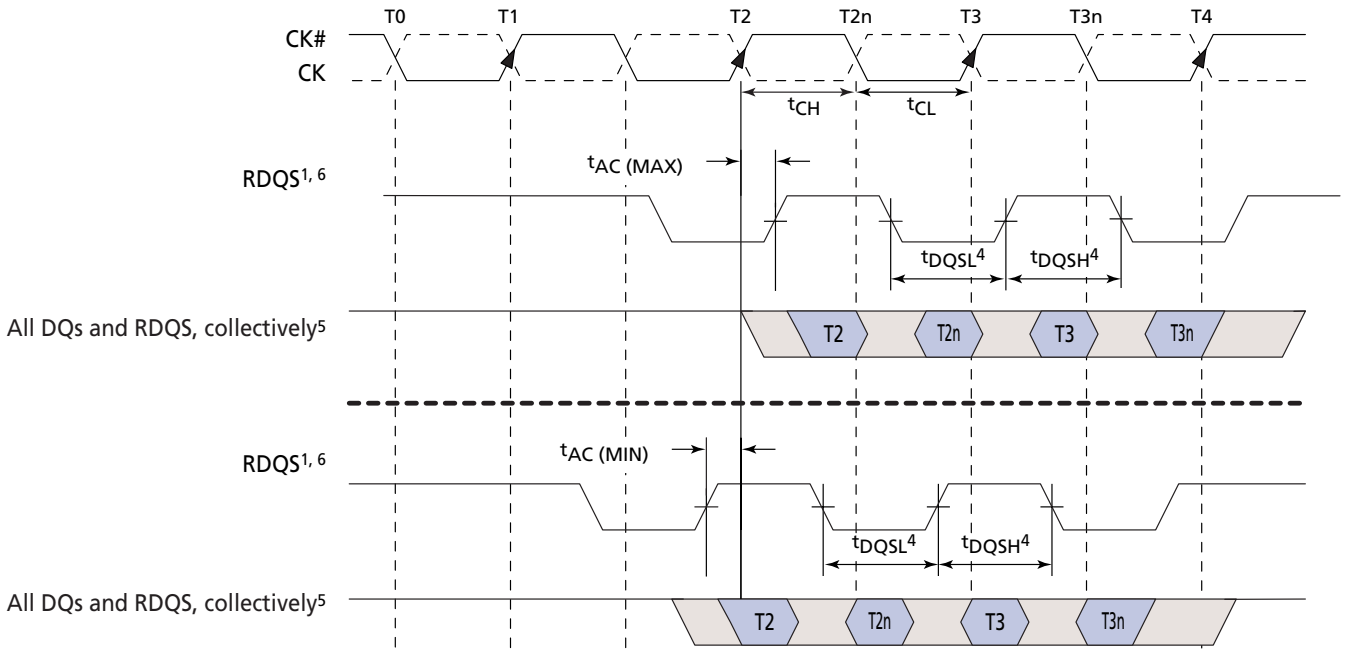

## Figure 38: Data Output Timing – tDQSQ, tQH, and Data Valid Window




NOTE:

1. tDQSQ represents the skew between the eight DQ lines and the respective RDQS pin.
2. tDQSQ is derived at each RDQS edge and is not cumulative over time and begins with first DQ transition and ends with the last valid transition of DQ.
3. tAC is shown in the nominal case.
4. tDQHP is the lesser of tDQSL or tDQSH strobe transition collectively when a bank is active.
5. The data valid window is derived for each RDQS transitions and is defined by tDV.
6. There are four RDQS pins for this device with RDQS0 in relation to DQ(0–7), RDQS1 in relation DQ(8–15), RDQS2 in relation to DQ(16–24), and RDQS3 in relation to DQ(25–31).
7. This diagram only represents one of the four byte lanes.

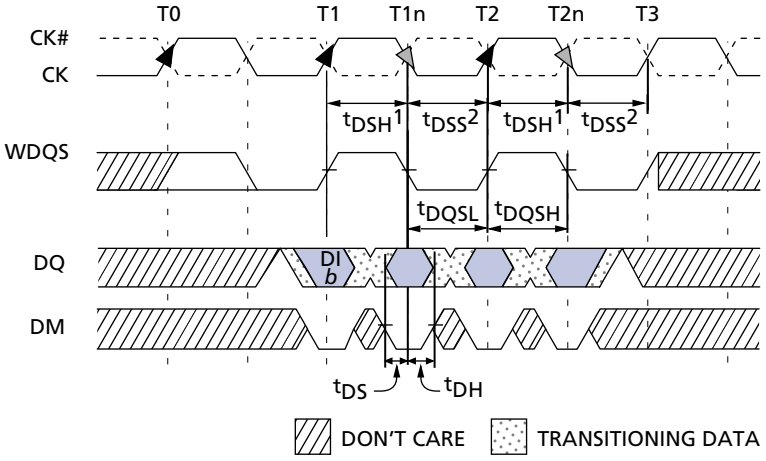
## Figure 39: Data Output Timing – $^{t}$AC




NOTE:

1. $^{t}$AC represents the relationship between DQ, RDQS to the crossing of CK and CK#.

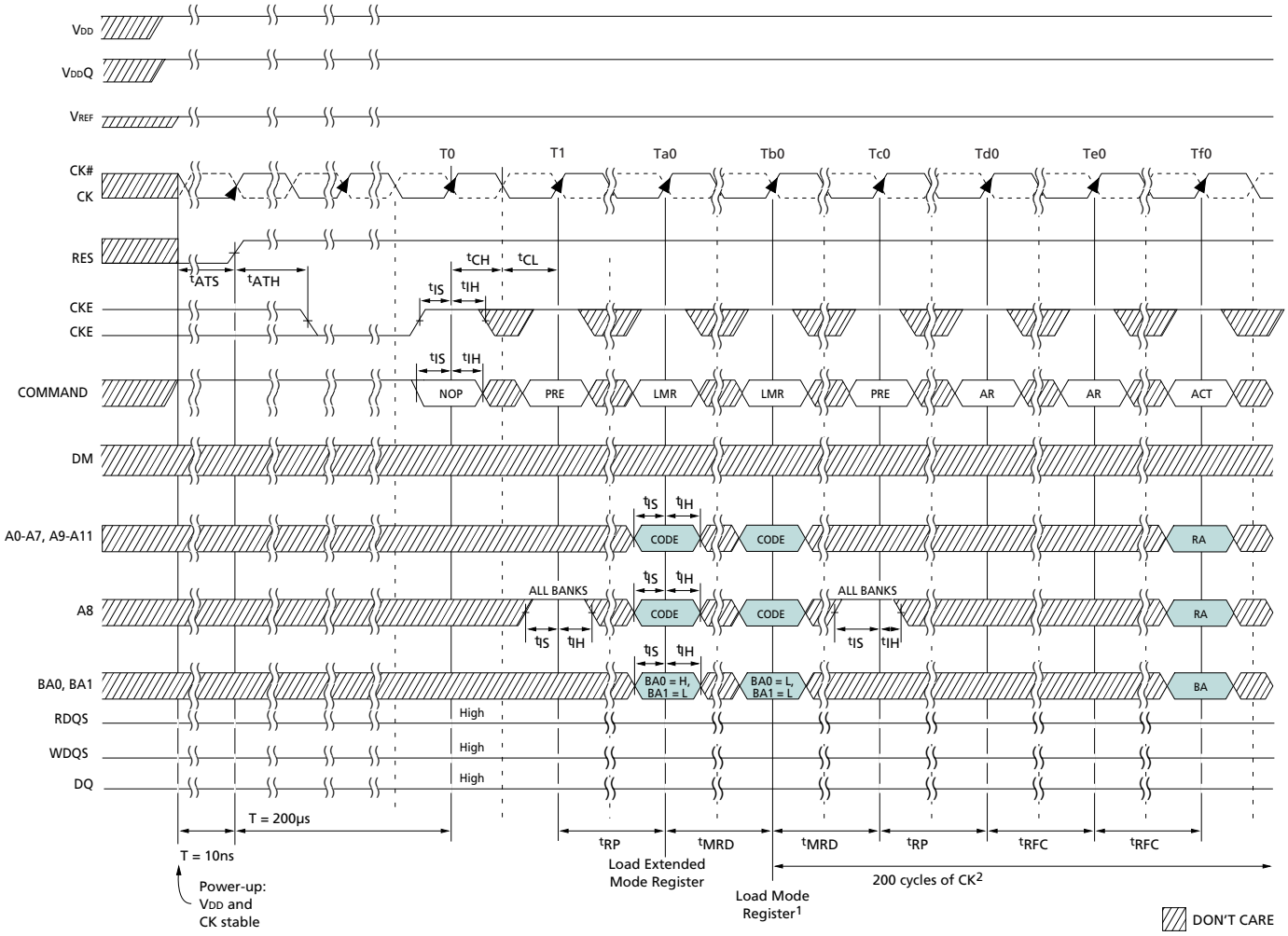
## Figure 40: Data Input Timing




NOTE:

1. $^{t}$DSH (MIN) generally occurs during $^{t}$DQSS (MIN).
2. $^{t}$DSS (MIN) generally occurs during $^{t}$DQSS (MAX).

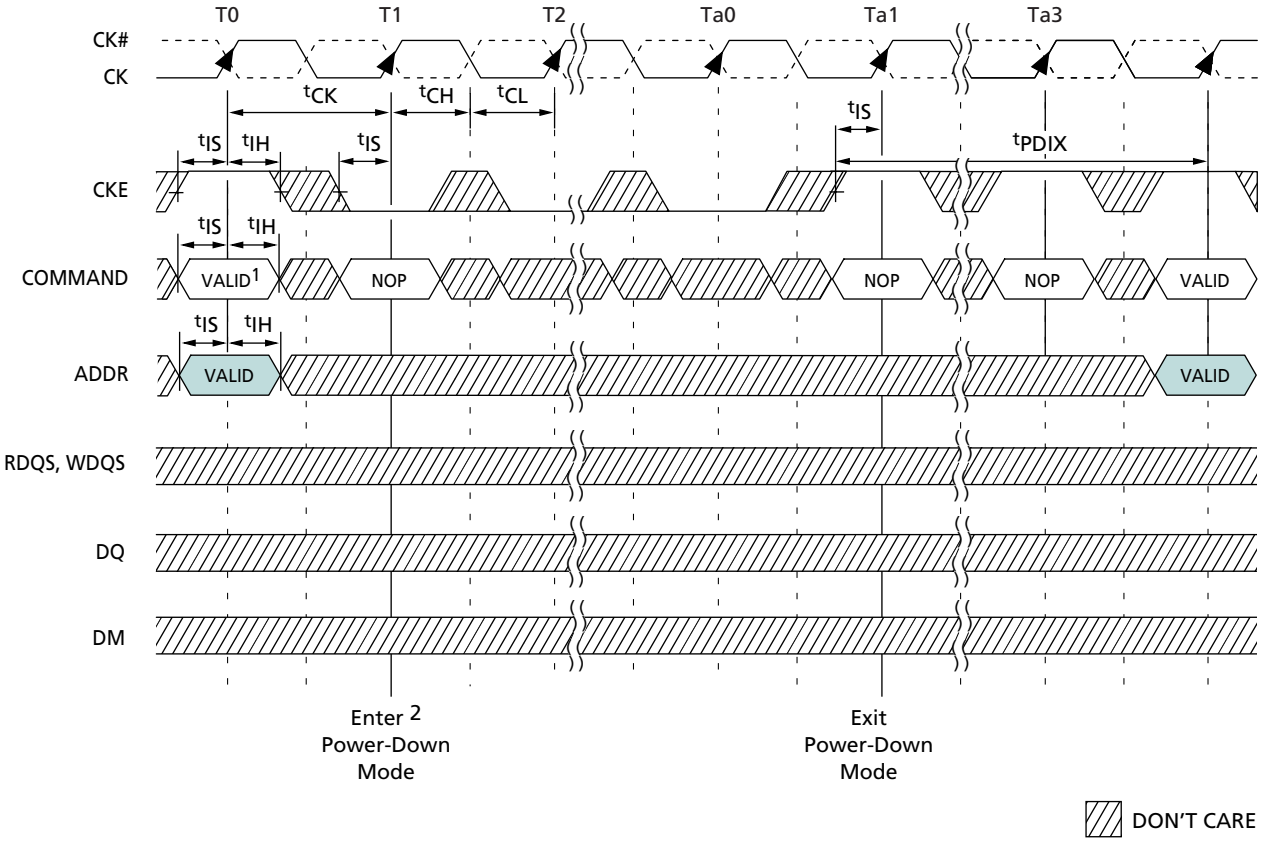
## Figure 41: Initialize and Load Mode Registers




NOTE:

1. A DLL reset with A8 = H is required after enabling the DLL.
2. $^{t}$MRD is required before any command can be applied, and 200 cycles of CK are required before a READ command can be issued.
3. The two AUTO REFRESH commands at Tc0 and Td0 may be applied after the LOAD MODE REGISTER command at Ta0.
4. PRE = PRECHARGE command, LMR = LOAD MODE REGISTER command, AR = AUTO REFRESH command, ACT = ACTIVE command, RA = Row Address, BA = Bank Address.
5. DQ[0:7] will be driving the vendor ID and die rev ID when the RES pin is in a logic low state prior to the first rising edge of RES during power-up.

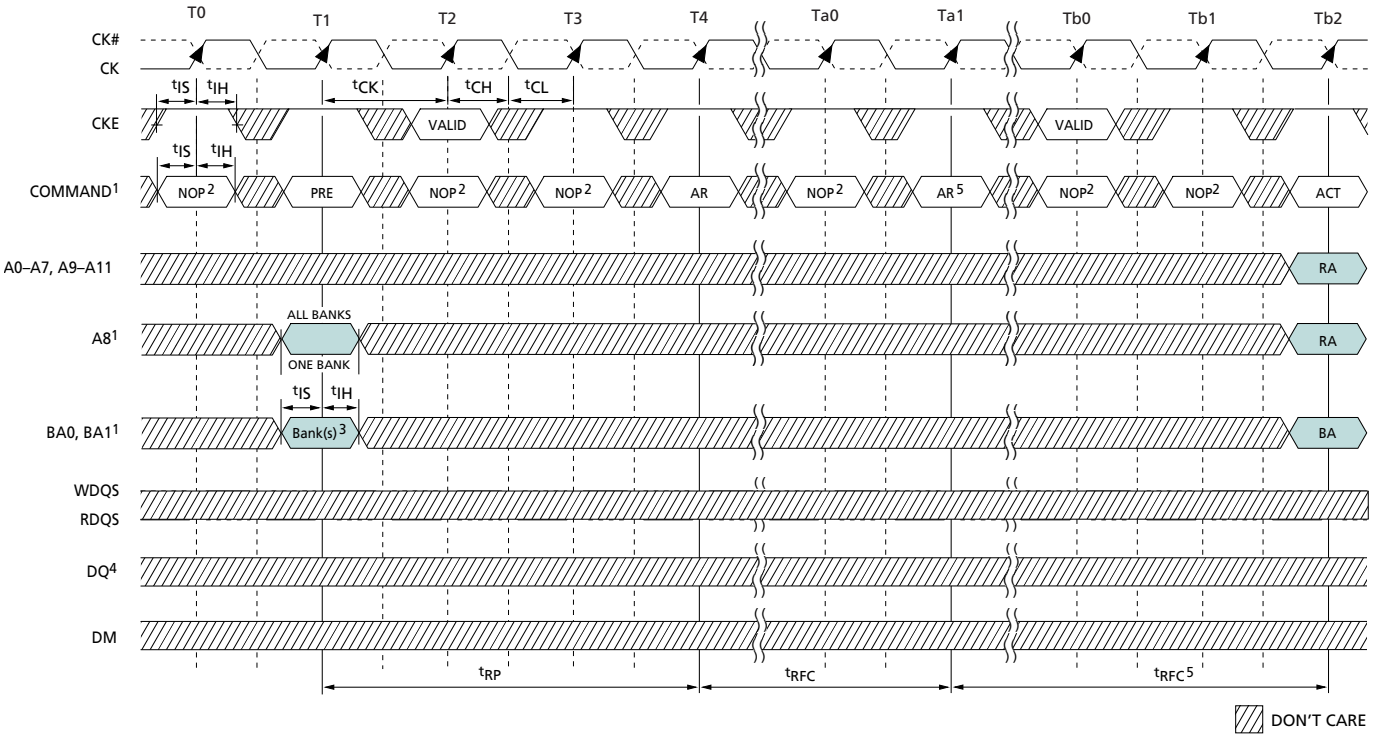
## Figure 42: Power-Down Mode




NOTE:

1. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down. If this command is an ACTIVE (or if at least one row is already active), then the power-down mode shown is active power-down.
2. No column accesses are allowed to be in progress at the time power-down is entered.

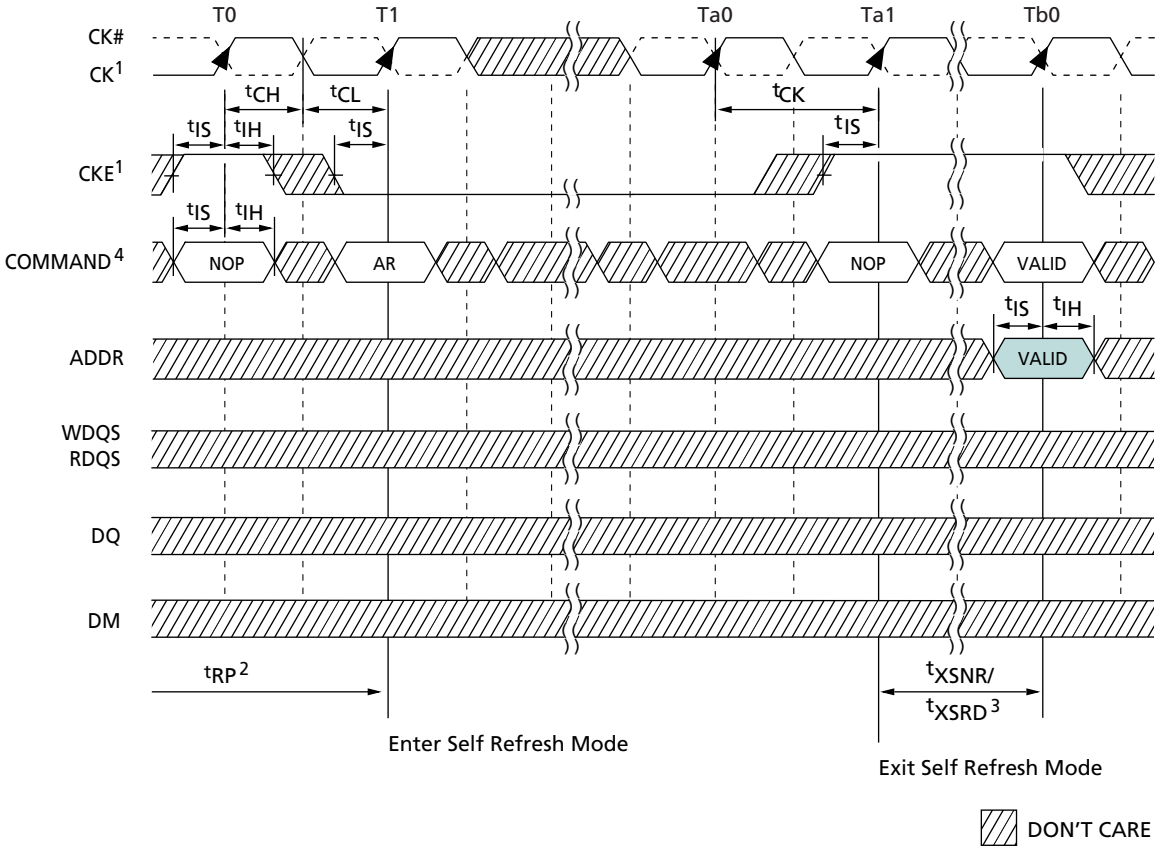
## Figure 43: Auto Refresh Mode




NOTE:

1. PRE = PRECHARGE, ACT = ACTIVE, AR = AUTO REFRESH, RA = Row Address, BA = Bank Address.
2. NOP commands are shown for ease of illustration; other valid commands may be possible at these times.
3. "Don't Care" if A8 is HIGH at this point; A8 must be HIGH if more than one bank is active (i.e., must precharge all active banks).
4. DM, DQ, and DQS signals are all "Don't Care"/High-Z for operations shown.
5. The second AUTO REFRESH is not required and is only shown as an example of two back-to-back AUTO REFRESH commands.

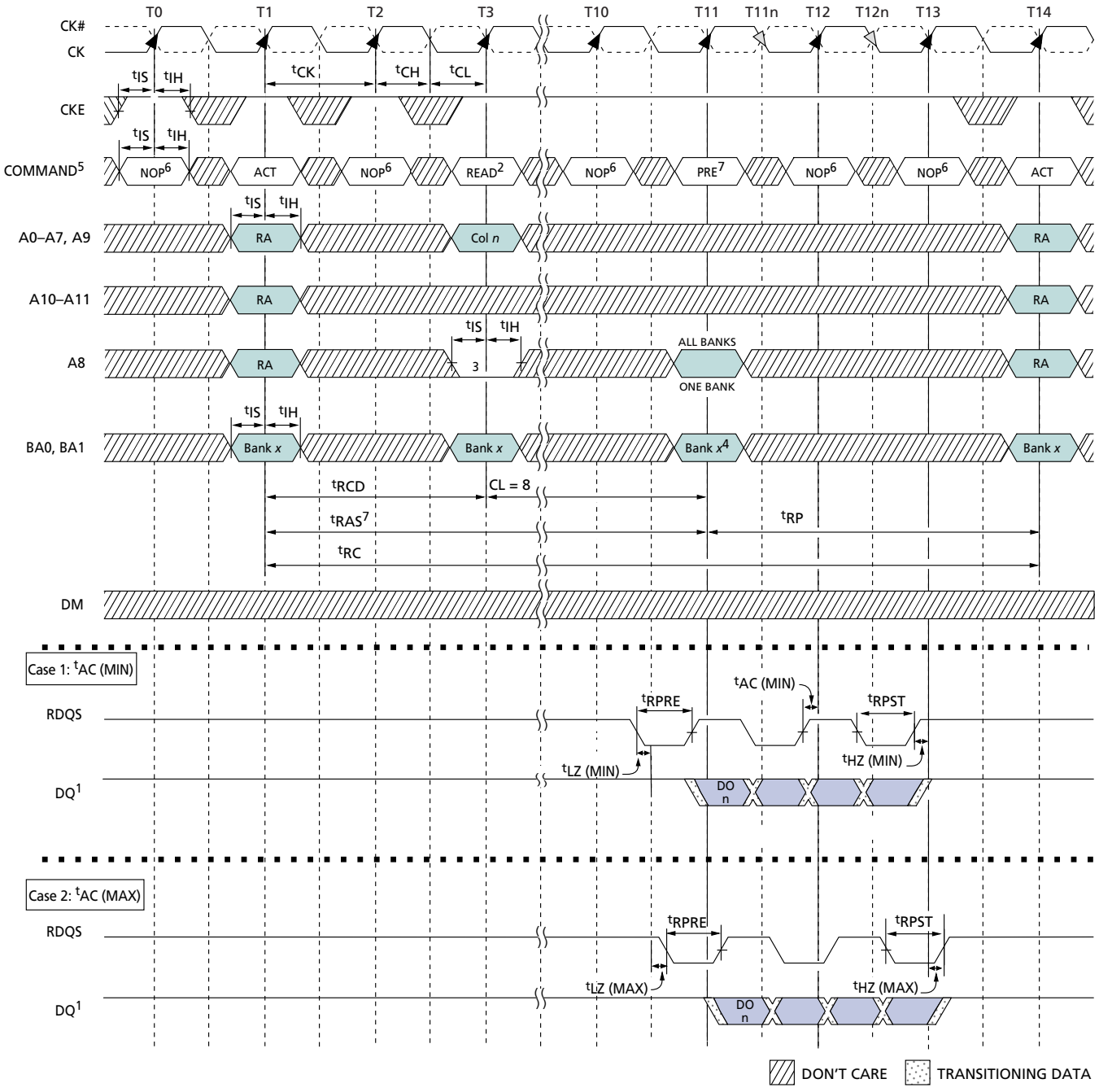
## Figure 44: Self Refresh Mode




NOTE:

1. Clock must be stable before exiting self refresh mode.
2. Device must be in the all banks idle state prior to entering self refresh mode.
3. $^{t}$XSNR is required before any non-READ command can be applied, and $^{t}$XSRD (200 cycles of CK) is required before a READ command can be applied.
4. AR = AUTO REFRESH command.

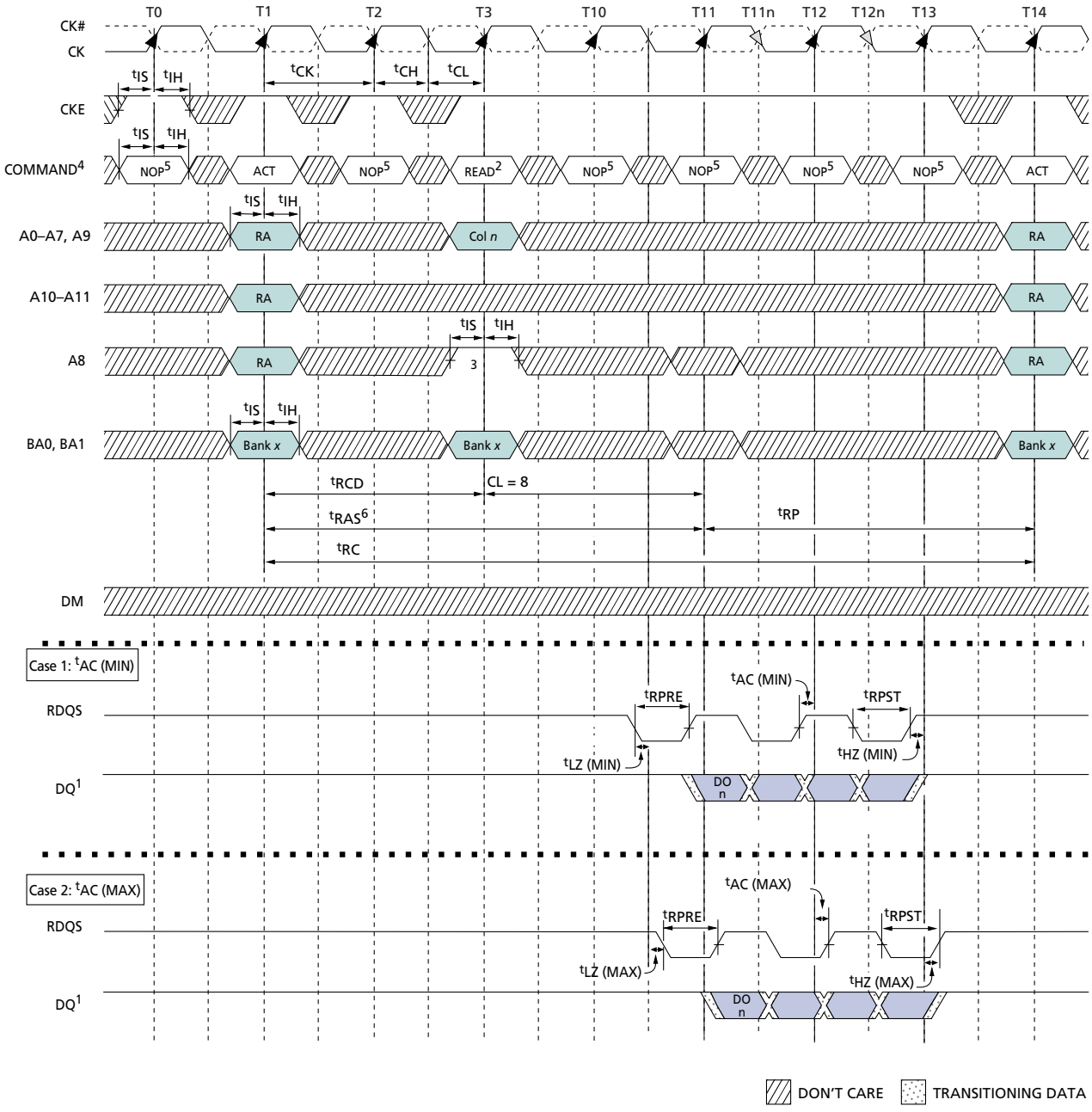
## Figure 45: Bank Read Without Auto Precharge




NOTE:

1. DO *n* = data-out from column *n*; subsequent elements are provided in the programmed order.
2. Burst length = 4 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A8 is HIGH at T5.
5. PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. The PRECHARGE command can be applied as early as T5 if $^{t}$RAS minimum is met.

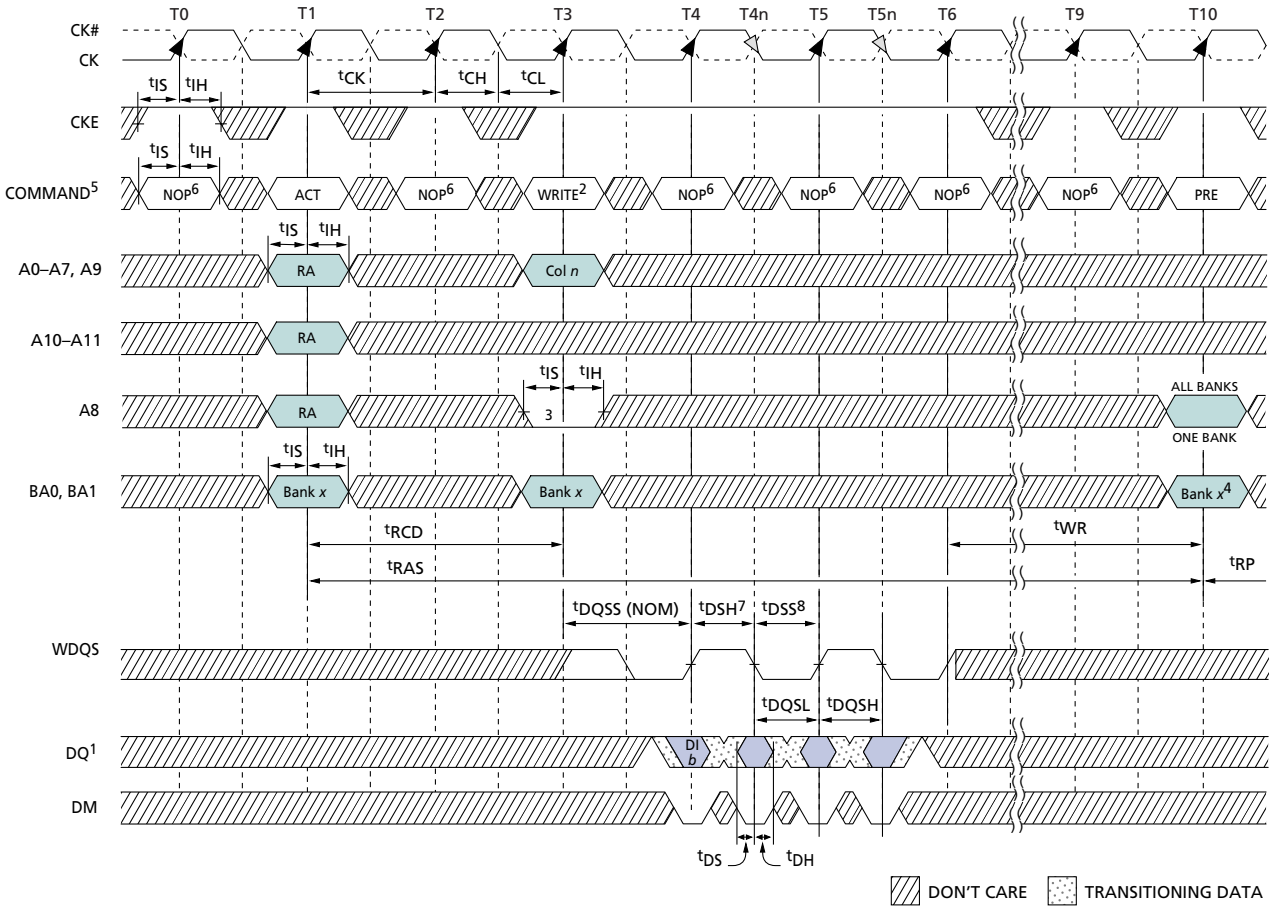
## Figure 46: Bank Read with Auto Precharge




NOTE:

1. DO *n* = data-out from column *n*; subsequent elements are provided in the programmed order.
2. Burst length = 4 in the case shown.
3. Enable auto precharge.
4. ACT = ACTIVE, RA = Row Address, BA = Bank Address.
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
6. The READ command can be applied even if $^{t}$RAS (MIN) has not been met by T5; the device will hold off the PRECHARGE command until $^{t}$RAS (MIN) is met.

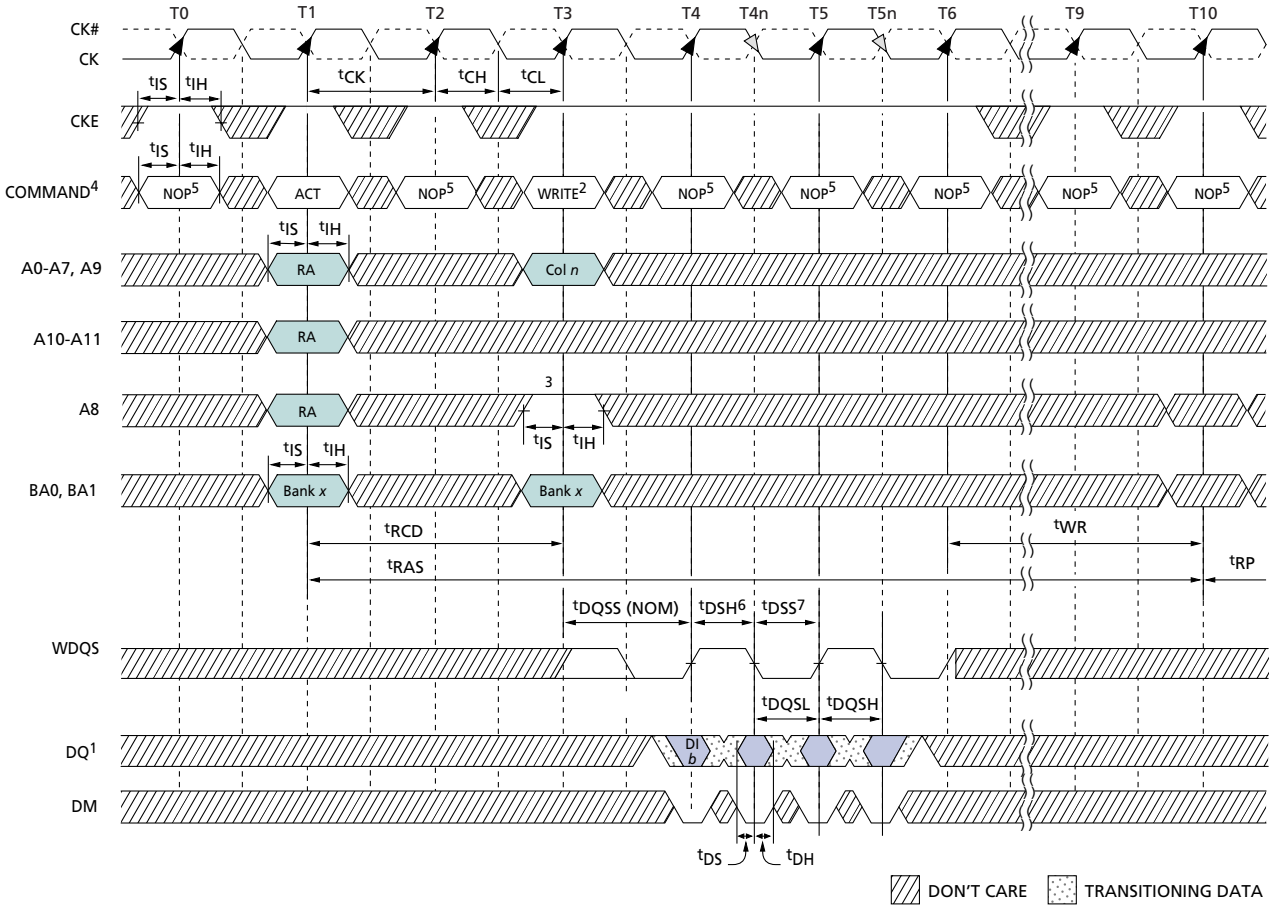
## Figure 47: Bank Write Without Auto Precharge




NOTE:

1. DI *n* = data-in to column *n*; subsequent elements are provided in the specified order.
2. Burst length = 4 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A8 is HIGH at T3.
5. PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. $^{t}$DSH is applicable during $^{t}$DQSS (MIN) and is referenced from CK T4 or T5.
8. $^{t}$DSS is applicable during $^{t}$DQSS (MAX) and is referenced from CK T5 or T6.
9. WRITE latency is set to one.

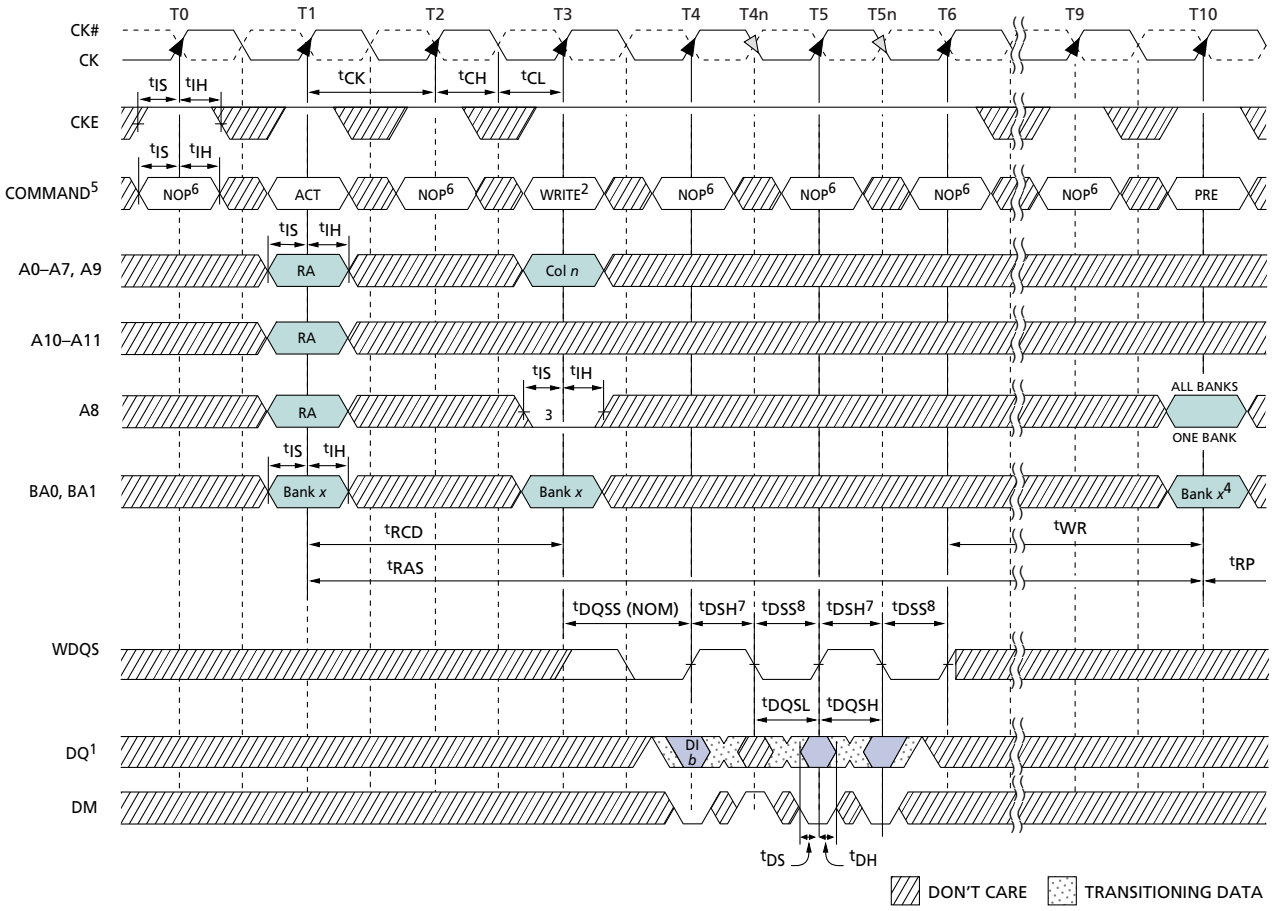
## Figure 48: Bank Write with Auto Precharge




NOTE:

1. DI *n* = data-in to column *n*; subsequent elements are provided in the specified order.
2. Burst length = 4 in the case shown.
3. Enable auto precharge.
4. ACT = ACTIVE, RA = Row Address, BA = Bank Address
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
6. $^{t}$DSH is applicable during $^{t}$DQSS (MIN) and is referenced from CK T4 or T5.
7. $^{t}$DSS is applicable during $^{t}$DQSS (MAX) and is referenced from CK T5 or T6.
8. WRITE latency is set to one.

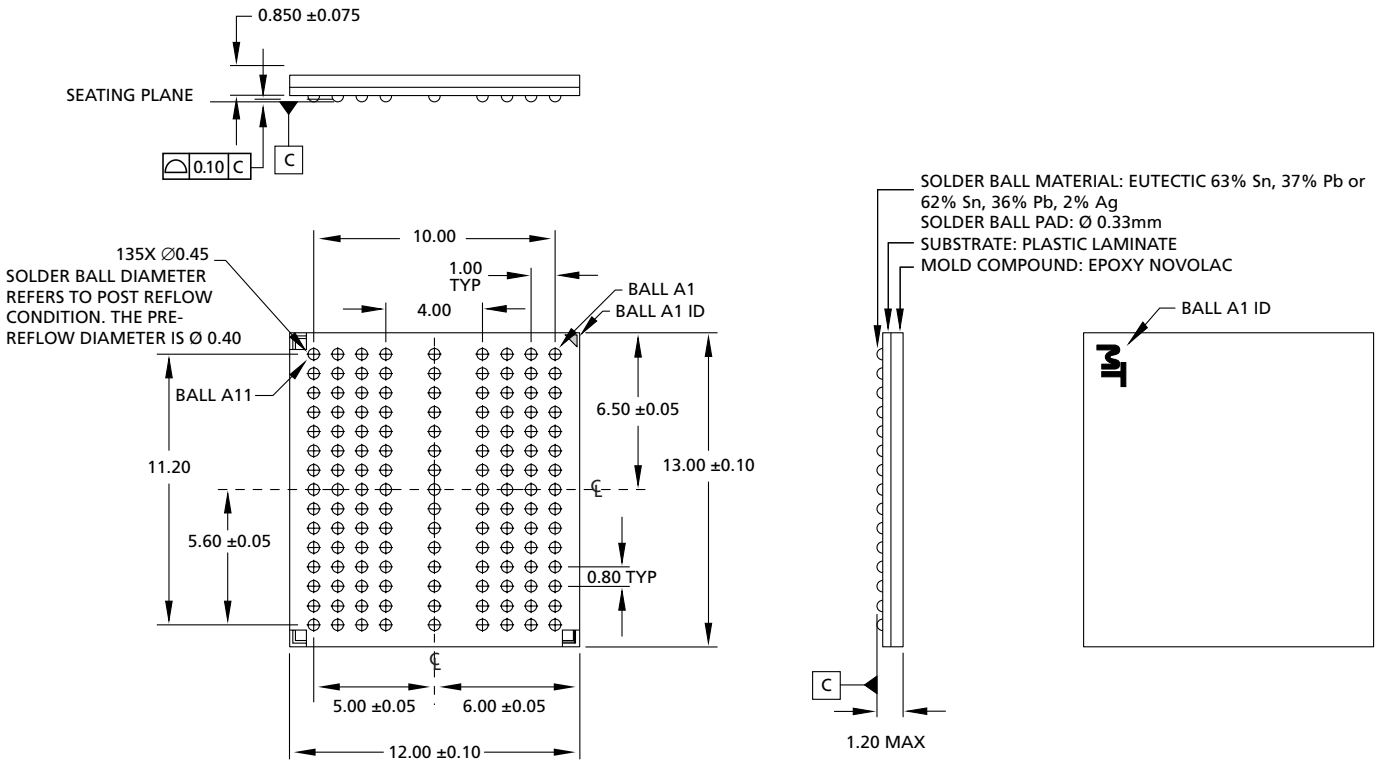
## Figure 49: Write – DM Operation




NOTE:

1. DI *n* = data-in to column *n*; subsequent elements are provided in the specified order.
2. Burst length = 4 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A8 is HIGH at T3.
5. PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. $^{t}$DSH is applicable during $^{t}$DQSS (MIN) and is referenced from CK T4 or T5.
8. t$^{t}$DSS is applicable during $^{t}$DQSS (MAX) and is referenced from CK T5 or T6.
9. $^{t}$DS and $^{t}$DH are referenced to WDQS.
10. WRITE latency is set to one.

## Figure 50: 135-Ball FBGA




NOTE:

All dimensions are in millimeters.

## Data Sheet Designation

**Advance**: This datasheet contains initial descriptions of products still under development.

**8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900**
**E-mail: prodmktg@micron.com, Internet: http://www.micron.com, Customer Comment Line: 800-932-4992**