Preliminary Data Sheet
January 1992

AT&T Microelectronics

ATT7C108
ATT7C109

High-Speed CMOS SRAM
1 Mbit (128 Kbit x 8), Common I/O

Features

- High speed —15 ns maximum access time
- Automatic powerdown during long cycles
- Easy memory expansion with $\overline{CE1}$, CE2, and $\overline{OE}$ options
- Advanced CMOS technology
- TTL-compatible inputs and outputs
- Data retention at 2 V for battery backup operation
- Low-power operation
  - — Active: 880 mW maximum at 25 ns
  - — Standby (typical): 110 mW (TTL inputs); 14 mW (CMOS inputs)
- Package styles available:
  - — 32-pin, plastic DIP
  - — 32-pin, plastic SOJ

Description

The ATT7C108 and ATT7C109 devices are high-performance, low-power CMOS static RAMs organized as 131,072 words by 8 bits per word. The eight data-in and data-out signals share I/O pins. The ATT7C108 and 109 differ in that the ATT7C108 has a single chip enable ($\overline{CE}$), while the ATT7C109 has two chip enables ($\overline{CE1}$ and CE2). Both devices have an active low output enable ($\overline{OE}$), and are available in three speeds with maximum access times from 15 ns to 25 ns.

Inputs and outputs are TTL compatible. Operation is from a single 5 V power supply. Power consumption is 880 mW (maximum) at 25 ns. Dissipation drops to 110 mW (typical) for both the ATT7C108 and ATT7C109 when the memory is deselected (enable is high).

Two standby modes are available. Powerdown circuitry reduces power consumption automatically when the memory is deselected, or during read or write cycles that are longer than the access time. In addition, data can be retained in inactive storage with a supply voltage as low as 2 V. The ATT7C108 and ATT7C109 consume only 1.5 mW (typical) at 3 V, allowing effective battery backup operation.

Pin Information

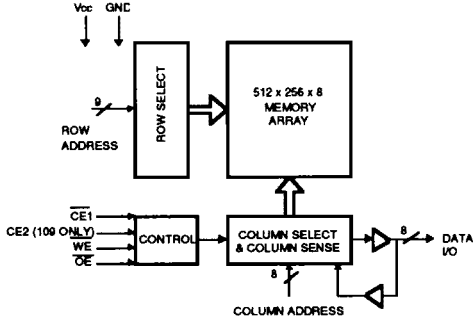


Figure 1. Block Diagram

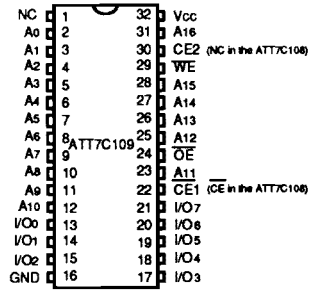


Figure 2. Pin Diagram

Table 1. Pin Descriptions

Pin	Function
A0—A16	Address Inputs
I/O0—I/O7	Data Input/Output
$\overline{CE1}$, CE2	Chip Enables
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
GND	Ground
Vcc	+5 V Supply
NC	No Connection

Functional Description

The ATT7C108 and ATT7C109 devices provide asynchronous (unclocked) operation with matching access and cycle times. One chip enable (active-low) on the ATT7C108 and two chip enables (one active-low and one active-high) on the ATT7C109, plus a 3-state I/O bus with a separate output-enable control, simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A0 through A16. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ 1 and $\overline{OE}$ low and CE2 (ATT7C109 only) high while $\overline{WE}$ remains high. The data in the addressed memory location then appears on the data I/O pins within one access time.

The eight input/output pins (I/O0 through I/O7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ 1 high or CE2 low), when the outputs are disabled ($\overline{OE}$ high), or during a write operation ($\overline{CE}$ 1 low, CE2 high, and $\overline{WE}$ low).

Either one of the CE and $\overline{WE}$ signals can be used to terminate a write operation. The data-in and data-out signals have the same polarity.

Latch-up and static discharge protection are provided on-chip. The ATT7C108 and ATT7C109 devices can withstand an injection current of up to 200 mA on any pin without damage.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those indicated in the operational sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	–65	150	°C
Operating Ambient Temperature	T_A	0	70	°C
Supply Voltage with Respect to Ground	V_{CC}	–0.5	7.0	V
Input Signal with Respect to Ground	—	–3.0	7.0	V
Signal Applied to High-impedance Output	—	–3.0	7.0	V
Output Current into Low Outputs	—	—	25	mA
Latch-up Current	—	>200	—	mA

Truth Table

Table 2. Truth Table for the ATT7C108 and ATT7C109

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	I/O0—I/O7	Mode	Power
H	X	X	X	High Z	Powerdown	Standby (I_{CC2} and I_{CC3})
X	L	X	X	High Z	Powerdown	Standby (I_{CC2} and I_{CC3})
L	H	H	L	Data Out	Read	Active (I_{CC1})
L	H	L	X	Data In	Write	Active (I_{CC1})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC1})

Handling Precautions

The ATT7C108 and ATT7C109 devices include internal circuitry designed to protect the chips from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use to avoid exposure to excessive electrical stress.

Recommended Operating Conditions

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0 °C to 70 °C	4.5 V ≤ Vcc ≤ 5.5 V
Data Retention, Commercial	0 °C to 70 °C	2.0 V ≤ Vcc ≤ 5.5 V

Electrical Characteristics

Over all recommended operating conditions.

Table 3. General Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage:						
High	V_{OH}	I_{OH} = –4.0 mA, Vcc = 4.5 V	2.4	—	—	V
Low	V_{OL}	I_{OL} = 8.0 mA	—	—	0.4	V
Input Voltage:						
High	V_{IH}	—	2.2	—	Vcc + 0.3	V
Low[1]	V_{IL}	—	–3.0	—	0.8	V
Input Current	I_{IX}	GND ≤ V_{IN} ≤ Vcc	–10	—	10	µA
Output Leakage Current	I_{OZ}	GND ≤ V_{OUT} ≤ Vcc, $\overline{CE}$ = Vcc	–10	—	10	µA
Output Short Current	I_{OS}	V_{OUT} = GND, Vcc = Max[2]	—	—	–350	mA
Vcc Current:						
TTL Inactive[3]	I_{CC2}	—	—	20	50	mA
CMOS Standby[4]	I_{CC3}	—	—	2.5	30	mA
Data Retention Mode[5]	I_{CC4}	Vcc = 3.0 V	—	5	8	mA
Capacitance (SOJ Package):[6]						
Inputs (A0—A16)	C_I	Ambient Temp = 25 °C, Vcc = 5.0 V	—	—	6	pF
Inputs ($\overline{CE1}$, CE2		Test Frequency = 1 MHz[7]	—	—	8	pF
$\overline{WE}$, $\overline{OE}$)	C_I					
Outputs (I/O0—I/O7)	C_O		—	—	8	pF

1. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.
2. Duration of the output short circuit should not exceed 30 seconds.
3. Tested with outputs open and all address and data inputs changing at the maximum read cycle. The device is continuously disabled, i.e., $\overline{CE}$ 1 ≥ V_{IH}, CE2 ≤ V_{IL}, max Vcc.
4. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ 1 = Vcc, CE2 = GND. Input levels are within 0.2 V of Vcc or ground, max Vcc.
5. Data retention operation requires that Vcc never drop below 2.0 V. $\overline{CE}$ 1 must be ≥ Vcc – 0.2 V. For the ATT7C108 and ATT7C109, all other inputs meet V_{IN} ≤ 0.2 V or V_{IN} ≥ Vcc – 0.2 V to ensure full powerdown.
6. Consult AT&T regarding DIP package capacitance.
7. These parameters are not 100% tested.

Table 4. Electrical Characteristics By Speed

Parameter	Symbol	Test Condition	Speed			Unit
			25	20	15	ns
Max Vcc Current, Active	I_{CC1}	*	160	225	270	mA

* Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}$ 1 or $\overline{WE}$ 2 ≤ V_{IL}. Input pulse levels are within 0 V to 3 V.
Max Icc shown applies over the active operating temperature range.

Timing Characteristics

Table 5. Read Cycle [1, 2, 3, 4, 5] (See Figures 3 and 4.)

Over all Recommended Operating Conditions; all measurements in ns.

Symbol	Parameter	Speed					
		25		20		15	
		Min	Max	Min	Max	Min	Max
tADVADX, tCEACEI	Read Cycle Time	25	—	20	—	15	—
tADVDOV	Address Valid to Output Valid[6, 7]	—	25	—	20	—	15
tADVDOX	Address Valid to Output Change	3	—	3	—	3	—
tCEADOV	Chip Enable Active to Output Valid[6, 8]	—	25	—	20	—	15
tCEADOZ	Chip Enable Active to Output Low-Z[9, 10]	3	—	3	—	3	—
tCEIDOZ	Chip Enable Inactive to Data Output High-Z[9, 10]	—	10	—	8	—	8
tOELDOV	Output Enable Low to Data Output Valid	—	12	—	10	—	8
tOELDOZ	Output Enable Low to Low-Z[9, 10]	0	—	0	—	0	—
tOEHDOZ	Output Enable High to Output High-Z[9, 10]	—	10	—	8	—	5
tCEAICH	Chip Enable Active to Powerup[11, 12]	0	—	0	—	0	—
tICHICL	Powerup to Powerdown[11, 12]	—	30	—	25	—	20
tCEIVCL	Chip Enable Inactive to Data Retention[11]	0	—	0	—	0	—
tVCHCEL	End Data Retention to Beginning of Read Cycle[11]	25	—	20	—	15	—

1. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Figure 8), and input pulse levels of 0 to 3.0 V (Figure 9).
2. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tADVWEH (Table 6) is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
3. All address timings are referenced from the last valid address line to the first transitioning address line.
4. $\overline{CE}$ 1 or CE2 must be inactive or $\overline{WE}$ must be high during address transitions.
5. This product is a very high-speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the Vcc and ground planes directly up to the contactor fingers. A 0.01 µF high-frequency capacitor is also required between Vcc and ground. To avoid signal reflections, proper terminations must be used.
6. $\overline{WE}$ is high for the read cycle.
7. The chip is continuously selected ($\overline{CE}$ 1 low and CE2 high).
8. All address lines are valid prior to or coincident with the $\overline{CE}$ 1 and CE2 transition to active.
9. At any given temperature and voltage condition, output-disable time is less than output-enable time for any given device.
10. Transition is measured ±200 mV from steady-state voltage with specified loading in Figure 8. This parameter is sampled and not 100% tested.
11. These parameters are not 100% tested.
12. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) transition of $\overline{CE}$ 1 and CE2 (ATT7C109 only) to an active state, (2) transition on any address line ($\overline{CE}$ 1, CE2 active), or (3) transition on any data line ($\overline{CE}$ 1, CE2 or $\overline{WE}$ active). The device automatically powers down from I_{CC2} to I_{CC1} after tICHICL has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, not on chip-enable pulse width.

Timing Characteristics (continued)

Table 6. Write Cycle [1, 2, 3, 4, 5, 8] (See Figures 6 and 7.)

Over all Recommended Operating Conditions; all measurements in ns.

Symbol	Parameter	Speed					
		25		20		15	
		Min	Max	Min	Max	Min	Max
tADVADX, tCEACEI	Write Cycle Time	20	—	20	—	15	—
tADVCEA	Address Set-up to Write Start	0	—	0	—	0	—
tADVCEI	Address Set-up to End of Write	15	—	15	—	12	—
tCEAWEH, tCEACEI	Chip Enable Active to End of Write	15	—	15	—	12	—
tADVWEX	Address Valid to Beginning of Write	0	—	0	—	0	—
tADVWEH, tADVCEI	Address Valid to End of Write	15	—	15	—	12	—
tWEHADX, tCEIADX	End of Write to Address Change	0	—	0	—	0	—
tWELWEH, tWELCEH	Write Enable Pulse Width	15	—	15	—	12	—
tDIVWEH, tDIVCEI	Data Valid to End of Write	10	—	10	—	7	—
tWEHDIX, tCEIDIX	End of Write to Data Change	0	—	0	—	0	—
tWEHDOZ	Write Enable High to Output Low-Z[6, 7]	0	—	0	—	0	—
tWELDOZ	Write Enable Low to Output High-Z[6, 7]	—	7	—	7	—	5

1. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (see Figure 8), and input pulse levels of 0 V to 3.0 V (see Figure 9).
2. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tADVWEH is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
3. All address timings are referenced from the last valid address line to the first transitioning address line.
4. $\overline{CE}$ 1 or CE2 must be inactive or $\overline{WE}$ must be high during address transitions.
5. This product is a very high-speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the Vcc and ground planes directly up to the contactor fingers. A 0.01 µF high-frequency capacitor is also required between Vcc and ground. To avoid signal reflections, proper terminations must be used.
6. At any given temperature and voltage condition, output-disable time is less than output-enable time for any given device.
7. Transition is measured ±200 mV from steady state voltage with specified loading in Figure 8. This parameter is sampled and not 100% tested.
8. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ 1 and CE 2 active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first. If $\overline{WE}$ goes low before or concurrent with the later of $\overline{CE}$ 1 and CE2 going active, the output remains in a high-impedance state. If $\overline{CE}$ 1 and CE2 go inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high-impedance state.

Timing Characteristics (continued)

Timing Diagrams

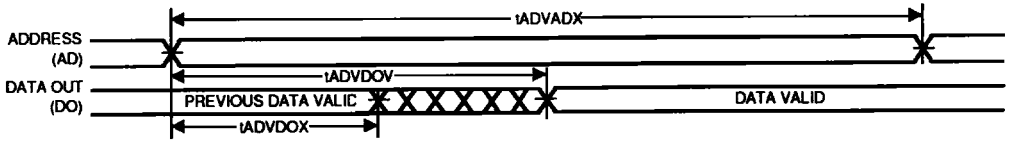


Figure 3. Read Cycle — Address Controlled
(See Table 4, Notes 6 and 7.)

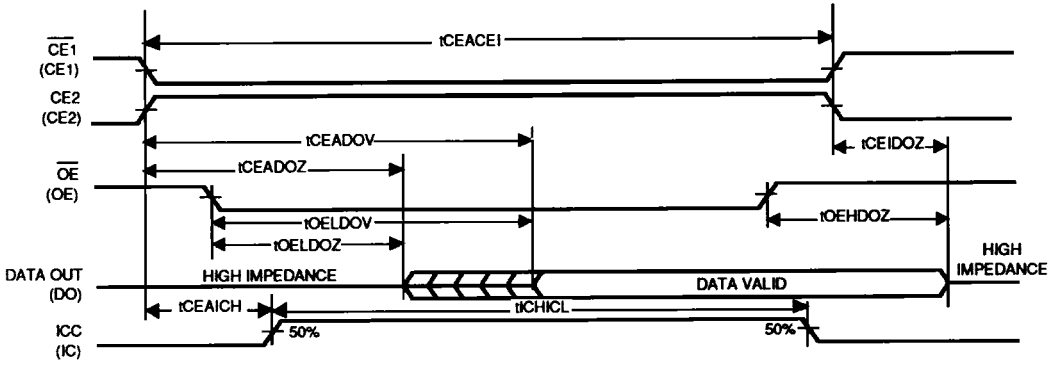


Figure 4. Read Cycle — $\overline{CE}$ / $\overline{OE}$ Controlled
(See Table 4, Notes 6 and 8.)

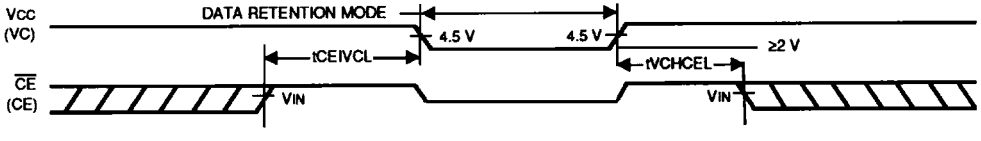


Figure 5. Data Retention

Timing Characteristics (continued)

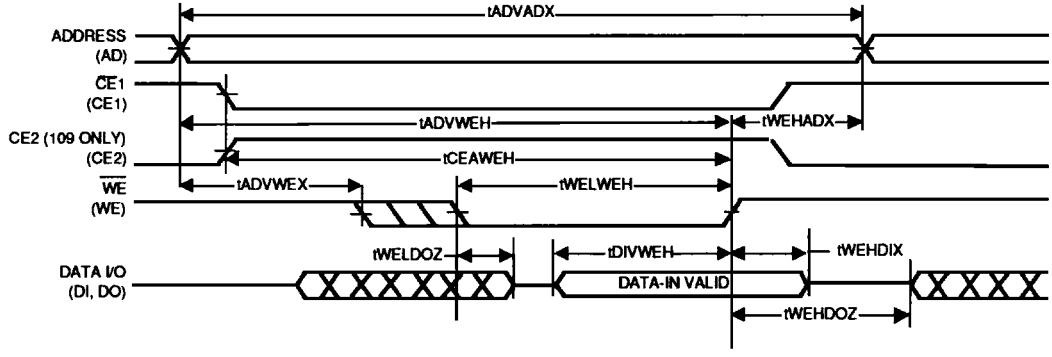


Figure 6. Write Cycle — $\overline{WE}$ Controlled ($\overline{OE}$ Low During Write)
(See Table 5, Note 12; and Table 6.)

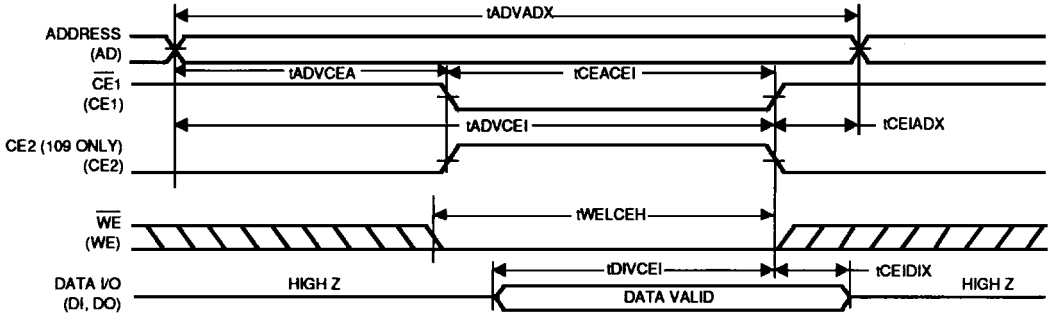
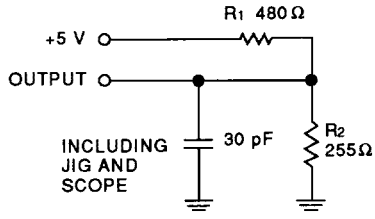
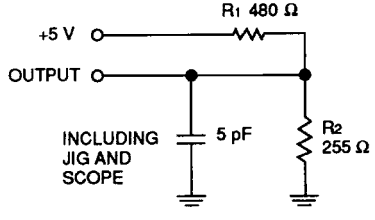


Figure 7. Write Cycle — $\overline{CE}$ Controlled
(See Table 5, Note 12; and Table 6.)

Timing Characteristics (continued)



A. Output Loading for I_{OL} and I_{OH} +30 pF



B. Output Loading for I_{OL} and I_{OH} +5 pF

Figure 8. Test Loads

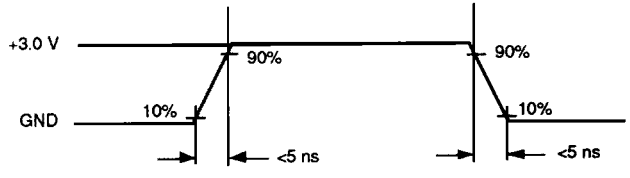
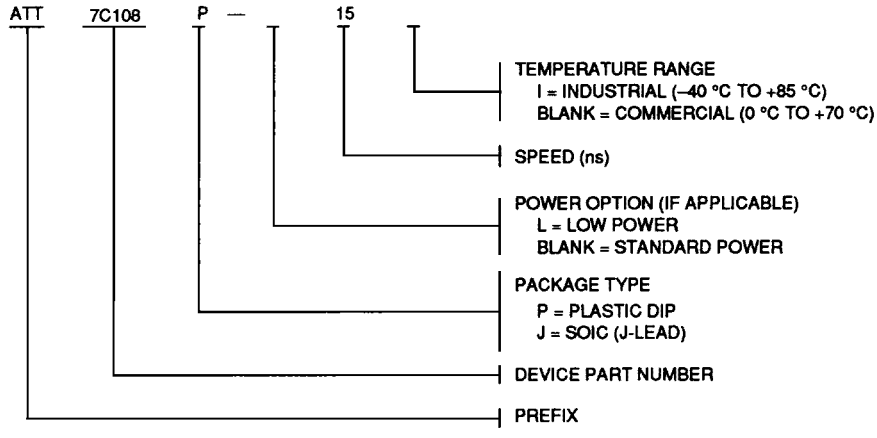


Figure 9. Transition Times

Ordering Information



ATT7C108

Operating Range 0 °C to 70 °C

Package Style	Performance Speed		
	25 ns	20 ns	15 ns
32-Pin, Plastic DIP	ATT7C108P–25	ATT7C108P–20	ATT7C108P–15
32-Pin, Plastic SOJ	ATT7C108J–25	ATT7C108J–20	ATT7C108J–15

ATT7C109

Operating Range 0 °C to 70 °C

Package Style	Performance Speed		
	25 ns	20 ns	15 ns
32-Pin, Plastic DIP	ATT7C109P–25	ATT7C109P–20	ATT7C109P–15
32-Pin, Plastic SOJ	ATT7C109J–25	ATT7C109J–20	ATT7C109J–15