PaceMips™ PR4000PC CPU

ADVANCE INFORMATION

64-BIT THIRD GENERATION RISC PROCESSOR WITH MMU, FPA, & PRIMARY CACHES

FEATURES

- 64-bit Superpipelined Third Generation RISC Microprocessor:
  - Highly integrated CPU with Integer unit, FPA, MMU, I & D caches
  - Balanced integer & floating point performance
  - Exploits 2-level instruction level parallelism
  - No issue restrictions on the instructions used
- User mode binary compatibility with PR3000A/ PR3010A, PR3400, PIMM, and PIPER
- Integer unit:
  - 32 entry 64-bit wide register file
  - 64-bit ALU
  - Dedicated Integer Multiplier/Divider
- 8KBytes of on-chip Instruction cache & 8KBytes of on-chip Data cache with parity protection
- Superpipelined FPA:
  - 32/16 entry 32/64 bit register file in a 32-bit mode
  - 32 entry 64-bit register file in 64-bit mode
  - Supports single & double precision
  - Conforms to ANSI/ IEEE Standard 754-1985
- Memory Management Unit
  - 48 entry TLB for fast virtual-to-physical address translation
  - Software managed control registers
  - Programmable page sizes from 4KBytes to16MBytes
  - Total physical memory space of 64GBytes
- Very high system performance
- Comprehensive system development support
- Produced with PACE III™ Technology
- Package: 179-pin Ceramic Pin Grid Array

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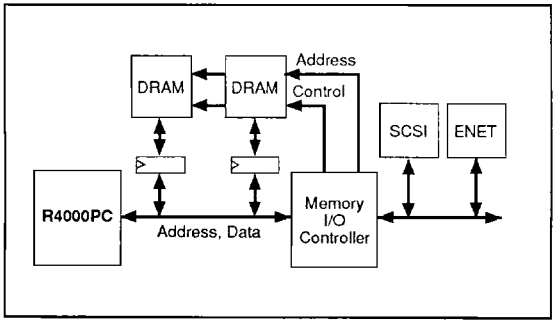
DESCRIPTION

The PaceMips PR4000PC is the third generation 64-bit superpipelined RISC processor designed for extremely high-performance applications. The high level of integration of PR4000P, that includes MMU, FPA, 8 KBytes of instruction cache, and 8 KBytes of data cache, coupled with PACE III Technology, delivers the highest possible performance among current RISC microprocessors. The PaceMipsPR4000PCis fully binary compatible with the PR3000A. The availability of superpipelined FPA on-chip enables the PR4000PC to provide balanced integer and floating point performance (both single- and double-precision) that is critical to a wide range of applications.

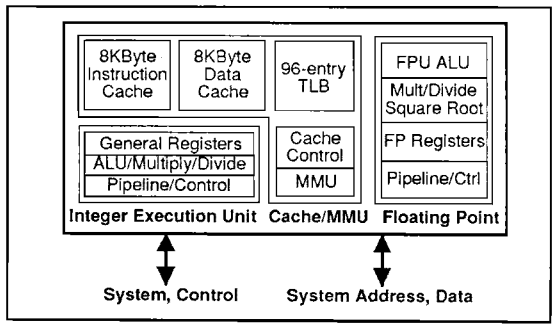
The 8 KBytes each of I & D caches are direct mapped, 64-bit wide with selectable refill sizes of 4 or 8 words. Byte parity protection is provided in both the caches. Write back scheme is followed for the data cache. The MMU is comprised of 48 entry TLB mapping onto 96 physical pages. The MMU registers are managed by software allowing programmable page sizes from 4KBytes to 16MBytes in 4KByte mulitiples. Each entry in TLB has an 8 bit process indentifier to distinguish virtual addresses of 256 different tasks. The PaceMips PR4000PC achieves its highest performance by exploiting 2-level instruction level parallelism with no issue restrictions. Besides being downward binary compatible with PR3000A, the PR4000PC also executes additional instructions that include double loads/stores to the floating point unit, branches with conditional execution of delay slot, single and double precision square root computations, conversions from floating point to integer with specific rounding mode, and conditional traps.

The PaceMips PR4000PC Microprocessor is available in a 179-lead Ceramic Pin Grid Array package.

PROCESSOR SYSTEM BLOCK DIAGRAM



PR4000 BLOCK DIAGRAM



1.0 CPU Overview

1.1 Superpipelined Implementation

The PR4000PC is the third generation RISC micro-processor from MIPS. It implements an 8-stage superpipeline which places no restrictions on instruction issue. Any two instructions can be issued each cycle under normal circumstances. The internal pipeline of the PR4000PC operates at a frequency twice that of the external clock frequency. The 8-stage superpipeline of the PR4000PC is made possible by pipelining cache accesses, shortening register access times, implementing virtually indexed primary caches, and allowing the latency of functional units to span multiple pipeline cycles. The operation of the internal pipeline is shown in Figure 1.1.

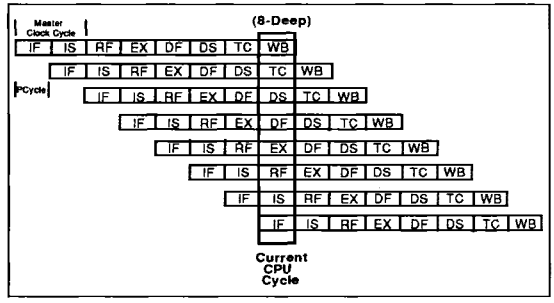


Figure 2.1 Internal Pipeline Operation

The execution of a single PR4000OC CPU instruction consists of the following eight primary steps:

IF = Instruction fetch First half. Virtual address is presented to the I-cache and TLB.

IS = Instruction fetch Second half. The I-cache outputs the instruction and the TLB generates the physical address.

RF = Register File. Three activities occur in parallel:
- (a) instruction is decoded and a check is made for interlock conditions,
- (b) instruction tag check is made to determine if there is a cache hit or not,
- (c) operands are fetched from the register file.

EX = Instruction EXecute. One of three activities can occur:
- (a) if the instruction is a register-to-register operation, an arithmetic, logical, shift, multiply, or divide operation is performed;
- (b) if the instruction is a load and store, the data virtual address is calculated;
- (c) if the instruction is a branch, the branch target virtual address is calculated and branch conditions are checked.

DF = Data cache First half. A virtual address is presented to the D-cache and TLB.

DS = Data cache Second half. The D-cache outputs the instruction and the TLB generates the physical address.

TC = Tag Check. A tag check is performed for loads and stores to determine if there is a hit or not.

WB = Write Back. The instruction result is written back to the register file.

The PR4000PC can be programmed to operate either as a 32-bit or a 64-bit microprocessor. When set to operate as a 32-bit microprocessor, PR4000PC generates 32-bit virtual addresses, and performs 32-bit operations on the contents of the general registers. When operating as a 64-bit microprocessor, the PR4000PC generates 64-bit virtual addresses, and performs 64-bit operations. The PR4000PC implements MIPS Instruction Set Architecture III, and all instructions in either mode are 32 bits wide.

1.2 Integer Unit

The PR4000PC integer processing unit contains a 32-entry register file, an ALU, and a dedicated multiplier/divider. The integer unit is the core processing unit in the PR4000PC and is responsible for instruction fetching, integer operation decoding and execution, and load and store operation execution.

The PR4000PC has thirty-two general purpose registers either 32 or 64-bits wide depending on operating mode. These registers are used for scalar integer operations and address calculation. The 32 general registers are all equivalent with two exceptions: r0 is hardwired to a zero value, and r31 is the link register for the JUMP AND LINK instruction. r0 maintains a value of zero when used as a source register under all conditions. When used as a target, the result is discarded. The register file consists of two read ports and one write port, and uses bypassing to enable the reading and writing of the same register twice per cycle, which minimizes the operation latency in the pipeline.

The PR4000PC ALU consists of the integer adder and logic unit. The adder performs address calculations in addition to arithmetic operations, and the logic unit performs all shift operations. Each of these units is highly optimized and can perform an operation in a single superpipeline cycle.The PR4000PC integer multiplier and divider units perform 32-bit and 64-bit signed and unsigned multiply and divide operations and execute instructions in parallel with the ALU. The results of the operation are placed in the MDHI and MDLO registers. The values can then be transferred to the general purpose register file using the Mfhi/Mflo instructions.

1.3 Floating Point Unit

The PR4000PC incorporates an entire floating-point unit on chip, including a floating-point register file and an execution unit that supports single and double-precision arithmetic, as specified in the IEEE standard 754. The execution unit is broken into separate multiply, divide, and add/convert/square root units, which allows for overlapped operations. The adder is pipelined, allowing a new add to begin every 4 cycles.

The floating-point register file is made up of sixteen 64-bit registers which can also be configured as thirty-two 32-bit floating-point registers. The floating-point control registers contain a register for determining configuration and revision information for the coprocessor and control and status information. Besides being fully binary compatible with MIPS ISA I, the floating point unit also implements single and double-precision square root, explicitly rounded conversions, and load and store doubleword instructions. Relative to the R3010, the latency (in nanoseconds) of floating-point multiply and divide has been improved by about 25 percent through the use of additional hardware, better process technology, and improved circuit design.

1.4 Primary Caches

The PR4000PC incorporates on-chip instruction and data caches. Each cache has its own 64-bit data path that can be accessed twice an external cycle, so the instruction and data caches can be accessed in parallel with full pipelining. Combining this feature with a pipelined access of each cache in a single external cycle, the cache subsystem provides the integer and floating-point units with an aggregate bandwidth of 1.6 GBytes per second at a master clock frequency of 50 MHz. The primary caches are virtually indexed and physically tagged. Using a part of the virtual index to address the cache enables the virtual address translation to happen in parallel with the primary cache lookup. The physically tagged cache implies that the cache need not be flushed on context switches.

The PR4000PC incorporates a direct-mapped on-chip instruction cache of 8 KBytes in size and is protected with byte parity. The tag holds a 24-bit physical address and a valid bit, and is parity protected. The instruction cache can be refilled or accessed twice per external cycle. Although the PR4000PC fetches one 64-bit unit per pipeline, only one 32-bit instruction is issued per pipeline cycle for a peak instruction bandwidth of 400 MBytes per second. The line size can be configured as four or eight words to allow different applications to have a line size that delivers optimum performance.

The PR4000PC includes a direct mapped 8 KByte on-chip data cache. The data cache is protected with byte parity and its tag is protected with a single parity bit. The D-Cache line size can be configured as four or eight words. The write policy is writeback, which means that a Store to a cache line does not immediately cause memory to be updated. This technique increases system performance by reducing bus traffic and eliminating the bottleneck of waiting for each Store operation to finish before issuing a subsequent memory operation.

A store buffer is associated with the D-Cache. When the PR4000PC executes a Store instruction, this 2-entry buffer gets written with the store data while the tag comparison is performed. If the tag matches, then the data gets written into the D-Cache in the next pipeline cycle that the D-Cache is unaccessed. The store buffer allows the PR4000PC to execute two stores per master clock cycle and to perform back-to-back stores without penalty. Likewise, the PR4000PC can perform two loads or a load and store per master clock cycle without penalty, yielding 800 MBytes per second bandwidth without restrictions on instruction combinations.

1.5 System Control Coprocessor

The system control coprocessor (CP0) translates virtual addresses into physical addresses, manages exceptions, and handles the transitions between kernel and user states. CP0 also controls the cache subsystem and provides diagnostic control and error recovery facilities. A generic system timer is provided for interval timing, time keeping, process accounting, and time slicing.

System Control Coprocessor Register File

The PR4000PC's system control coprocessor (CP0) registers provide the path through which the virtual memory system's page mapping is examined and changed, the operating modes (kernel vs. user mode, interrupts enabled or disabled, cache features) controlled, and exceptions handled. In addition, the PR4000PC includes registers to implement a real-time cycle counting facility, to address reference traps for debugging, to aid in cache diagnostic testing, and to assist in data error detection and correction.

The on-chip memory management unit controls the virtual memory system's page mapping, the operating modes, and exception handling. It consists of an instruction translation lookaside buffer (ITLB), a joint TLB, and a coprocessor register file.

Joint TLB

For fast virtual-to-physical instruction and data address translation, the PR4000PC uses a 96-entry translation lookaside buffer. This fully associative TLB is arranged in 48 even-odd page pairs. The TLB maps a 32bit virtual address and an 8-bit address space identifier into a 36bit physical address to access 64 GBytes of physical memory.

The page size can be configured, on a per-entry basis, to equal 4 KBytes to 16 MBytes in increments of powers of four. The large page size allows the TLB to map up to 1.6 GBytes of memory at any one time. The second feature is extremely important in systems where a deterministic response time to an interrupt is necessary. Each entry in the TLB can be "locked" to guarantee that translations remains in the buffer.

TLB Structure

Mapped virtual addresses are translated into physical addresses using an on-chip, fully-associative translation lookaside buffer (TLB). The TLB on the PR4000PC contains translations for 48 even-odd pairs of pages, each of which map pages ranging from 4 KBytes to 16 MBytes in size. The page size is controlled on a per-pair basis by a page mask.

Instruction TLB

The PR4000PC also incorporates a 2-entry instruction TLB. Each entry maps a 4 KByte page. The instruction TLB improves performance by allowing instruction address translation to occur in parallel with data address translation.

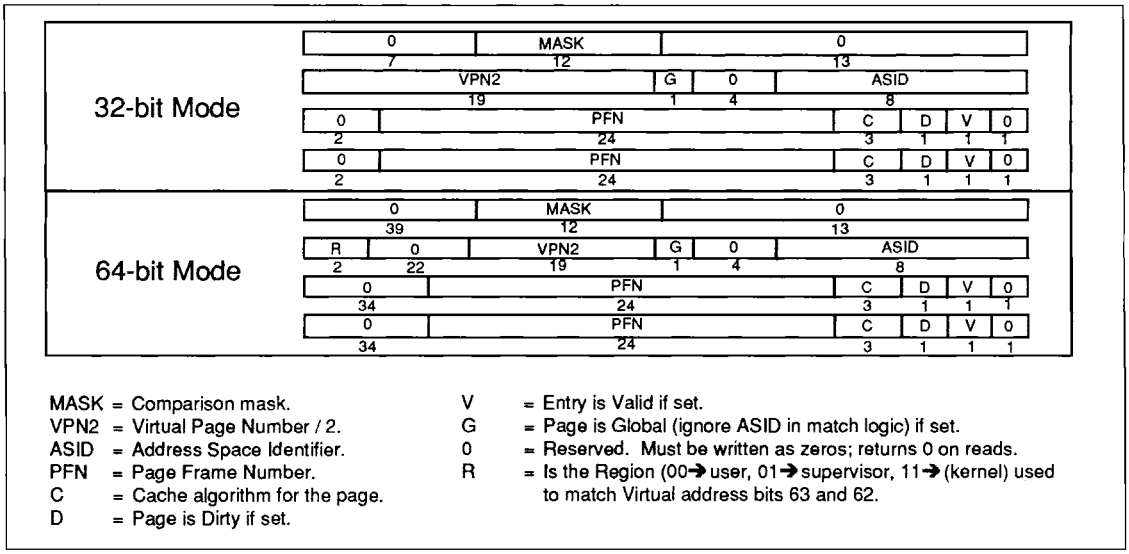


Figure 1.2 Format of a TLB Entry

When a miss occurs on an instruction address translation, the ITLB is filled from the JTLB. The operation of the ITLB is invisible to the user.

The PR4000PC provides three modes of virtual addressing: User mode, Kernal mode, and Supervisior mode. These three modes are available to system software to provide a secure environment for user processes. Bits in a status register determine which virtual addressing mode is used and whether the 32-bit or 64-bit addressing model is used. Table 2.1 shows the available virtual address space in the three modes of virtual addressing.

Table 1.1 Virtual Address Space

	KERNEL MODE	USER MODE	SUPERVISOR MODE
32-Bit	2 GBYTES	4 GBYTES	2.5 GBYTES
64-Bit	1 TERABYTE	3 TERABYTES	2 TERABYTES

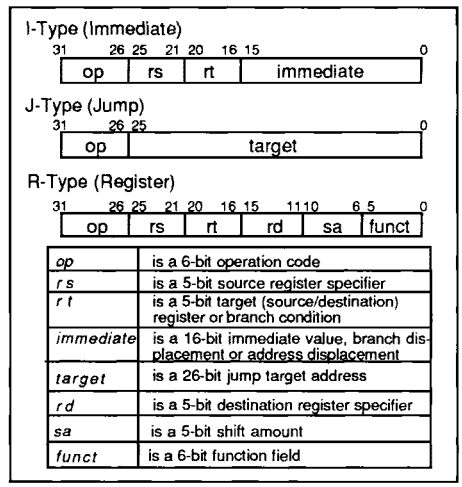


Figure 1.3 Instruction Set Formats

1.6 Instruction Set

The PR4000PC implements the extended MIPS Instruction Set Architecture (MIPS ISA III) which improves performance and adds functional capabilities while maintaining complete applications binary compatibility with earlier MIPS microprocessors. The extensions result in better code density, greater multiprocessing support, improved performance for commonly used code sequences in operating system kernels, and faster execution of floating-point intensive applications. Every instruction is 32-bits wide to allow easy and fast decode.

When operating as a 32-bit microprocessor, the PR4000PC takes an exception on those instructions that take advantage of the 64-bit architecture.

Load and Store Instructions

Load and Store instructions move data between memory and general registers. Only one addressing mode is specified: base register plus a signed 16-bit immediate offset. Bytes, halfwords, and words may be loaded to and stored from general registers by specifying aligned addresses. Unaligned memory references are efficiently supported by two pairs of load and store instructions.

The PR4000PC implementation allows the instruction immediately following a load to use the contents of the register loaded. In such cases, the hardware interlocks until the load is completed. This mechanism reduces code size in

the cases where the compiler is unable to schedule a useful instruction between a load and the use of the value loaded. It is still desirable to separate a load instruction from the instruction that uses the register loaded, but not required for correct functionality.

Computational Instructions
Computational instructions perform arithmetic, logical, and shift operations on values in registers.

Jump and Branch Instructions
All Jump and Branch instructions have an architectural delay of exactly one instruction to reduce the pipeline branch penalty. However, the PR4000PC implementation of the architecture has a three-cycle branch delay. RISC compilers manage the instruction scheduling such that the delay slot is occupied by a real instruction (instead of a nop) in most instances of Jump and Branch instructions.

Jump instructions provide an unconditional transfer of flow during program execution. Branch instructions provide a mechanism to branch based on the outcome of a specified test. An extensive set of such tests allows the efficient compilation of high-level languages. In addition, there is a variant of the branch instructions in which the instruction in the delay slot is nullified if the branch is not taken.

Exception Instructions
Exception instructions cause a trap to be executed. The trap causes a branch to the general exception handling vector.

Coprocessor Instructions
Coprocessor instructions perform operations in special-purpose hardware blocks called coprocessors.

Synchronization Instructions
There are two instructions that support synchronization between processes executing on the same processor or on different processors: Load Linked and Store Conditional. The Load Linked instruction, in addition to doing a simple load, sets a state bit called the link bit. The link bit forms a breakable link between the load linked instruction and a subsequent Store Conditional instruction. The Store Conditional instructions performs a simple store if, and only if, the link bit is set when the store is executed. If the link bit is not set, then the store will fail to execute. The success or failure of the Store Conditional instructions is indicated in the target register of the store.

1..7 Data Formats
Integer operations are performed on 32-bit or 64-bit unsigned and signed (two's complement) data. Floating-point operations are performed on data in the single-precision and double-precision floating-point formats. Loads and stores are performed on 8-bit, 16-bit, 32-bit, and 64-bit operands. The MIPS Instruction Set Architecture defines an 8-bit byte, a 16-bit halfword, a 32-bit word, and a 64-bit doubleword. The byte ordering is user configurable into either big-endian or little-endian byte ordering.

1.8 Clocking/Frequency
The PR4000PC processor bases all clocking methodology on a single clock input. This clock is then multiplied by two using internal phase lock loop techniques in order to get the internal pipeline operating frequency. The phase lock loops also eliminate skew in all clocks used and generated by the PR4000PC.

This internal clock is then divided to generate two system interface clocks, RClock and TClock. The frequency of these clocks is programmable and can be set to be either half, one third, or one fourth the processor internal clock frequency. This feature makes it easier to interface to memory and I/O systems of various frequencies.

1.9 System Interface
The PR4000PC supports a 64-bit system interface that can be used to construct systems as simple as a uniprocessor with a direct DRAM interface and no secondary cache or as sophisticated as a fully cache coherent multiprocessor. The interface consists of a 64-bit Address/Data bus with 8 check bits and a 9-bit command bus protected with parity. In addition, there are 8 handshake signals. The interface has a simple timing specification and is capable of transferring data between the processor and memory at a peak rate of 400 MBytes/second at 50 MHz. The interface signals are shown in Figure 1.4.

System Address/Data Bus
The 64-bit System Address Data (SysAD) bus is used to transfer addresses and data between the PR4000PC and the rest of the system. It is protected with an 8-bit check bus, SysADC. The check bits can be configured as either parity or ECC, for flexibility in interfacing to either parity or ECC memory systems.

The data rate and bus frequency at which the PR4000PC transmits data to the system interface are programmable via boot time mode control bits. Also, the rate at which the processor receives data is fully controlled by the external device. Therefore, either a low-cost interface requiring no write buffering or a fast, high-performance interface can be designed to communicate with the PR4000PC.

The PR4000PC interface has a 9-bit System Command (SysCmd) bus, which indicates whether the SysAD bus carries an address or data. If the SysAD carries an address, then the SysCmd bus also indicates what type of transaction is to take place (for example, a read or write). The SysCmd bus is bidirectional to support both processor requests and external requests to the PR4000PC.

The PR4000PC supports byte, halfword, tribyte, word, doubleword, and block transfers on the SysAD bus. For a

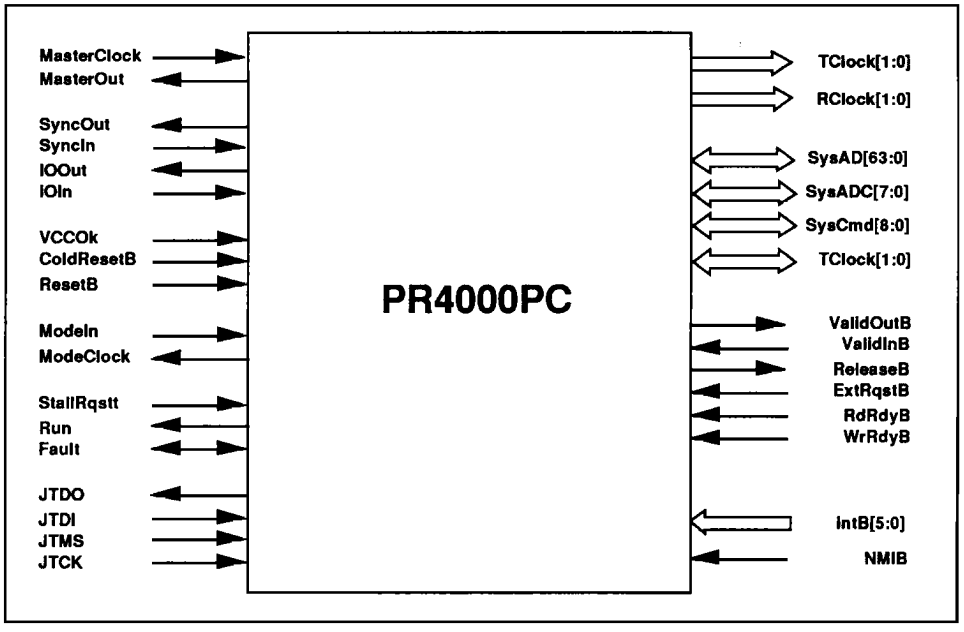


Figure1.4 PR4000PC Symbolic Pinout

sub-doubleword transfer, the low-order 3 address bits gives the byte address of the transfer, and the SysCmd bus indicates the number of bytes being transferred.

Handshake Signals

There are eight handshake signals on the system interface. Two, RdRdy* and WrRdy*, are used by an external device to indicate to the PR4000PC whether it can accept a new read or write transaction. The PR4000PC samples these signals before deasserting the address on read and write requests.

ExtRqst* and Release* are used to transfer control of the SysAD and SysCmd buses between the processor and an external device. When an external device needs to control the interface, it asserts ExtRqst*. The PR4000PC responds by asserting Release* to release the system interface to slave state. ValidOut* and ValidIn* are used by the PR4000PC and the external device respectively to indicate that there is a valid command or data on SysAD and SysCmd buses. The PR4000PC asserts ValidOut* when it is driving these buses with a valid command or data, and the external device drives ValidIn* when it has control of the buses and is driving a valid command or data.

1.10 PR4000PC Requests

The PR4000PC, which is capable of issuing requests to a memory and I/O subsystem, supports non-overlap mode of operation. This means that only one processor request may be outstanding at a time and that the request must be serviced by an external device before the PR4000PC issues another request. The PR4000PC can issue read and write requests to an external device, and an external device can issue read and write requests to the PR4000PC.

Figure 1.5 shows a processor read request. The PR4000PC asserts ValidOut* and simultaneously drives the address and read command on the SysAD and SysCmd buses. If the system interface has RdRdy* asserted, then the processor tristates its drivers and releases the system interface to slave state by asserting Release*. The external device can then begin sending the data to the PR4000PC. Figure 1.6 shows a processor write request.

External Requests

The PR4000PC responds to requests issued by an external device. The requests can take several forms. An external device may need to supply data in response to an PR4000PC read request or it may need to gain control over the system interface bus to access other resources which may be on that bus.

1.11 Interrupts

The PR4000PC processor supports six hardware interrupts and two software interrupts. The six hardware interrupts are accessible via an external write request in all three configurations, and the also through six dedicated interrupt pins on the PR4000PC.

1.12 JTAG Boundary Scan

The PR4000PC implements JTAG boundary scan, which provides a capability for testing the interconnect between the PR4000PC processor, the printed circuit board, and the other

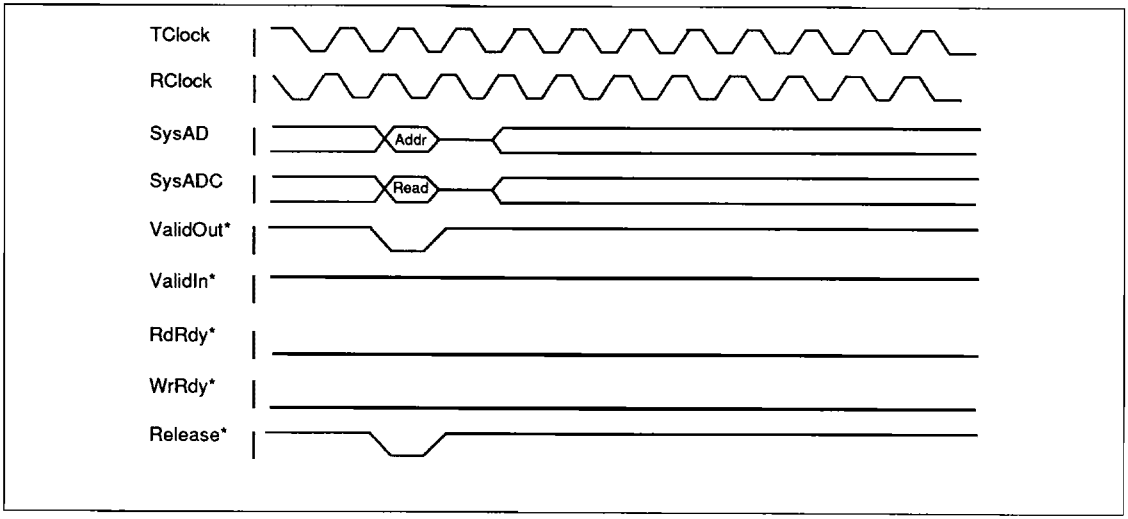


Figure 1.5 Processor Read Request

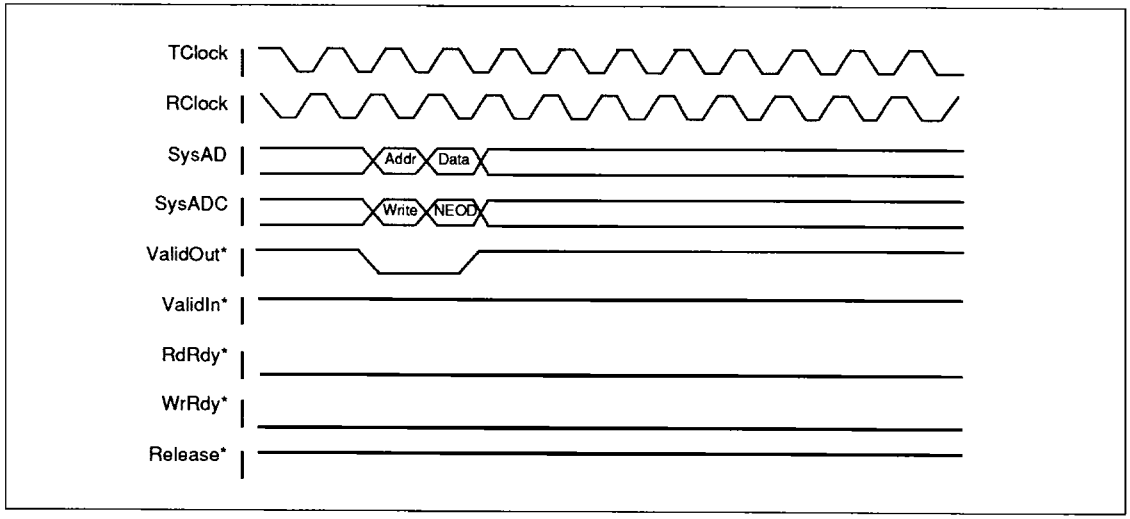


Figure1.6 Processor Write Request

components on the board. In addition, the mechanism is intended to provide a means to test the secondary cache RAM. In accordance with the JTAG specification, the PR4000PC contains a TAP controller, JTAG instruction registers, JTAG boundary scan register, JTAG identification register, and JTAG bypass register.

1.13 Boot Time Mode Control

PR4000PC fundamental operational modes are initialized viaboot time mode control interface. This serial interface operates at a very low frequency (1/64th of the input clock frequency), which allows the initialization information to be kept in a low-cost EPROM. Upon reset, PR4000PC reads serial PROM to access configuration information.

1.14 Resets

The PR4000PC processor uses a multi-level reset sequence that allows the implementation of a power-on reset, cold reset, and warm reset. Upon power on and cold reset, all processor internal state machines reset, and the PR4000PC begins fetching instructions from hex address BFC00000, which is in uncached, unmapped space. During a warm reset, however, processor internal state is preserved.

1.1.5 Fault Tolerant Support

Two PR4000PCs can be connected together to form a self-checking pair. In this mode, each PR4000PC checks the other and a difference is indicated with the assertion of a fault signal.

1.16 Debugging Support

The coprocessor Watch Register allows the setting of data break points, which cause traps when either a load or store instruction is executed to a specified physical address. Also, instruction breakpoints can be set by using the Breakpoint instruction. Development of Cache and TLB diagnostic software is facilitated by PR4000PC instructions that allow the reading and writing of any location in the cache and TLB.

1.17 Software Development Tools

MIPS offers a number of programs, utilities, and tools designed for the system programmer which aid in the development of operating systems and stand-alone software for machines based on the MIPS R4000. Among these software tools are a cache simulator, which allows the user to model the cache and memory hierarchy; an instruction set simulator, which allows the user to debug stand-alone programs; and tools and utilities that allow the user to program PROMS for a test system, download stand-alone programs from a development system to the test system, and initiate program execution and debugging.

1.18 PR4000PC System

The PR4000PC offers a one-chip processor solution for low-cost desktop systems and high-performance embedded controllers. The parts count in this system configuration, shown in Figure 1.7, is minimal.

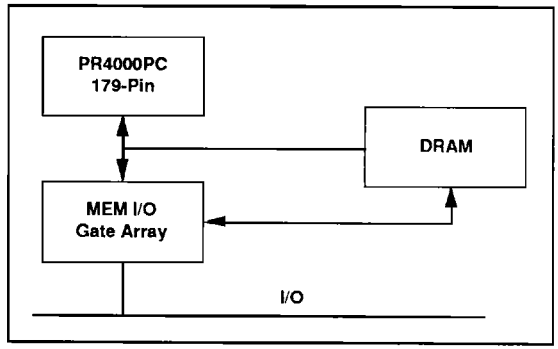


Figure1.7 Low-Cost Configuration

2.0 Interface Signals

System Interface

These signals comprise the interface between the PR4000PC and other components in the system.

ExtRqst*:	I	**External request** An external agent asserts ExtRqst* to request use of the system interface. The PR4000PC grants the request by asserting Release*.
Release*:	O	**Release interface** In response to the assertion of ExtRqst*, the PR4000PC asserts Release* to signal the requesting device that the system interface is available.
RdRdy*:	I	**Read ready** The external agent asserts RdRdy* to indicate that it can accept processor read, invalidate, or update requests in both overlap and non-overlap mode or can accept a read followed by a potential invalidate or update request in overlap mode.
SysAD(63:0):	I/O	**System address/data bus** A 64-bit address and data bus for communication between the processor and an external agent.
SysADC(7:0):	I/O	**System address/data check bus** An 8-bit bus containing check bits for the SysAD bus.
SysCmd(8:0):	I/O	**System command/data identifier bus parity** A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP:	I/O	**System command/data identifier bus parity** A single, even-parity bit for the SysCmd bus.
ValidIn*:		**IValid input** An external agent asserts ValidIn* when it is driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ValidOut*:	O	**Valid output** The PR4000PC asserts ValidOut* when it is driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
WrRdy*:	I	**Write ready** An external agent asserts WrRdy* when it can accept a processor write request.

Clock/Control Interface

These signals comprise the interface for clocking and maintenance functions.

IOOut:	O	**I/O output** Output slew rate control feedback loop output. Must be connected to IOIn through a delay loop that models the IO path from the PR4000PC to an external agent.
IOIn:	I	**I/O input** Output slew rate control feedback loop input (see IOOut).
MasterClock:	I	**Master clock** Master clock input establishes the processor operating frequency.
MasterOut:	O	**Master clock out** Master clock output aligned with MasterClock.
RClock(1:0):	O	**Receive clocks** Two identical receive clocks that establish the system interface frequency.
SyncOut:	O	**Synchronization clock out** Synchronization clock output. Must be connected to SyncIn through an interconnect that models the interconnect between MasterOut, TClock, RClock, and the external agent.
SyncIn:	I	**Synchronization clock in** Synchronization clock input.

TClock(1:0):	**O**	**Transmit clocks** Two identical transmit clocks that establish the system interface frequency.
GrpRun*:	**O**	**Group run** The PR4000PC pulses GrpRun* after completing a group of instructions.
GrpStall*:	**I**	**Group stall** An external agent asserts GrpStall* to stall the processor after completion of the current group of instructions.
Fault*:	**O**	**Fault** The PR4000PC asserts Fault* to indicate a mismatch output of boundary comparators.
Status(7:0):	**O**	**Status** An 8-bit bus that indicates the current operation status of the processor.
VccP:	**I**	**Quiet VCC for PLL** Quiet Vcc for the internal phase locked loop.
VccSense:	**I/O**	**VCC sense** This is a special pin used only in component testing and characterization. It provides a separate, direct connection from the on-chip VCC node to a package pin without attaching to the in-package power planes. Test fixtures treat VccSense as an analog output pin: the voltage at this pin directly shows the behavior of the on-chip VCC. Thus, characterization engineers can easily observe the effects of di/dt noise, transmission line reflections, etc. VccSense should be connected to VCC in functional system designs.
VssP:	**I**	**Quiet VSS for PLL** Quiet Vss for the internal phase locked loop.
VssSense:	**I/O**	**VSS sense** VssSense provides a separate, direct connection from on-chip VSS node to a package pin without attaching to the in-package ground planes. VssSense should be connected to VSS in functional system designs.

Interrupt Interface

These signals comprise the interface used by external agents to interrupt the PR4000PC processor.

Int*(5:1):	**I**	**Interrupt** Five of six general processor interrupts, bit-wise ORed with bits 5:1 of the interrupt register.
Int*(0):	**I**	**Interrupt** One of six general processor interrupts, bit-wise ORed with bit 0 of the interrupt register.
NMI*	**I:**	**Non-maskable interrupt** Non-maskable interrupt, ORed with bit 6 of the interrupt register. Non-maskable interrupt, ORed with bit 6 of the interrupt register.

Initialization Interface

These signals comprise the interface by which an external agent initializes the PR4000PC operating parameters.

ColdReset*:	**I**	**Cold reset** This signal must be asserted for a power on reset or a cold reset. The clocks SClock, TClock, and RClock begin to cycle and are synchronized with the de-assertion edge of ColdReset*. ColdReset* must be de-asserted synchronously with MasterOut.
ModeClock:	**O**	**Boot mode clock** Serial boot-mode data clock output at the system clock frequency divided by two hundred and fifty six.
ModeIn:	**I**	**Boot mode data in** Serial boot-mode data input.
Reset*:	**I**	**Reset** This signal must be asserted for any reset sequence. It may be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. Reset* must be de-asserted synchronously with MasterOut.
VCCOk:	**I**	**VCC is OK** When asserted, this signal tells the PR4000PC that the +5 volt power supply has been above 4.75V for more than 100 milliseconds & will remain stable. Assertion of VCCOk initiates initialization sequence.

JTAG Interface

These signals comprise the interface by which the JTAG boundary scan mechanism is provided.

JTDI:	**I**	**JTAG data in** Data is serially scanned in through this pin.
JTCK	**I**	**JTAG clock input** The R4000 outputs a serial clock on JTCK. On the rising edge of JTCK both JTDI and JTMS are sampled.
TDO:	**O**	**JTAG data out** Data is serially scanned out through this pin.
JTMS:	**I**	**JTAG command** JTAG command signal, signals that the incoming serial data is command data.

3.0 PR4000PC Processor Signal Summary

Description	Name	I/O	Asserted State	3-State
System address/data bus	SysAD(63:0)	I/O	High	Yes
System address/data check bus	SysADC(7:0)	I/O	High	Yes
System command/data identifier bus parity	SysCmd(8:0)	I/O	High	Yes
System command/data identifier bus parity	SysCmdP	I/O	High	Yes
Valid input	ValidIn*	I	Low	Yes
Valid output	ValidOut*	O	Low	Yes
External request	ExtRqst*	O	Low	No
Release interface	Release*	O	Low	No
Read ready	RdRdy*	I	Low	No
Write ready	WrRdy*	I	Low	No
Interrupts	Int*(5:1)	I	Low	No
Interrupt	Int*(0)	I	Low	No
Non-maskable interrupt	NMI*	I	Low	No
Boot mode data in	ModeIn	I	High	No
Boot mode clock	ModeClock	O	High	No
JTAG data in	JTDI	I	High	No
JTAG data out	JTDO	O	High	No
JTAG command	JTMS	I	High	No
JTAG clock input	JTCK	I	High	No
Transmit clocks	TClock(1:0)	O	High	No
Receive clocks	RClock(1:0)	O	High	No
Master clock	MasterClock	I	High	No
Master clock out	MasterOut	O	High	No
Synchronization clock out	SyncOut	O	High	No
Synchronization clock in	SyncIn	I	High	No
I/O output	IOOut	O	High	No
I/O input	IOIn	I	High	No
VCC is OK	VCCOk	I	High	No
Cold reset	ColdReset*	I	Low	No
Reset	Reset*	I	Low	No
Group run	GrpRun*	O	Low	No
Group stall	GrpStall*	I	Low	No
Fault	Fault*	O	Low	No
Quiet VCC for PLL	VccP	I	High	No
Quiet VSS for PLL	VssP	I	High	No

4.0 Timing Diagrams

Figure 4.1 MasterClock

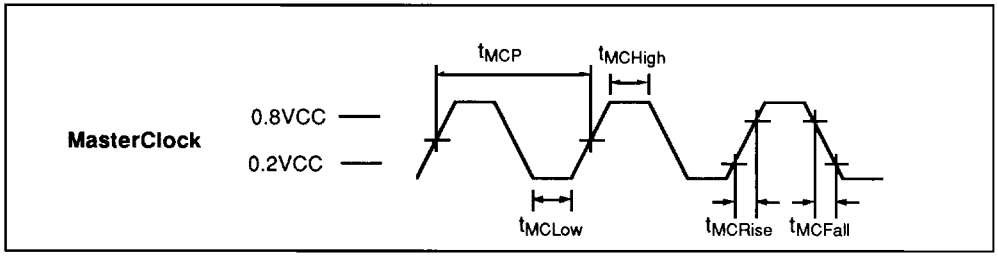
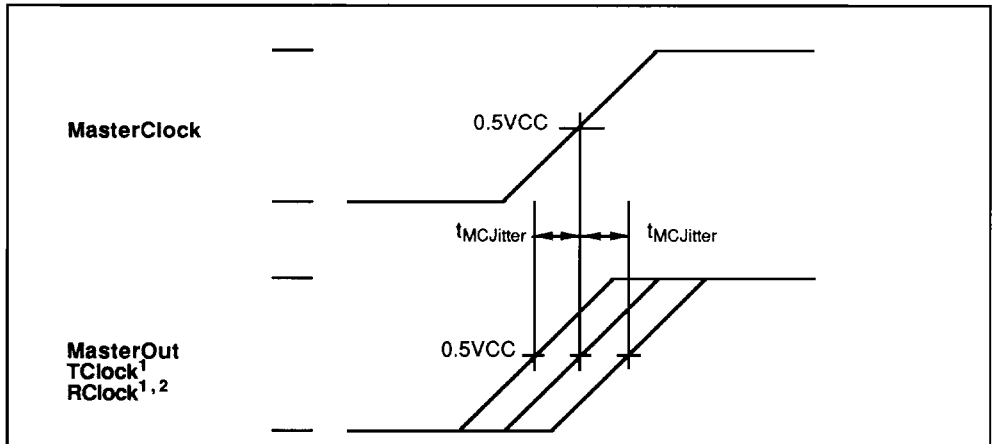


Figure 4.2 Clock Jitter



(1) With SyncOut shorted to SyncIn by the shortest path, the 50% point of TClock lines up with the 50% point of MasterClock.
(2) RClock leads TClock by 90°.
(3) The SyncIn/SyncOut path, TClock and RClock must have the same capacitive loading to match the MasterClock edges.

Figure 4.3 Processor Clock, PClock to SClock Divisor of 2

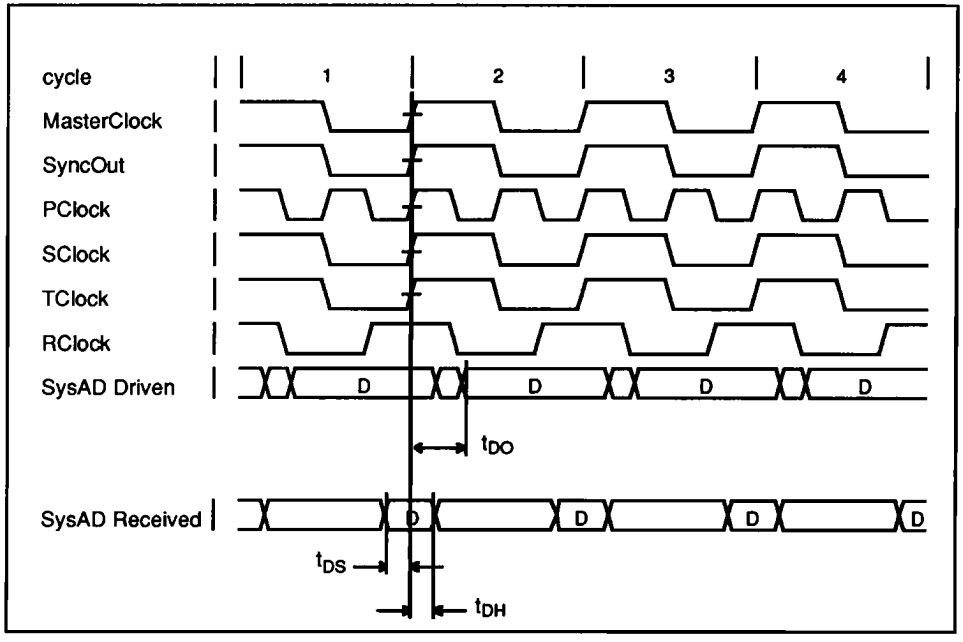


Figure 4.4 Processor Clock, PClock to SClock Divisor of 3

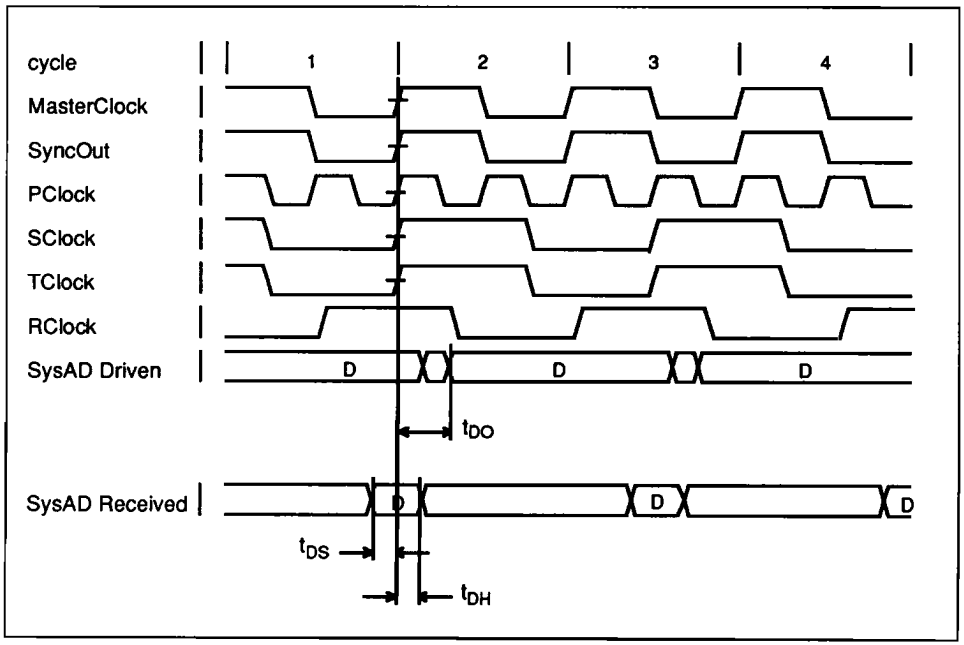


Figure 4.5 Processor Clock, PClock to SClock Divisor of 4

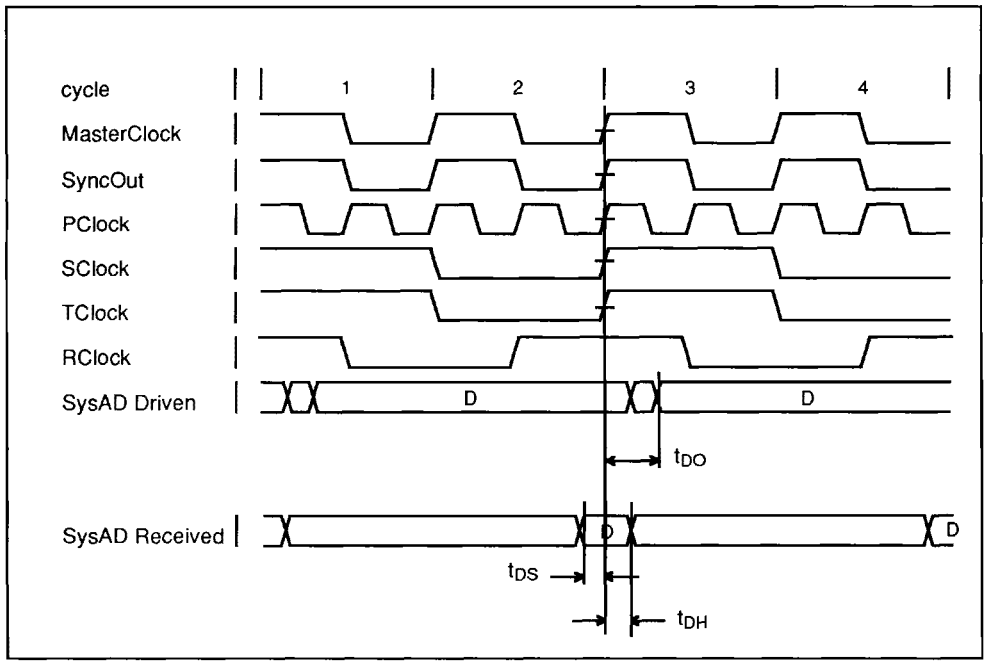
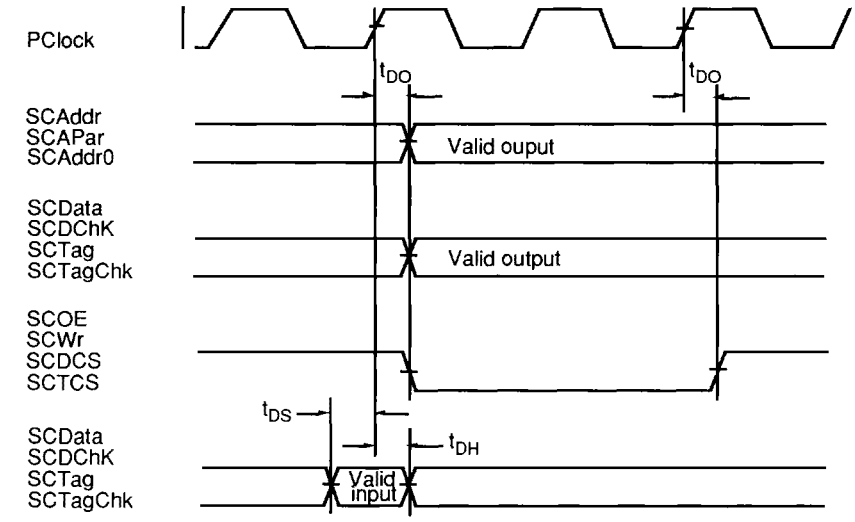


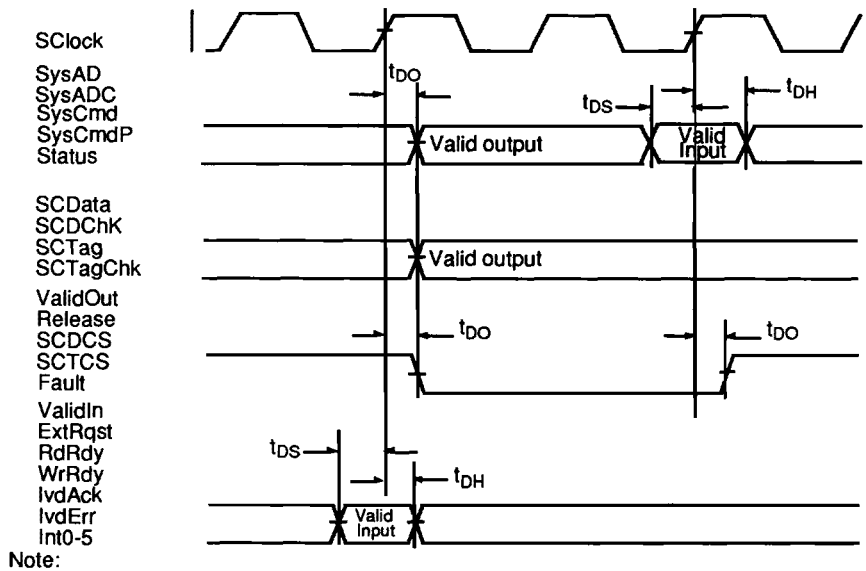
Figure 4.6 Secondary Cache Edge Timing Relationships



Note:

These waveforms only describe edge to edge timing relationships. Functional descriptions are contained in previous chapters.

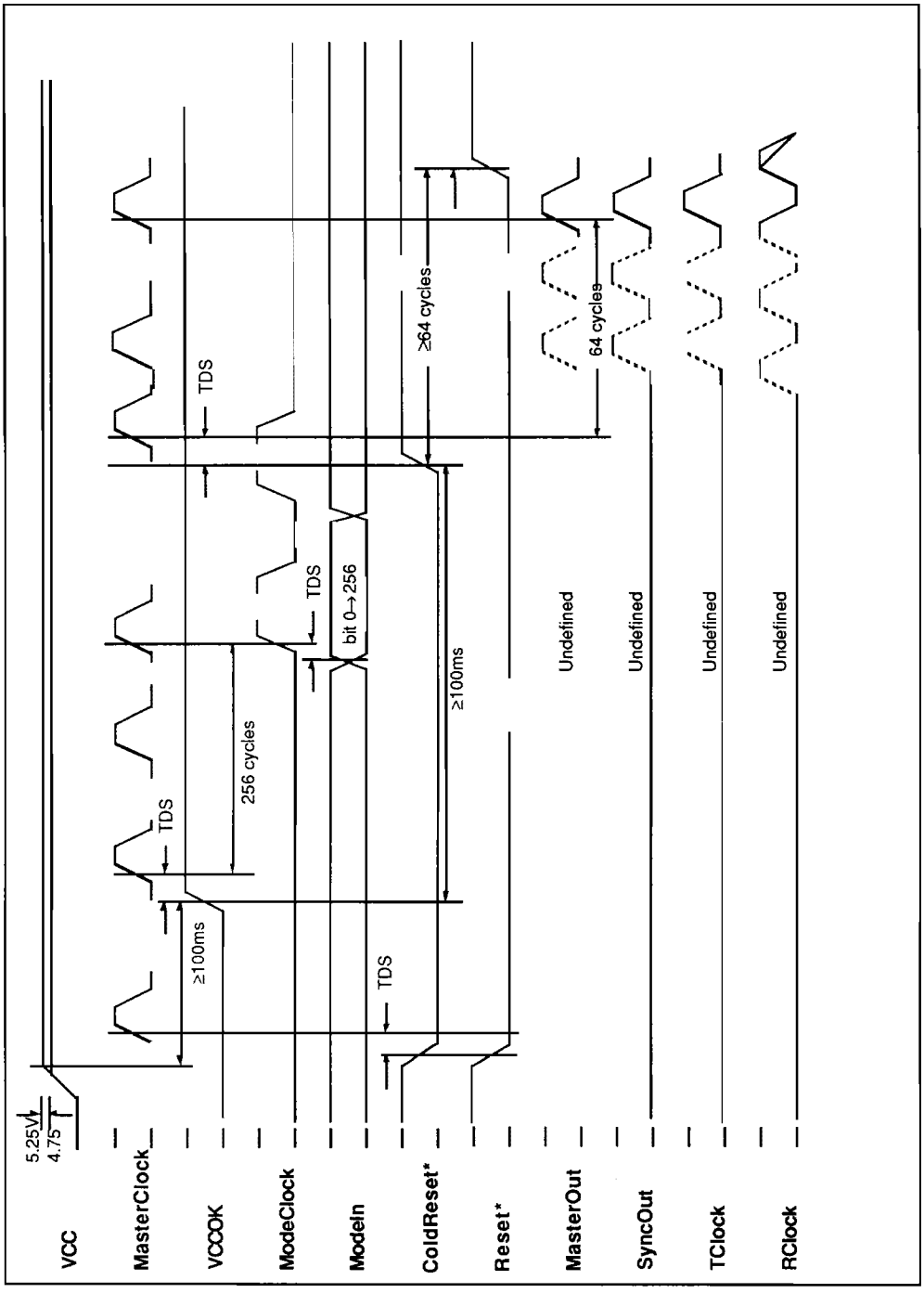
Figure 4.3 Processor Clock, PClock to SClock Divisor of 2



Note:

These waveforms only describe edge to edge timing relationships. Functional descriptions are contained in previous chapters.

Figure 4.8 Power-On Reset or Cold Reset



5.0 Specifications

5.1 DC Characteristics

Maximum Ratings – Operation beyond the limits set forth in this table may impair device's useful life.

Parameter	Symbol	Min	Max	Units
Supply Voltage	VCC	-0.5	+7.0	VDC
Input Voltage	VIN	-0.5[1]	+7.0	VDC
Storage Temperature	TST	-65.	+150.	°C
Operating Temperature	TA	0.	+70.	°C

Note:1 VIN Min. = –3.0V for pulse width less than15ns.

5.2 Recommended Operating Conditions

Range	Case	VCC
Commercial	0 to 85°C	5V ± 5%

5.3 Capacitive Load Derating Factor

Parameter	Symbol	Conditions	50MHz Min	50MHz Max	Units
Output HIGH Voltage	VOH	IOH = -4mA	3.5		V
Output HIGH Voltage (MasterOut, TClock, RClock, SyncOut)	VOHC	IOH = -4mA	4.0		V
Output LOW Voltage	VOL	IOL = 4mA		0.4	V
Input HIGH Voltage	VIH		2.0	Vcc+.5	V
Input LOW Voltage[1]	VIL		-0.5	0.8	V
Input HIGH Voltage (MasterClock, SyncIn)	VIHC		3.0	Vcc+.5	V
Input LOW Voltage[1] (MasterClock, SyncIn)	VILC		-0.5	0.2Vcc	V
Input Capacitance	CIn			10.0	pF
Output Capacitance	COut			10.0	pF
Operating Current	Icc	VCC = 5.5V		1.82	A

Note: 1 VIL Min. = –3.0V for pulse width less than 15ns.

5.4 DC Electrical Characteristics

Parameter	Symbol	Conditions	50MHz Min	50MHz Max	Units
Output HIGH Voltage	VOH	Vcc = Min.	3.5		V
Clk Output HIGH Voltage[3]	VOHC	Vcc = Min.	4.0		V
Output LOW Voltage	VOL	Vcc = Min.		0.4	V
Input HIGH Voltage[2]	VIH		2	Vcc +0.5	V
Input LOW Voltage[1,2]	VIL		–0.5[1]	0.8	V
MasterClock Input HIGH Voltage	VIHC		-0.8 Vcc	Vcc + 0.5	V
MasterClock Input LOW Voltage	VILC		–0.5[1]	0.2Vcc	V
Input Capacitance	Cin			10	pF
Output Capacitance	COut			10	pF
Operating Current	ECC	Vcc = 5V, TC=0C		3	A
Input Leakage	ILeak			10	µA
Input/Output Leakage	IOLeak	VCC = 5.5V		20	µA

Notes: 1. VIL Min. = –3.0V for pulse width less than 15ns.
2. Except for MasterClock input.
3. Applies to TClock, RClock, MasterOut and ModeClock outputs.

5.5 MasterClock and Clock Parameter

Parameter	Symbol	Test Conditions	50 MHz Min	50 MHz Max	Units
MasterClock High	t_{MCHigh}	Transition ≤ 5ns	4		ns
MasterClock Low	t_{MCLow}	Transition ≤ 5ns	4		ns
MasterClock Freq[1]			25	50	MHz
MasterClock Period	t_{MCP}		20	40	ns
Clock Jitter	$t_{MCJitter}$			500	ps
MasterClock Rise Time	t_{MCRise}			5	ns
MasterClock Fall Time	t_{MCFall}			5	ns
ModeClock Period	$t_{ModeCKP}$			$256*t_{MCP}$	ns

Note: 1 Operation of the PR4000 is only guaranteed with the Phase Lock Loop enabled.

5.6 System Interface Parameters

Parameter	Symbol	Test Conditions	50 MHz Min	50 MHz Max	Units
MasterClock High[1,2,3,4]	t_{DO}	Maximum Slew Rate Modebits[53:56]=0 Modebits[57:60]=15	2	10	ns
		Minimum Slew Rate Modebits[53:56]=15 Modebits[57:60]=0	6	16	ns
		MC* 0.5 Drive Time Modebits[50:53]=011	TBD	TBD	ns
		MC* 0.75 Drive Time Modebits[50:53]=101	TBD	TBD	ns
		MC* 1.0 Drive Time Modebits[50:53]=110	TBD	TBD	ns
Data Setup	t_{DS}		5		ns
Data Setup	t_{DH}		2		ns

Notes:
1. Parameter $t_{DM} = t_{DO}$ (min.)
2. Slew rate control and configurable drive time cannot be used at the same time. Enabling the di/dt feedback mechanism by setting Modebit[61] or Modebit[62] equal to 1, disables the effects of Modebits[50:53].
3. Timings are measured from 1.5V of the clock to 1.5V of the signal.
4. Capacitive load for all output timings is 30pF.
5. Data Output, Data Setup, and Data Hold apply to all logic signals driven out of or driven into the PR4000 on the system interface. Secondary cache signals are specified separately.

5.7 Capacitive Load Deration

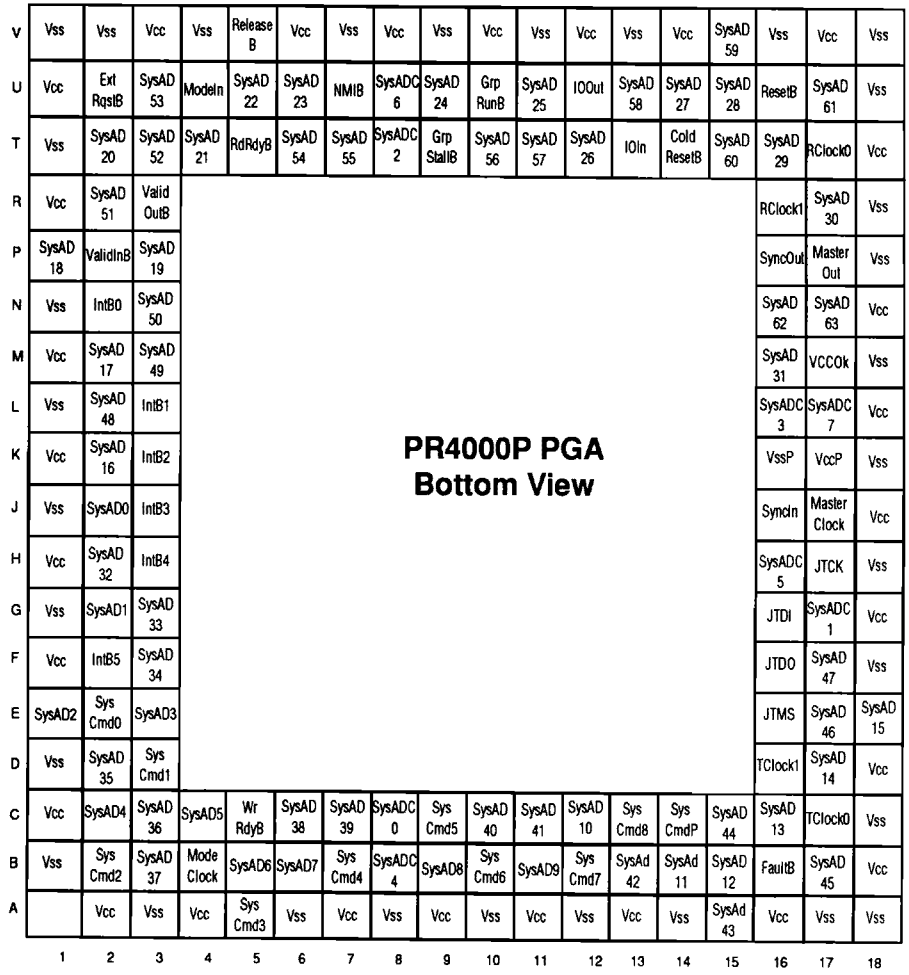
Parameter	Symbol	50 MHz Min	50 MHz Max	Units
Load Derate	CLD		2	ns/25pF

6.0 MECHANICAL DATA – Pin Assignments and Package Dimensions

Table 6.1 PR4000P Pinout – 179-Pin Ceramic Pin Grid Array, Cavity Down

Pin Name	Number	Pin Name	Number	Pin Name	Number	Pin Name	Number
ColdResetB	T14	SysAD21	T4	SysCmd1	D3	Vcc	B1
ExtRqstB	U2	SysAD22	U5	SysCmd2	B2	Vcc	C18
FaultB	B16	SysAD23	U6	SysCmd3	A5	Vcc	D1
GrpRunB	U10	SysAD24	U9	SysCmd4	B7	Vcc	R18
GrpStallB	T9	SysAD25	U11	SysCmd5	C9	Vcc	T1
IOIn	T13	SysAD26	T12	SysCmd6	B10	Vcc	U18
IOOut	U12	SysAD27	U14	SysCmd7	B12	Vcc	V1
IntB0	N2	SysAD28	U15	SysCmd8	C13	Vcc	V2
IntB1	L3	SysAD29	T16	SysCmdP	C14	Vcc	V4
IntB2	K3	SysAD30	R17	TClock0	C17	Vcc	V7
IntB3	J3	SysAD31	M16	TClock1	D16	Vcc	V9
IntB4	H3	SysAD32	H2	VCCOk	M17	Vcc	V11
IntB5	F2	SysAD33	G3	ValidInB	P2	Vcc	V13
JTCK	H17	SysAD34	F3	ValidOutB	R3	Vcc	V16
JTDI	G16	SysAD35	D2	WrRdyB	C5	Vcc	V18
JTDO	F16	SysAD36	C3	VccP	K17		
JTMS	E16	SysAD37	B3	VssP	K16		
MasterClock	J17	SysAD38	C6	Vcc	A2		
MasterOut	P17	SysAD39	C7	Vcc	A4		
ModeClock	B4	SysAD40	C10	Vcc	A7		
ModeIn	U4	SysAD41	C11	Vcc	A9		
NMIB	U7	SysAD42	B13	Vcc	A11		
PLLCap0	****	SysAD43	A15	Vcc	A13		
PLLCap1	****	SysAD44	C15	Vcc	A16		
RClock0	T17	SysAD45	B17	Vcc	B18		
RClock1	R16	SysAD46	E17	Vcc	C1		
RdRdyB	T5	SysAD47	F17	Vcc	D18		
ReleaseB	V5	SysAD48	L2	Vcc	F1		
ResetB	U16	SysAD49	M3	Vcc	H1		
SyncIn	J16	SysAD50	N3	Vcc	J18		
SyncOut	P16	SysAD51	R2	Vcc	K1		
SysAD0	J2	SysAD52	T3	Vcc	L18		
SysAD1	G2	SysAD53	U3	Vcc	M1		
SysAD2	E1	SysAD54	T6	Vcc	N18		
SysAD3	E3	SysAD55	T7	Vcc	R1		
SysAD4	C2	SysAD56	T10	Vcc	T18		
SysAD5	C4	SysAD57	T11	Vcc	U1		
SysAD6	B5	SysAD58	U13	Vcc	V3		
SysAD7	B6	SysAD59	V15	Vcc	V6		
SysAD8	B9	SysAD60	T15	Vcc	V8		
SysAD9	B11	SysAD61	U17	Vcc	A10		
SysAD10	C12	SysAD62	N16	Vcc	A12		
SysAD11	B14	SysAD63	N17	Vcc	A14		
SysAD12	B15	SysADC0	C8	Vcc	A17		
SysAD13	C16	SysADC1	G17	Vcc	A3		
SysAD14	D17	SysADC2	T8	Vcc	A6		
SysAD15	E18	SysADC3	L16	Vcc	A8		
SysAD16	K2	SysADC4	B8	Vcc	A10		
SysAD17	M2	SysADC5	H16	Vcc	A12		
SysAD18	P1	SysADC6	U8	Vcc	A14		
SysAD19	P3	SysADC7	L17	Vcc	A17		
SysAD20	T2	SysCmd0	E2	Vcc	A18		

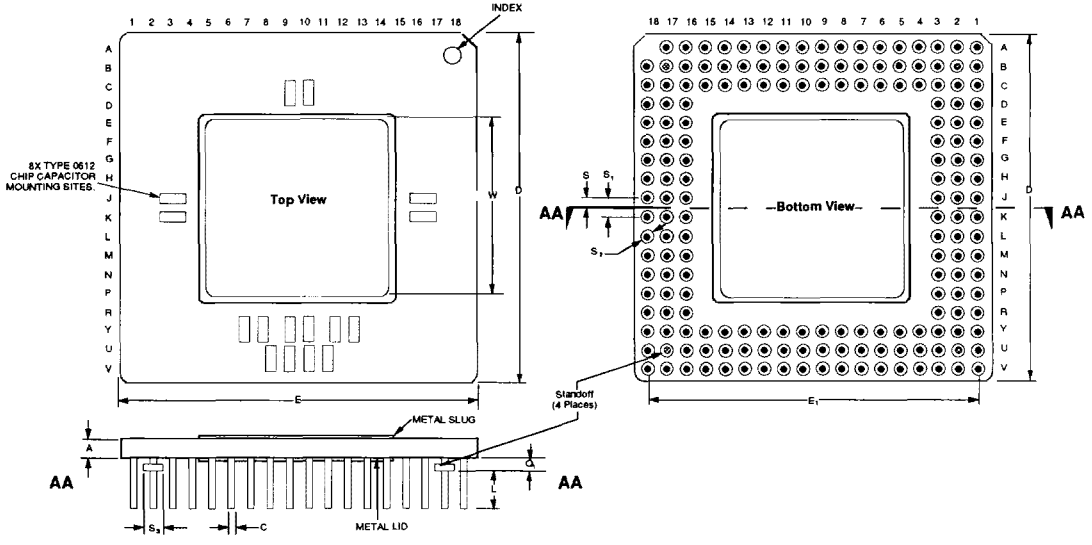
Figure 6.1 PR4000P Pin Diagram – 179-Pin Ceramic Pin Grid Array, Cavity Down



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
V	Vss	Vss	Vcc	Vss	Release B	Vcc	Vss	Vcc	Vss	Vcc	Vss	Vcc	Vss	Vcc	SysAD 59	Vss	Vcc	Vss
U	Vcc	Ext RqstB	SysAD 53	ModeIn	SysAD 22	SysAD 23	NMIB	SysADC 6	SysAD 24	Grp RunB	SysAD 25	IOOut	SysAD 58	SysAD 27	SysAD 28	ResetB	SysAD 61	Vss
T	Vss	SysAD 20	SysAD 52	SysAD 21	RdRdyB	SysAD 54	SysAD 55	SysADC 2	Grp StallB	SysAD 56	SysAD 57	SysAD 26	IOIn	Cold ResetB	SysAD 60	SysAD 29	RClock0	Vcc
R	Vcc	SysAD 51	Valid OutB													RClock1	SysAD 30	Vss
P	SysAD 18	ValidInB	SysAD 19													SyncOut	Master Out	Vss
N	Vss	IntB0	SysAD 50													SysAD 62	SysAD 63	Vcc
M	Vcc	SysAD 17	SysAD 49													SysAD 31	VCCOk	Vss
L	Vss	SysAD 48	IntB1													SysADC 3	SysADC 7	Vcc
K	Vcc	SysAD 16	IntB2													VssP	VccP	Vss
J	Vss	SysAD0	IntB3													SyncIn	Master Clock	Vcc
H	Vcc	SysAD 32	IntB4													SysADC 5	JTCK	Vss
G	Vss	SysAD1	SysAD 33													JTDI	SysADC 1	Vcc
F	Vcc	IntB5	SysAD 34													JTDO	SysAD 47	Vss
E	SysAD2	Sys Cmd0	SysAD3													JTMS	SysAD 46	SysAD 15
D	Vss	SysAD 35	Sys Cmd1													TClock1	SysAD 14	Vcc
C	Vcc	SysAD4	SysAD 36	SysAD5	Wr RdyB	SysAD 38	SysAD 39	SysADC 0	Sys Cmd5	SysAD 40	SysAD 41	SysAD 10	Sys Cmd8	Sys CmdP	SysAD 44	SysAD 13	TClock0	Vss
B	Vss	Sys Cmd2	SysAD 37	Mode Clock	SysAD6	SysAD7	Sys Cmd4	SysADC 4	SysAD8	Sys Cmd6	SysAD9	Sys Cmd7	SysAd 42	SysAd 11	SysAD 12	FaultB	SysAD 45	Vcc
A		Vcc	Vss	Vcc	Sys Cmd3	Vss	Vcc	Vss	Vcc	Vss	Vcc	Vss	Vcc	Vss	SysAd 43	Vcc	Vss	Vss

Figure 6.1 PR4000P Pin Diagram – 179-Pin Ceramic Pin Grid Array, Cavity Down

7.0 PR4000PC 179-PIN CERAMIC PIN GRID ARRAY

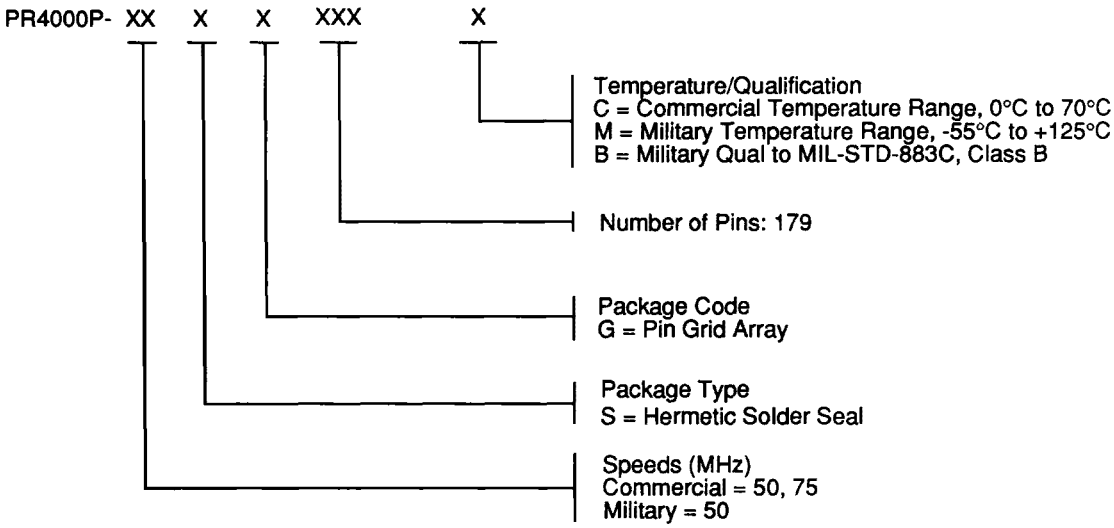


Symbol	Min.		Max	
	In.	mm.	In.	mm.
A	0.116	2,95	0.156	3,96
D	1.842	4,70	1.878	4,77
D_1	1.842	4,70	1.878	4,77
E	1.700	4,32	1.700	4,32
E_1	1.700	4,32	1.700	4,32
L	0.100	2,54	0.200	5,08
M*	18	18	18	18
N**	179	179	179	179
S	0.050	1,27	0.050	1,27
S_1	0.100	2,54	0.100	2,54
S_2	0.055	1,40	0.075	1,90
S_3	0.050	1,27	0.050	1,27
C	0.016	0,40	0.020	0,50
Q	N/A	N/A	N/A	N/A
Q_1	0.050	1,27	0.050	1,27
W	0.960	0,40	1.135	0,50

* Typical number of pins per row

** Total number of pins per package

8.0 ORDERING INFORMATION



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