

FLASH MEMORY

CMOS

16M (2M × 8/1M × 16) BIT

MBM29LV160T-90-X/-12-X/MBM29LV160B-90-X/-12-X

■ FEATURES

- **Single 3.0 V read, program and erase**
Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
Uses same software commands as E²PROMs
- **Compatible with JEDEC-standard world-wide pinouts**
48-pin TSOP (I) (Package suffix: PFTN-Normal Bend Type, PFTR-Reversed Bend Type)
46-pin SON (Package suffix: PN)
48-ball FBGA (Package suffix: PBT)
- **Minimum 100,000 program/erase cycles**
- **High performance**
90 ns maximum access time
- **Sector erase architecture**
One 8K word, two 4K words, one 16K word, and thirty-one 32K words sectors in word mode
One 16K byte, two 8K bytes, one 32K byte, and thirty-one 64K byte sectors in byte mode
Any combination of sectors can be concurrently erased. Also supports full chip erase
- **Boot Code Sector Architecture**
T = Top sector
B = Bottom sector
- **Embedded Erase™ Algorithms**
Automatically pre-programs and erases the chip or any sector
- **Embedded program™ Algorithms**
Automatically programs and verifies data at specified address
- **Data Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/Busy output (RY/BY)**
Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
When addresses remain stable, automatically switches themselves to low power mode
- **Low V_{cc} write inhibit ≤ 2.5 V**

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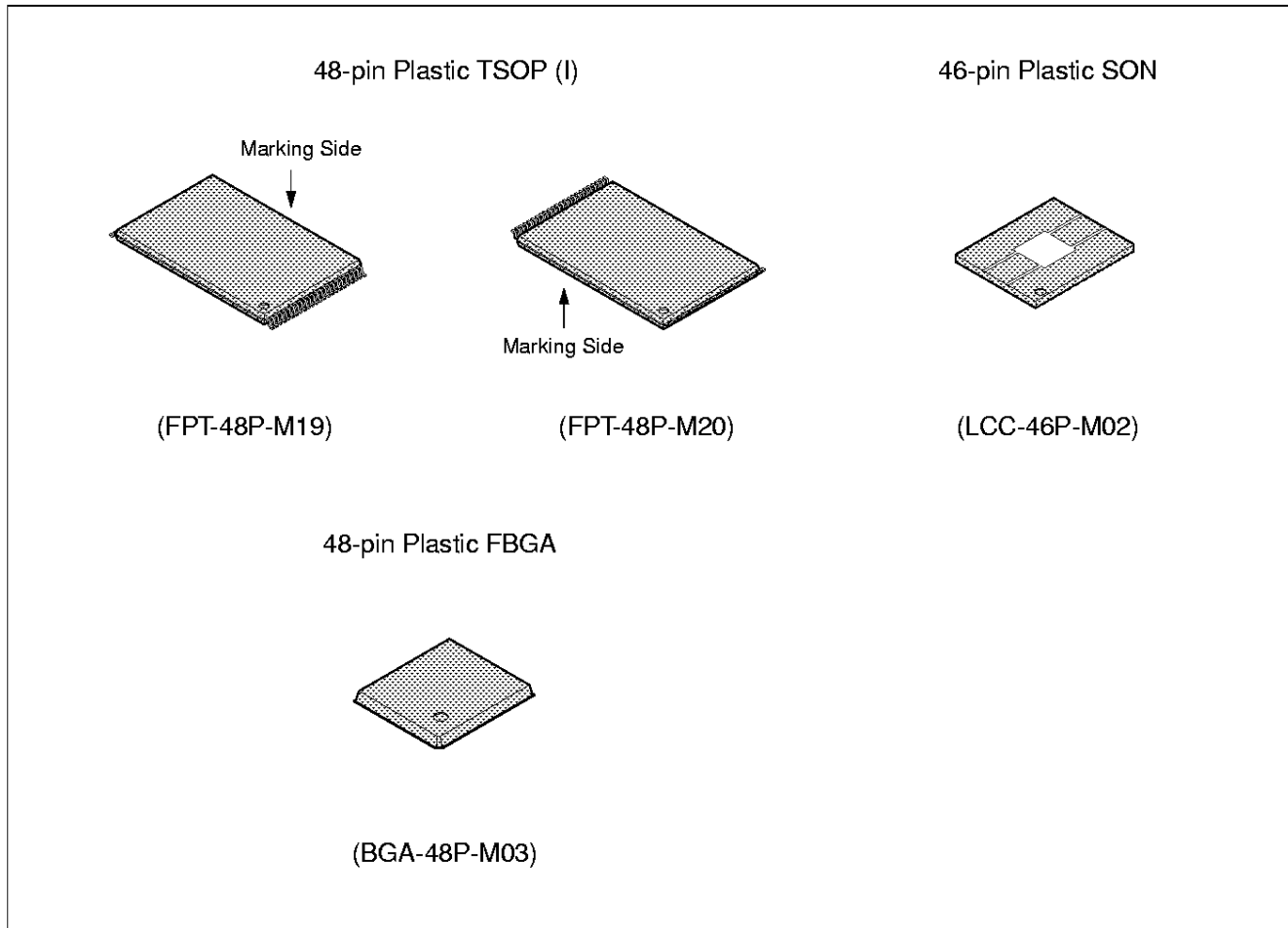
MBM29LV160T-90-X/-12-X/MBM29LV160B-90-X/-12-X

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- **Erase Suspend/Resume**
Suspends the erase operation to allow a read data and/or program in another sector within the same device
- **Sector protection**
Hardware method disables any combination of sectors from program or erase operations
- **Sector Protection set function by Extended sector Protect command.**
- **Temporary sector unprotection**
Temporary sector unprotection via the $\overline{\text{RESET}}$ pin
- **In accordance with CFI (Common Flash Memory Interface)**
- **Extended operating temperature range : -40°C to $+85^{\circ}\text{C}$**

Please refer to "MBM29LV160T/MBM29LV160B" in detailed specifications.

■ PACKAGE



MBM29LV160T-90-X/-12-X/MBM29LV160B-90-X/-12-X

■ GENERAL DESCRIPTION

The MBM29LV160T-X/B-X is a 16M-bit, 3.0 V-only Flash memory organized as 2M bytes of 8 bits each or 1M words of 16 bits each. The MBM29LV160T-X/B-X is offered in a 48-pin TSOP (I), 46-pin SON and 48-ball FBGA package. The device is designed to be programmed in-system with the standard system 3.0 V V_{CC} supply. 12.0 V V_{PP} and 5.0 V V_{CC} are not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The standard MBM29LV160T-X/B-X offers access times of 90 ns, and 120 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable (\overline{CE}), write enable (\overline{WE}), and output enable (\overline{OE}) controls.

The MBM29LV160T-X/B-X is pin and command set compatible with JEDEC standard E²PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The MBM29LV160T-X/B-X is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margins. Typically, each sector can be programmed and verified in about 0.5 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margins.

Any individual sector is typically erased and verified in 1.0 second. (If already preprogrammed.)

The device also features a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The MBM29LV160T-X/B-X is erased when shipped from the factory.

The device features single 3.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by Data Polling of DQ_7 , by the Toggle Bit feature on DQ_6 , or the $\overline{RY}/\overline{BY}$ output pin. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

The MBM29LV160T-X/B-X also has a hardware **RESET** pin. When this pin is driven low, execution of any Embedded Program Algorithm or Embedded Erase Algorithm is terminated. The internal state machine is then reset to the read mode. The **RESET** pin may be tied to the system reset circuitry. Therefore, if a system reset occurs during the Embedded Program Algorithm or Embedded Erase Algorithm, the device is automatically reset to the read mode and will have erroneous data stored in the address locations being programmed or erased. These locations need re-writing after the Reset. Resetting the device enables the system's microprocessor to read the boot-up firmware from the Flash memory.

Fujitsu's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability, and cost effectiveness. The MBM29LV160T-X/B-X memory electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

MBM29LV160T-90-X/-12-X/MBM29LV160B-90-X/-12-X

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

- One 8K word, two 4K words, one 16K word, and thirty-one 32K words sectors in word mode.
- One 16K byte, two 8K bytes, one 32K byte, and thirty-one 64K bytes sectors in byte mode.
- Individual-sector, multiple-sector, or bulk-erase capability.
- Individual or multiple-sector protection is user definable.

Sector	Sector Size	(× 8) Address Range	(× 16) Address Range
SA0	64 Kbytes or 32 Kwords	00000H to 0FFFFH	00000H to 07FFFFH
SA1	64 Kbytes or 32 Kwords	10000H to 1FFFFH	08000H to 0FFFFH
SA2	64 Kbytes or 32 Kwords	20000H to 2FFFFH	10000H to 17FFFFH
SA3	64 Kbytes or 32 Kwords	30000H to 3FFFFH	18000H to 1FFFFH
SA4	64 Kbytes or 32 Kwords	40000H to 4FFFFH	20000H to 27FFFFH
SA5	64 Kbytes or 32 Kwords	50000H to 5FFFFH	28000H to 2FFFFH
SA6	64 Kbytes or 32 Kwords	60000H to 6FFFFH	30000H to 37FFFFH
SA7	64 Kbytes or 32 Kwords	70000H to 7FFFFH	38000H to 3FFFFH
SA8	64 Kbytes or 32 Kwords	80000H to 8FFFFH	40000H to 47FFFFH
SA9	64 Kbytes or 32 Kwords	90000H to 9FFFFH	48000H to 4FFFFH
SA10	64 Kbytes or 32 Kwords	A0000H to AFFFFH	50000H to 57FFFFH
SA11	64 Kbytes or 32 Kwords	B0000H to BFFFFH	58000H to 5FFFFH
SA12	64 Kbytes or 32 Kwords	C0000H to CFFFFH	60000H to 67FFFFH
SA13	64 Kbytes or 32 Kwords	D0000H to DFFFFH	68000H to 6FFFFH
SA14	64 Kbytes or 32 Kwords	E0000H to EFFFFH	70000H to 77FFFFH
SA15	64 Kbytes or 32 Kwords	F0000H to FFFFFH	78000H to 7FFFFH
SA16	64 Kbytes or 32 Kwords	100000H to 10FFFFH	80000H to 87FFFFH
SA17	64 Kbytes or 32 Kwords	110000H to 11FFFFH	88000H to 8FFFFH
SA18	64 Kbytes or 32 Kwords	120000H to 12FFFFH	90000H to 97FFFFH
SA19	64 Kbytes or 32 Kwords	130000H to 13FFFFH	98000H to 9FFFFH
SA20	64 Kbytes or 32 Kwords	140000H to 14FFFFH	A0000H to A7FFFFH
SA21	64 Kbytes or 32 Kwords	150000H to 15FFFFH	A8000H to AFFFFH
SA22	64 Kbytes or 32 Kwords	160000H to 16FFFFH	B0000H to B7FFFFH
SA23	64 Kbytes or 32 Kwords	170000H to 17FFFFH	B8000H to BFFFFH
SA24	64 Kbytes or 32 Kwords	180000H to 18FFFFH	C0000H to C7FFFFH
SA25	64 Kbytes or 32 Kwords	190000H to 19FFFFH	C8000H to CFFFFH
SA26	64 Kbytes or 32 Kwords	1A0000H to 1AFFFFH	D0000H to D7FFFFH
SA27	64 Kbytes or 32 Kwords	1B0000H to 1BFFFFH	D8000H to DFFFFH
SA28	64 Kbytes or 32 Kwords	1C0000H to 1CFFFFH	E0000H to E7FFFFH
SA29	64 Kbytes or 32 Kwords	1D0000H to 1DFFFFH	E8000H to EFFFFH
SA30	64 Kbytes or 32 Kwords	1E0000H to 1EFFFFH	F0000H to F7FFFFH
SA31	32 Kbytes or 16 Kwords	1F0000H to 1F7FFFFH	F8000H to FBFFFFH
SA32	8 Kbytes or 4 Kwords	1F8000H to 1F9FFFFH	FC000H to FCFFFFH
SA33	8 Kbytes or 4 Kwords	1FA000H to 1FBFFFFH	FD000H to FDFFFFH
SA34	16 Kbytes or 8 Kwords	1FC000H to 1FFFFFFH	FE000H to FEFFFFH

MBM29LV160T-X Top Boot Sector Architecture

MBM29LV160T-90-X/-12-X/MBM29LV160B-90-X/-12-X

Sector	Sector Size	(× 8) Address Range	(× 16) Address Range
SA0	16 Kbytes or 8 Kwords	00000H to 03FFFFH	00000H to 01FFFFH
SA1	8 Kbytes or 4 Kwords	04000H to 05FFFFH	02000H to 02FFFFH
SA2	8 Kbytes or 4 Kwords	06000H to 07FFFFH	03000H to 03FFFFH
SA3	32 Kbytes or 16 Kwords	08000H to 0FFFFFFH	04000H to 07FFFFH
SA4	64 Kbytes or 32 Kwords	10000H to 1FFFFFFH	08000H to 0FFFFFFH
SA5	64 Kbytes or 32 Kwords	20000H to 2FFFFFFH	10000H to 17FFFFH
SA6	64 Kbytes or 32 Kwords	30000H to 3FFFFFFH	18000H to 1FFFFFFH
SA7	64 Kbytes or 32 Kwords	40000H to 4FFFFFFH	20000H to 27FFFFH
SA8	64 Kbytes or 32 Kwords	50000H to 5FFFFFFH	28000H to 2FFFFFFH
SA9	64 Kbytes or 32 Kwords	60000H to 6FFFFFFH	30000H to 37FFFFH
SA10	64 Kbytes or 32 Kwords	70000H to 7FFFFFFH	38000H to 3FFFFFFH
SA11	64 Kbytes or 32 Kwords	80000H to 8FFFFFFH	40000H to 47FFFFH
SA12	64 Kbytes or 32 Kwords	90000H to 9FFFFFFH	48000H to 4FFFFFFH
SA13	64 Kbytes or 32 Kwords	A0000H to AFFFFFFH	50000H to 57FFFFH
SA14	64 Kbytes or 32 Kwords	B0000H to BFFFFFFH	58000H to 5FFFFFFH
SA15	64 Kbytes or 32 Kwords	C0000H to CFFFFFFH	60000H to 67FFFFH
SA16	64 Kbytes or 32 Kwords	D0000H to DFFFFFFH	68000H to 6FFFFFFH
SA17	64 Kbytes or 32 Kwords	E0000H to EFFFFFFH	70000H to 77FFFFH
SA18	64 Kbytes or 32 Kwords	F0000H to FFFFFFFH	78000H to 7FFFFFFH
SA19	64 Kbytes or 32 Kwords	100000H to 10FFFFFFH	80000H to 87FFFFH
SA20	64 Kbytes or 32 Kwords	110000H to 11FFFFFFH	88000H to 8FFFFFFH
SA21	64 Kbytes or 32 Kwords	120000H to 12FFFFFFH	90000H to 97FFFFH
SA22	64 Kbytes or 32 Kwords	130000H to 13FFFFFFH	98000H to 9FFFFFFH
SA23	64 Kbytes or 32 Kwords	140000H to 14FFFFFFH	A0000H to A7FFFFH
SA24	64 Kbytes or 32 Kwords	150000H to 15FFFFFFH	A8000H to AFFFFFFH
SA25	64 Kbytes or 32 Kwords	160000H to 16FFFFFFH	B0000H to B7FFFFH
SA26	64 Kbytes or 32 Kwords	170000H to 17FFFFFFH	B8000H to BFFFFFFH
SA27	64 Kbytes or 32 Kwords	180000H to 18FFFFFFH	C0000H to C7FFFFH
SA28	64 Kbytes or 32 Kwords	190000H to 19FFFFFFH	C8000H to CFFFFFFH
SA29	64 Kbytes or 32 Kwords	1A0000H to 1AFFFFFFH	D0000H to D7FFFFH
SA30	64 Kbytes or 32 Kwords	1B0000H to 1BFFFFFFH	D8000H to DFFFFFFH
SA31	64 Kbytes or 32 Kwords	1C0000H to 1CFFFFFFH	E0000H to E7FFFFH
SA32	64 Kbytes or 32 Kwords	1D0000H to 1DFFFFFFH	E8000H to EFFFFFFH
SA33	64 Kbytes or 32 Kwords	1E0000H to 1EFFFFFFH	F0000H to F7FFFFH
SA34	64 Kbytes or 32 Kwords	1F0000H to 1FFFFFFH	F8000H to FFFFFFFH

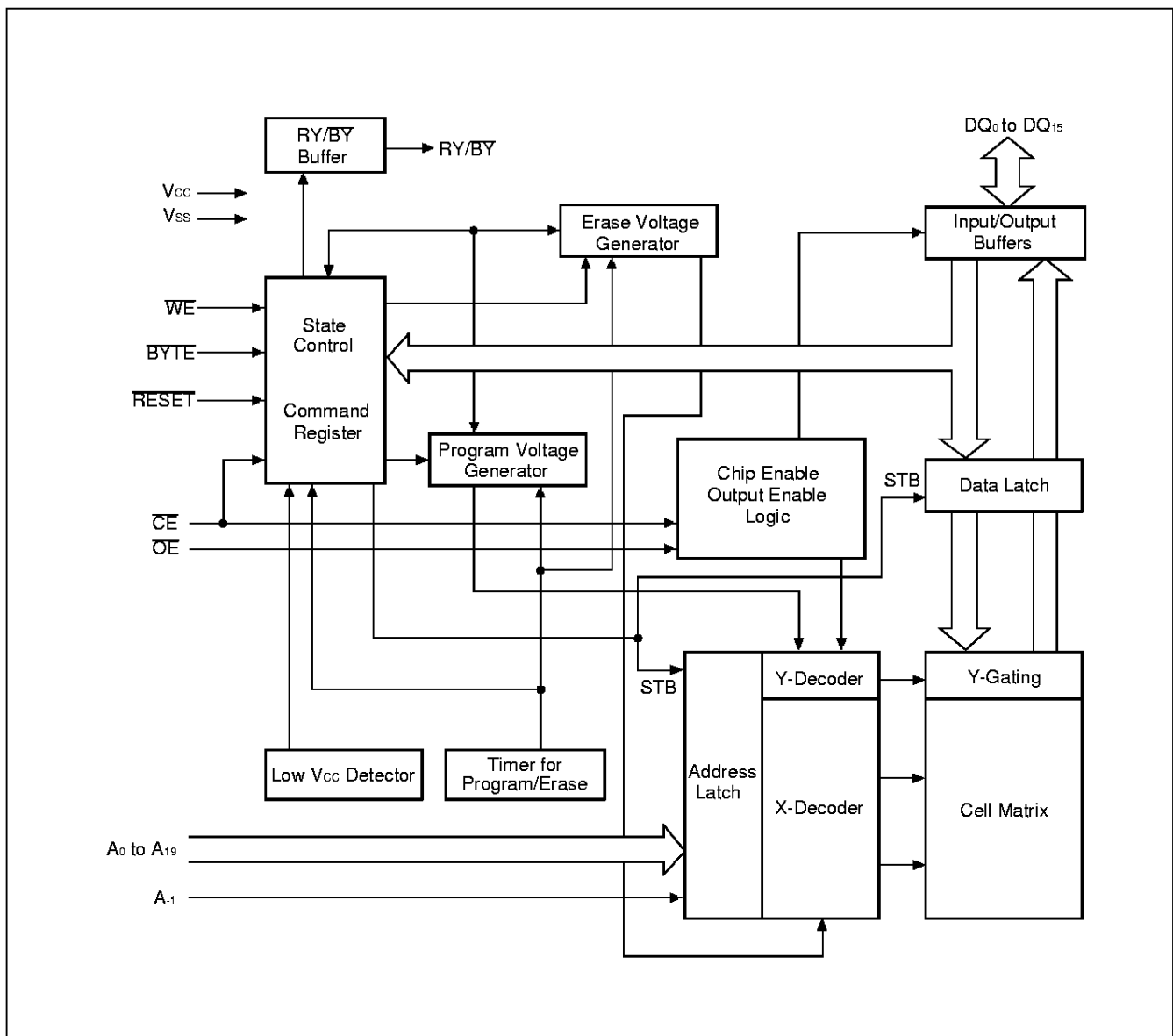
MBM29LV160B-X Bottom Boot Sector Architecture

MBM29LV160T-90-X/-12-X/MBM29LV160B-90-X/-12-X

■ PRODUCT LINE UP

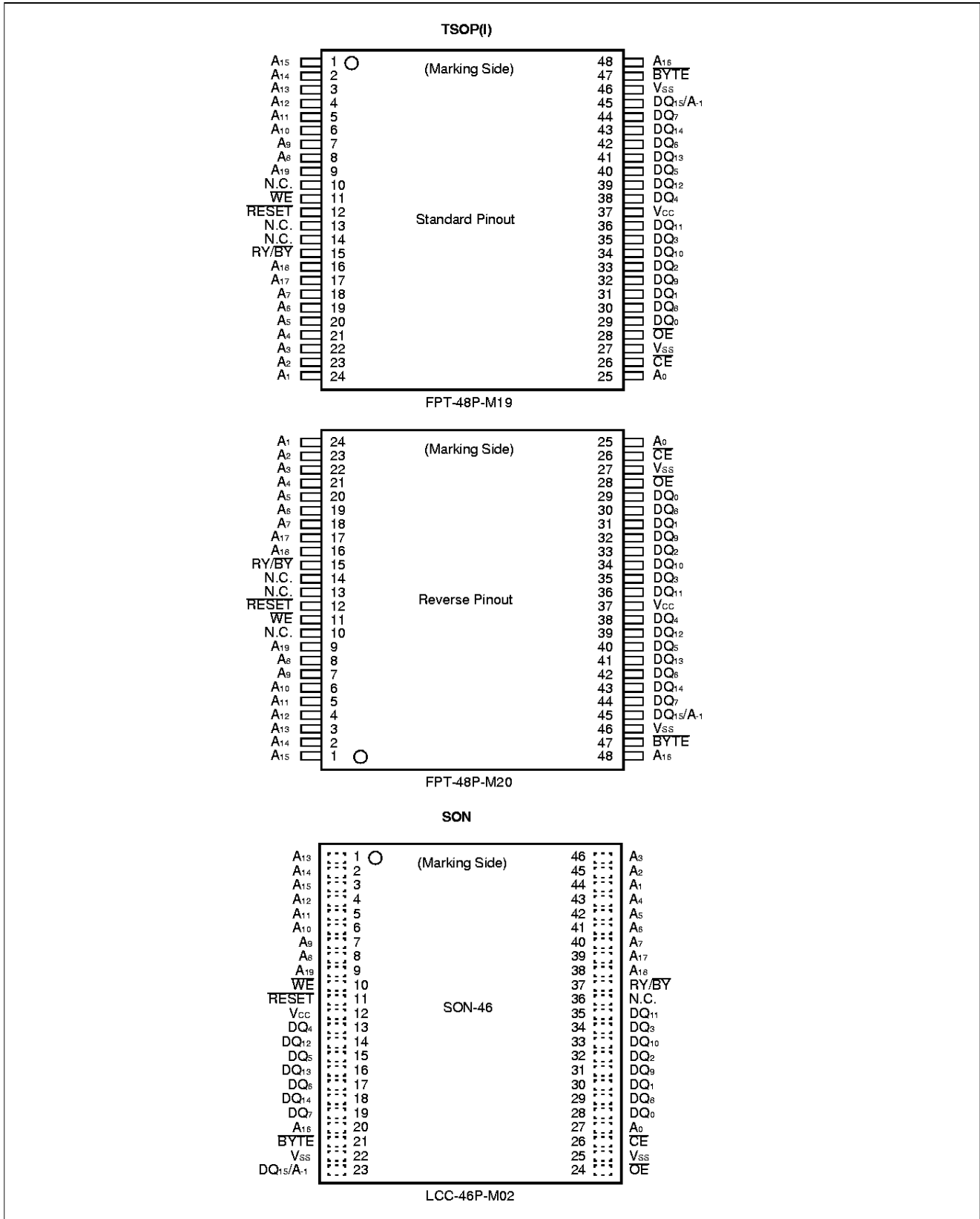
Part No.		MBM29LV160T-X/MBM29LV160B-X	
Ordering Part No.	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	-90	—
	$V_{CC} = 3.0\text{ V} \begin{matrix} +0.6\text{ V} \\ -0.3\text{ V} \end{matrix}$	—	-12
Max. Address Access Time (ns)		90	120
Max. $\overline{\text{CE}}$ Access Time (ns)		90	120
Max. $\overline{\text{OE}}$ Access Time (ns)		35	50

■ BLOCK DIAGRAM



MBM29LV160T-90-X/-12-X/MBM29LV160B-90-X/-12-X

CONNECTION DIAGRAMS

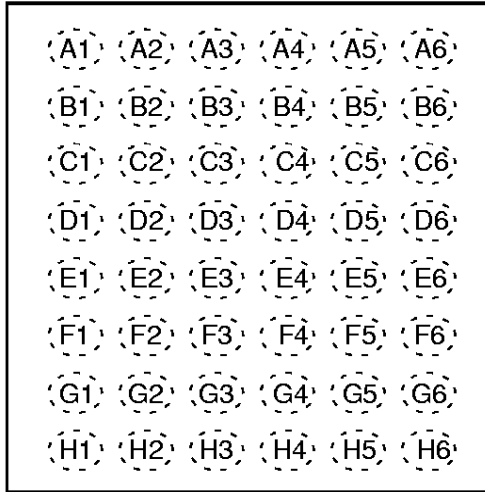


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MBM29LV160T-90-X/-12-X/MBM29LV160B-90-X/-12-X

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FPGA Marking side



(BGA-48P-M03)

A1	A ₃	A2	A ₇	A3	RY/BY	A4	WE	A5	A ₉	A6	A ₁₃
B1	A ₄	B2	A ₁₇	B3	N.C.	B4	RESET	B5	A ₈	B6	A ₁₂
C1	A ₂	C2	A ₆	C3	A ₁₈	C4	N.C.	C5	A ₁₀	C6	A ₁₄
D1	A ₁	D2	A ₅	D3	N.C.	D4	A ₁₉	D5	A ₁₁	D6	A ₁₅
E1	A ₀	E2	DQ ₀	E3	DQ ₂	E4	DQ ₅	E5	DQ ₇	E6	A ₁₆
F1	\overline{CE}	F2	DQ ₈	F3	DQ ₁₀	F4	DQ ₁₂	F5	DQ ₁₄	F6	BYTE
G1	\overline{OE}	G2	DQ ₉	G3	DQ ₁₁	G4	V _{CC}	G5	DQ ₁₃	G6	DQ ₁₅ /A-1
H1	V _{SS}	H2	DQ ₁	H3	DQ ₃	H4	DQ ₄	H5	DQ ₆	H6	V _{SS}

MBM29LV160T-90-X/-12-X/MBM29LV160B-90-X/-12-X

■ LOGIC SYMBOL

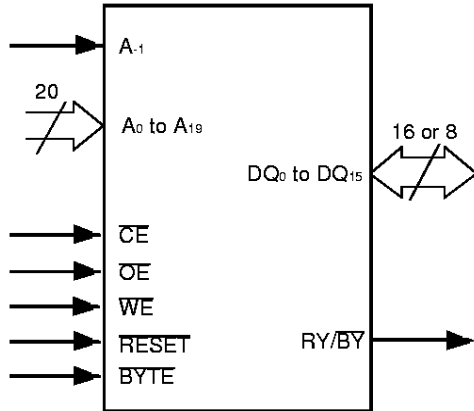


Table 1 MBM29LV160T-X/160B-X Pin Configuration

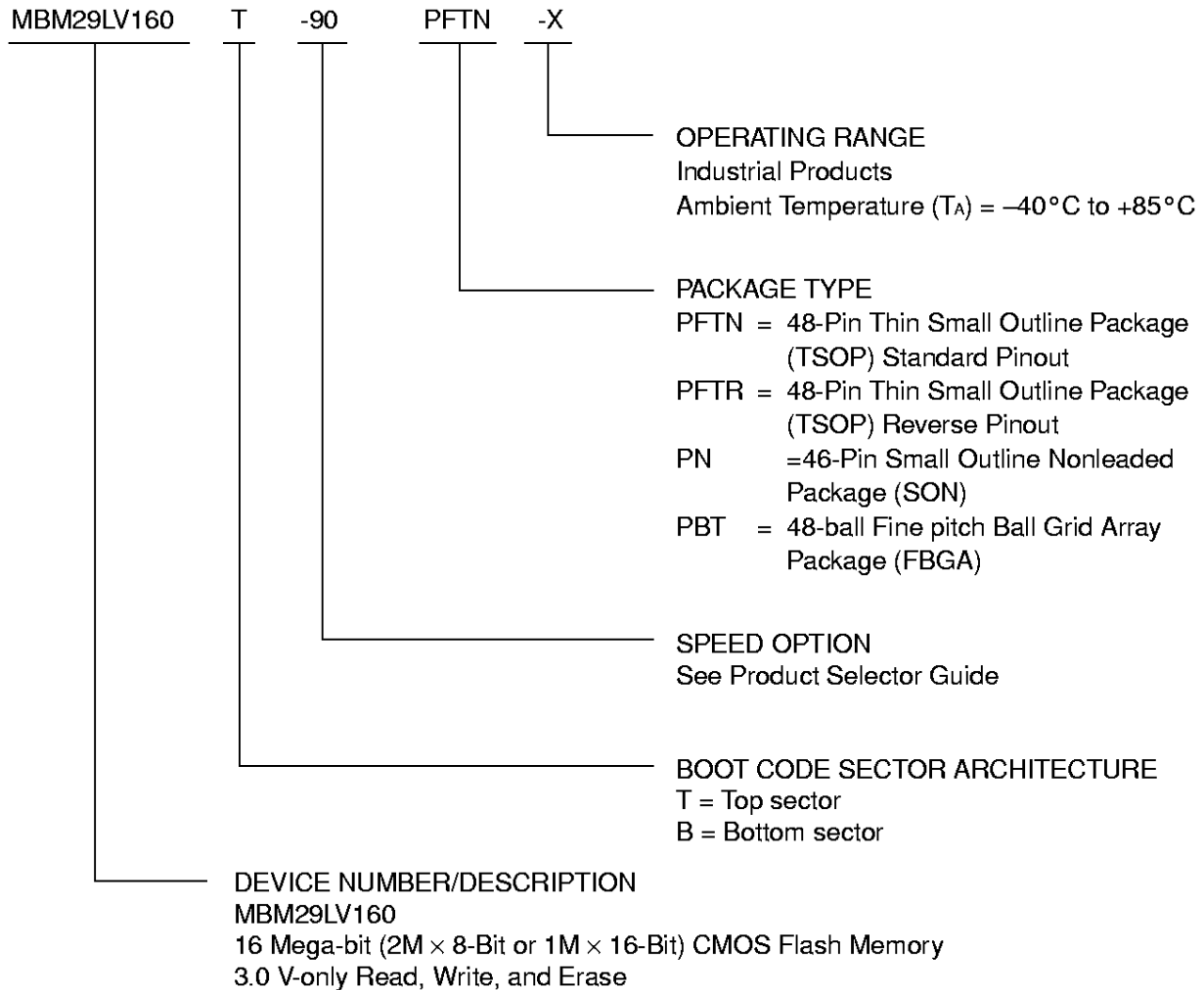
Pin	Function
A-1, A ₀ to A ₁₉	Address Inputs
DQ ₀ to DQ ₁₅	Data Inputs/Outputs
\overline{CE}	Chip Enable
\overline{OE}	Output Enable
\overline{WE}	Write Enable
RY/BY	Ready/Busy Output
RESET	Hardware Reset Pin/ Temporary Sector Unprotection
BYTE	Selects 8-bit or 16-bit mode
N.C.	Pin Not Connected Internally
V _{SS}	Device Ground
V _{CC}	Device Power Supply

MBM29LV160T-90-X/-12-X/MBM29LV160B-90-X/-12-X

■ ORDERING INFORMATION

Industrial Devices

Fujitsu industrial devices are available in several packages. The order number is formed by a combination of:



MBM29LV160T-90-X/-12-X/MBM29LV160B-90-X/-12-X

■ ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Voltage with respect to Ground All pins except A ₉ , OE, and RESET (Note 1)	-0.5 V to +V _{CC} +0.5 V
V _{CC} (Note 1)	-0.5 V to +5.5 V
A ₉ , OE, and RESET (Note 2)	-0.5 V to +13.0 V

- Notes:** 1. Minimum DC voltage on input or I/O pins are -0.5 V. During voltage transitions, inputs may negative overshoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins are V_{CC} +0.5 V. During voltage transitions, outputs may positive overshoot to V_{CC} +2.0 V for periods of up to 20 ns.
2. Minimum DC input voltage on A₉, OE, and RESET pins are -0.5 V. During voltage transitions, A₉, OE, and RESET pins may negative overshoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC input voltage on A₉, OE, and RESET pins are +13.0 V which may positive overshoot to 14.0 V for periods of up to 20 ns. Voltage difference between input voltage and supply voltage (V_{IN} - V_{CC}) do not exceed 9 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING RANGES

Industrial Devices

Ambient Temperature (T _A)	-40°C to +85°C
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V_{CC} Supply Voltages

V _{CC} Supply Voltages for MBM29LV160T/B-90	+3.0 V to +3.6 V
V _{CC} Supply Voltages for MBM29LV160T/B-12-X	+2.7 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges. Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ MAXIMUM OVERSHOOT

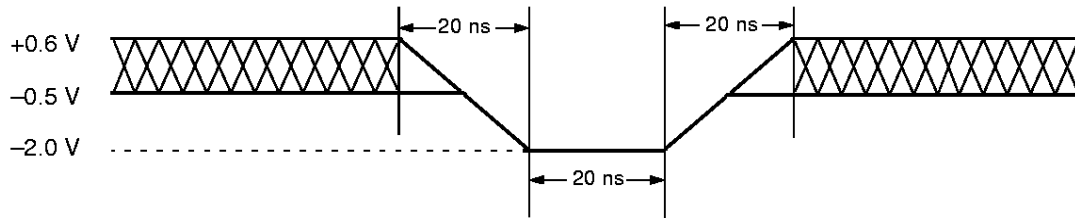


Figure 1 Maximum Negative Overshoot Waveform

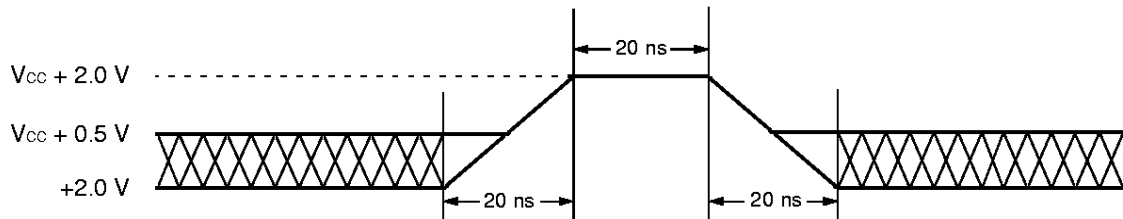
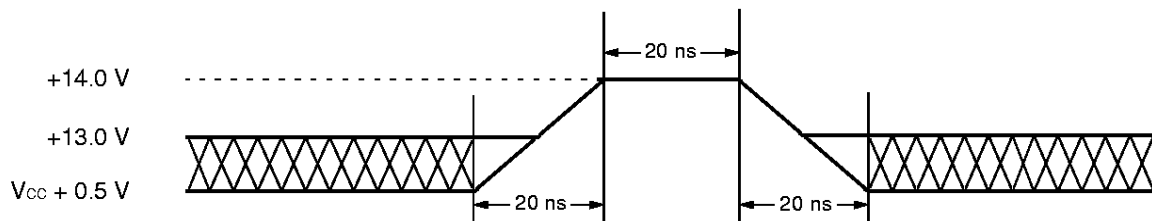


Figure 2 Maximum Positive Overshoot Waveform 1



Note : This waveform is applied for A_9 , \overline{OE} , and RESET.

Figure 3 Maximum Positive Overshoot Waveform 2

MBM29LV160T-90-X/-12-X/MBM29LV160B-90-X/-12-X

■ DC CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit	
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC} , $V_{CC} = V_{CC}$ Max.	-1.0	+1.0	μA	
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC} , $V_{CC} = V_{CC}$ Max.	-1.0	+1.0	μA	
I_{LIT}	A_9 , \overline{OE} , RESET Inputs Leakage Current	$V_{CC} = V_{CC}$ Max., A_9 , \overline{OE} , RESET = 12.5 V	—	80	μA	
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ $f = 10$ MHz	Byte	—	30	mA
			Word	—	35	
		$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ $f = 5$ MHz	Byte	—	15	mA
			Word	—	17	
I_{CC2}	V_{CC} Active Current (Note 2)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	—	35	mA	
I_{CC3}	V_{CC} Current (Standby)	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{CC} \pm 0.3$ V, RESET = $V_{CC} \pm 0.3$ V	—	5	μA	
I_{CC4}	V_{CC} Current (Standby, RESET)	$V_{CC} = V_{CC}$ Max., RESET = $V_{SS} \pm 0.3$ V	—	5	μA	
I_{CC5}	V_{CC} Current (Automatic Sleep Mode) (Note 3)	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{SS} \pm 0.3$ V, RESET = $V_{CC} \pm 0.3$ V, $V_{IN} = V_{CC} \pm 0.3$ V or $V_{SS} \pm 0.3$ V	—	5	μA	
V_{IL}	Input Low Level	—	-0.5	0.6	V	
V_{IH}	Input High Level	—	2.0	$V_{CC} + 0.3$	V	
V_{ID}	Voltage for Autoselect, Sector Protection, and Temporary Sector Unprotection (A_9 , \overline{OE} , RESET) (Note 4)	—	11.5	12.5	V	
V_{OL}	Output Low Voltage Level	$I_{OL} = 4.0$ mA, $V_{CC} = V_{CC}$ Min.	—	0.45	V	
V_{OH1}	Output High Voltage Level	$I_{OH} = -2.0$ mA, $V_{CC} = V_{CC}$ Min.	2.4	—	V	
V_{OH2}		$I_{OH} = -100$ μA , $V_{CC} = V_{CC}$ Min.	$V_{CC} - 0.4$	—	V	
V_{LKO}	Low V_{CC} Lock-Out Voltage	—	2.3	2.5	V	

- Notes:**
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component.
 2. I_{CC} active while Embedded Erase or Embedded Program is in progress.
 3. Automatic sleep mode enables the low power mode when address remain stable for 150 ns.
 4. ($V_{ID} - V_{CC}$) do not exceed 9 V.

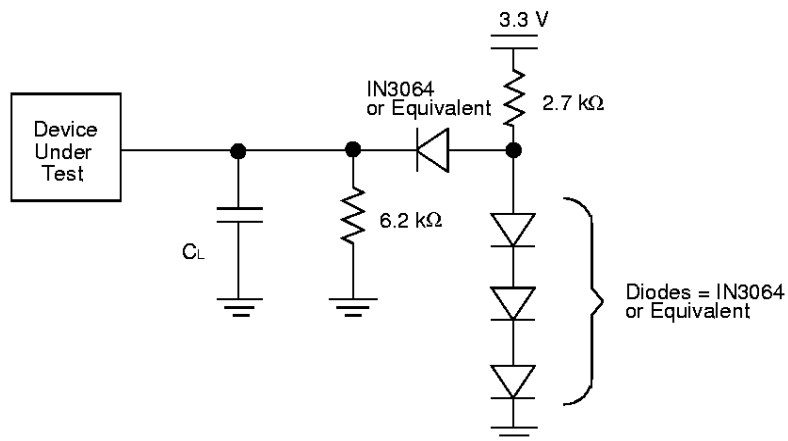
MBM29LV160T-90-X/-12-X/MBM29LV160B-90-X/-12-X

AC CHARACTERISTICS

• Read Only Operations Characteristics

Parameter Symbols		Description	Test Setup		-90-X (Note)	-12-X (Note)	Unit
JEDEC	Standard						
t_{AVAV}	t_{RC}	Read Cycle Time	—	Min.	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max.	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Max.	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	—	Max.	35	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output HIGH-Z	—	Max.	30	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output HIGH-Z	—	Max.	30	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Address, \overline{CE} or \overline{OE} , Whichever Occurs First	—	Min.	0	0	ns
—	t_{READY}	RESET Pin Low to Read Mode	—	Max.	20	20	μ s
—	t_{ELFL} t_{ELFH}	\overline{CE} or \overline{BYTE} Switching Low or High	—	Max.	5	5	ns

Note: Test Conditions: Output Load: 1 TTL gate and 30 pF (MBM29LV160T/B-90-X)
 1 TTL gate and 100 pF (MBM29LV160T/B-12-X)
 Input rise and fall times: 5 ns
 Input pulse levels: 0.0 V to 3.0 V
 Timing measurement reference level
 Input: 1.5 V
 Output: 1.5 V



Notes: $C_L = 30$ pF including jig capacitance (MBM29LV160T/B-90-X)
 $C_L = 100$ pF including jig capacitance (MBM29LV160T/B-12-X)

Figure 4 Test Conditions

MBM29LV160T-90-X/-12-X/MBM29LV160B-90-X/-12-X

• Write (Erase/Program) Operations

Parameter Symbols		Description			-90-X	-12-X	Unit	
JEDEC	Standard							
tAVAV	tWC	Write Cycle Time		Min.	90	120	ns	
tAVWL	tAS	Address Setup Time		Min.	0	0	ns	
tWLAX	tAH	Address Hold Time		Min.	45	50	ns	
tDVWH	tDS	Data Setup Time		Min.	45	50	ns	
tWHDX	tDH	Data Hold Time		Min.	0	0	ns	
—	tOES	Output Enable Setup Time		Min.	0	0	ns	
—	tOEH	Output Enable Hold Time	Read	Min.	0	0	ns	
			Toggle and $\overline{\text{Data}}$ Polling	Min.	10	10	ns	
tGHWL	tGHWL	Read Recover Time Before Write		Min.	0	0	ns	
tGHEL	tGHEL	Read Recover Time Before Write (OE High to CE Low)		Min.	0	0	ns	
tELWL	tCS	$\overline{\text{CE}}$ Setup Time		Min.	0	0	ns	
tWLEL	tWS	$\overline{\text{WE}}$ Setup Time		Min.	0	0	ns	
tWHEH	tCH	$\overline{\text{CE}}$ Hold Time		Min.	0	0	ns	
tEHWH	tWH	$\overline{\text{WE}}$ Hold Time		Min.	0	0	ns	
tWLWH	tWP	Write Pulse Width		Min.	45	50	ns	
tELEH	tCP	$\overline{\text{CE}}$ Pulse Width		Min.	45	50	ns	
tWHWL	tWPH	Write Pulse Width High		Min.	25	30	ns	
tEHEL	tCPH	$\overline{\text{CE}}$ Pulse Width High		Min.	25	30	ns	
tWHWH1	tWHWH1	Programming Operation		Byte	Typ.	8	8	μs
				Word		16		
tWHWH2	tWHWH2	Sector Erase Operation (Note 1)		Typ.	1	1	sec	
—	tEOE	Delay Time from Embedded Output Enable		Max.	90	120	ns	
—	tVCS	V _{CC} Setup Time		Min.	50	50	μs	
—	tVLHT	Voltage Transition Time (Note 2)		Min.	4	4	μs	
—	tWPP	Write Pulse Width (Note 2)		Min.	100	100	μs	
—	tOESP	$\overline{\text{OE}}$ Setup Time to $\overline{\text{WE}}$ Active (Note 2)		Min.	4	4	μs	
—	tCSP	$\overline{\text{CE}}$ Setup Time to $\overline{\text{WE}}$ Active (Note 2)		Min.	4	4	μs	
—	tRB	Recover Time From RY/BY		Min.	0	0	ns	

(Continued)

MBM29LV160T_{-90-X/-12-X}/MBM29LV160B_{-90-X/-12-X}

(Continued)

Parameter Symbols		Description		-90-X	-12-X	Unit
JEDEC	Standard					
—	t _{RH}	RESET Hold Time Before Read	Min.	50	50	ns
—	t _{RPD}	RESET to Power Down Time	Min.	20	20	μs
—	t _{BUSY}	Program/Erase Valid to RY/BY Delay	Max.	90	90	ns
—	t _{FLOZ}	BYTE Switching Low to Output HIGH-Z	Max.	30	40	ns
—	t _{FHOV}	BYTE Switching High to Output Active	Min.	30	40	ns
—	t _{VIDR}	Rise Time to V _{ID} (Note 2)	Min.	500	500	ns
—	t _{RP}	RESET Pulse Width	Min.	500	500	ns

- Notes:**
1. This does not include the preprogramming time.
 2. This timing is for Sector Protection operation.

MBM29LV160T-90-X/-12-X/MBM29LV160B-90-X/-12-X

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Sector Erase Time	—	1	15	sec	Excludes programming time prior to erasure
Byte Programming Time	—	8	3,600	μs	Excludes system-level overhead
Word Programming Time	—	16	5,200		
Chip Programming Time	—	16.8	100	sec	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycles	—

■ TSOP (I) PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0	T.B.D.	T.B.D.	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0	T.B.D.	T.B.D.	pF
C _{IN2}	Control Pin Capacitance	V _{IN} = 0	T.B.D.	T.B.D.	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ SON PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0	T.B.D.	T.B.D.	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0	T.B.D.	T.B.D.	pF
C _{IN2}	Control Pin Capacitance	V _{IN} = 0	T.B.D.	T.B.D.	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ FBGA PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0	T.B.D.	T.B.D.	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0	T.B.D.	T.B.D.	pF
C _{IN2}	Control Pin Capacitance	V _{IN} = 0	T.B.D.	T.B.D.	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

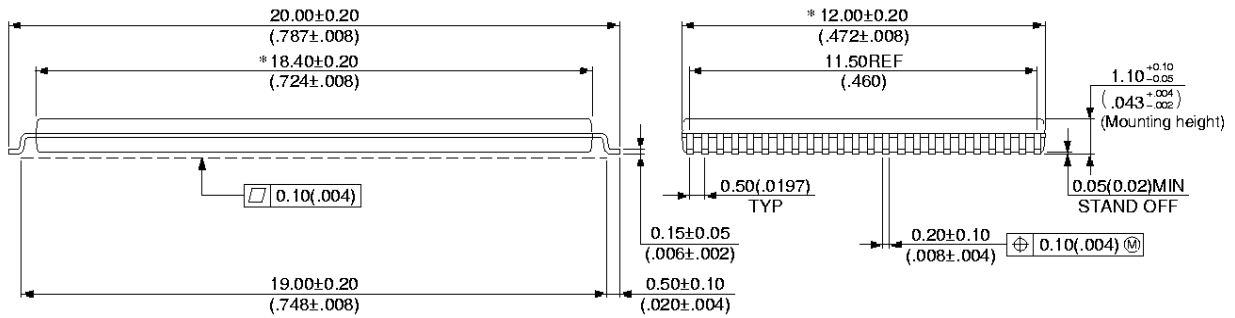
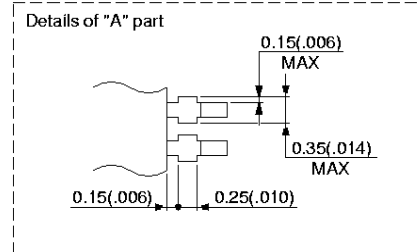
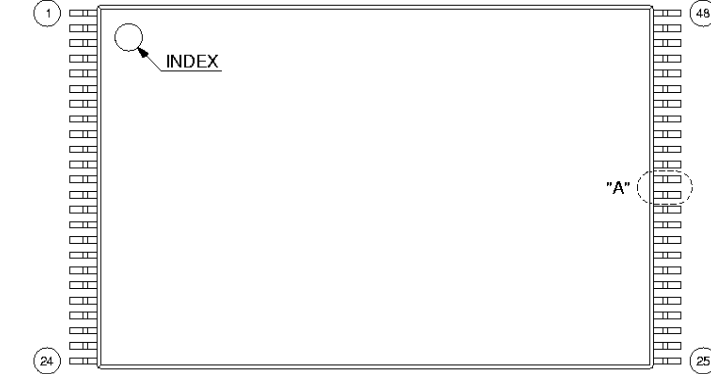
MBM29LV160T-90-X/-12-X/MBM29LV160B-90-X/-12-X

PACKAGE DIMENSIONS

48-pin plastic TSOP (I)
(FPT-48P-M19)

*: Resin protrusion. (Each side: 0.15(.006) Max)

LEAD No.



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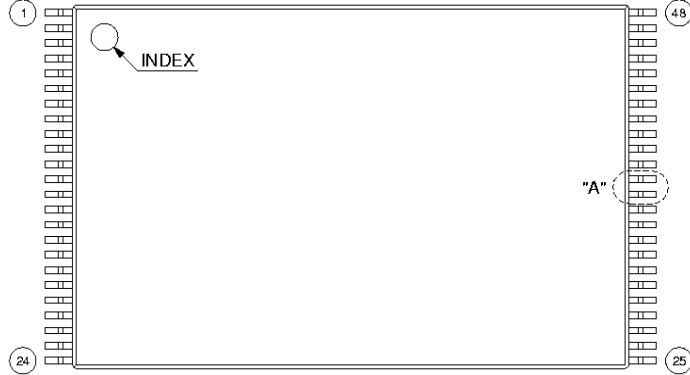
Dimensions in mm (inches)

MBM29LV160T-90-X/-12-X/MBM29LV160B-90-X/-12-X

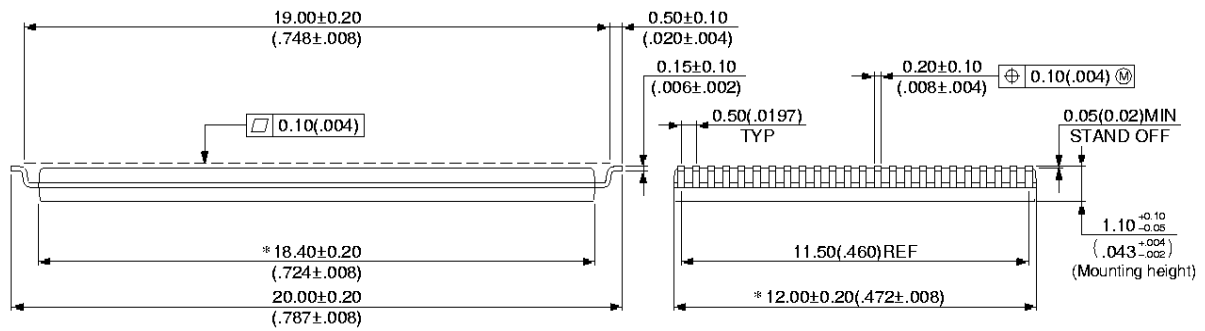
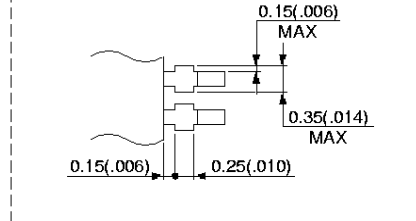
48-pin plastic TSOP (I)
(FPT-48P-M20)

*: Resin protrusion. (Each side: 0.15(.006) Max)

LEAD No.



Details of "A" part



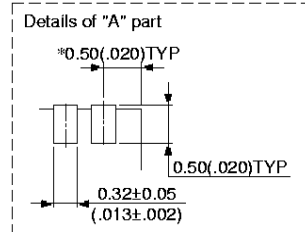
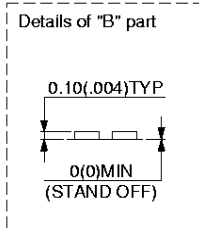
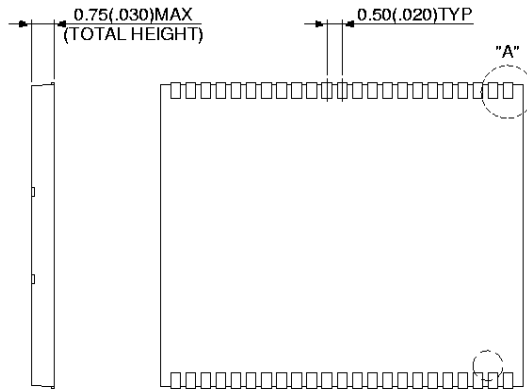
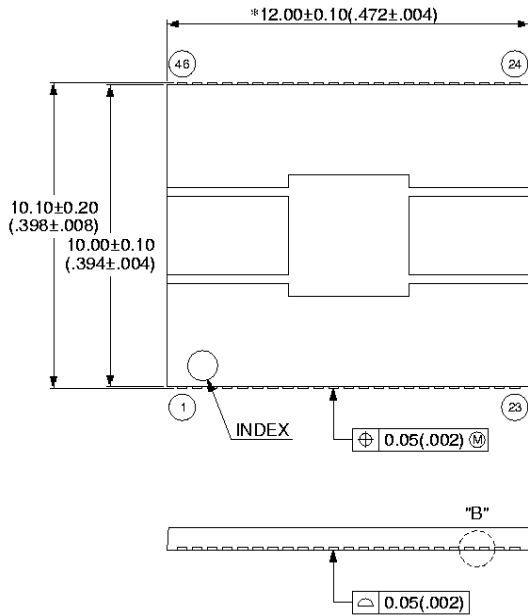
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Dimensions in mm (inches)

MBM29LV160T-90-X/-12-X/MBM29LV160B-90-X/-12-X

46-pin plastic SON
(LCC-46P-M02)

Note 1) Resin residue for * marked dimensions is 0.15 max on a single side.
Note 2) Die pad geometry may change with the models.



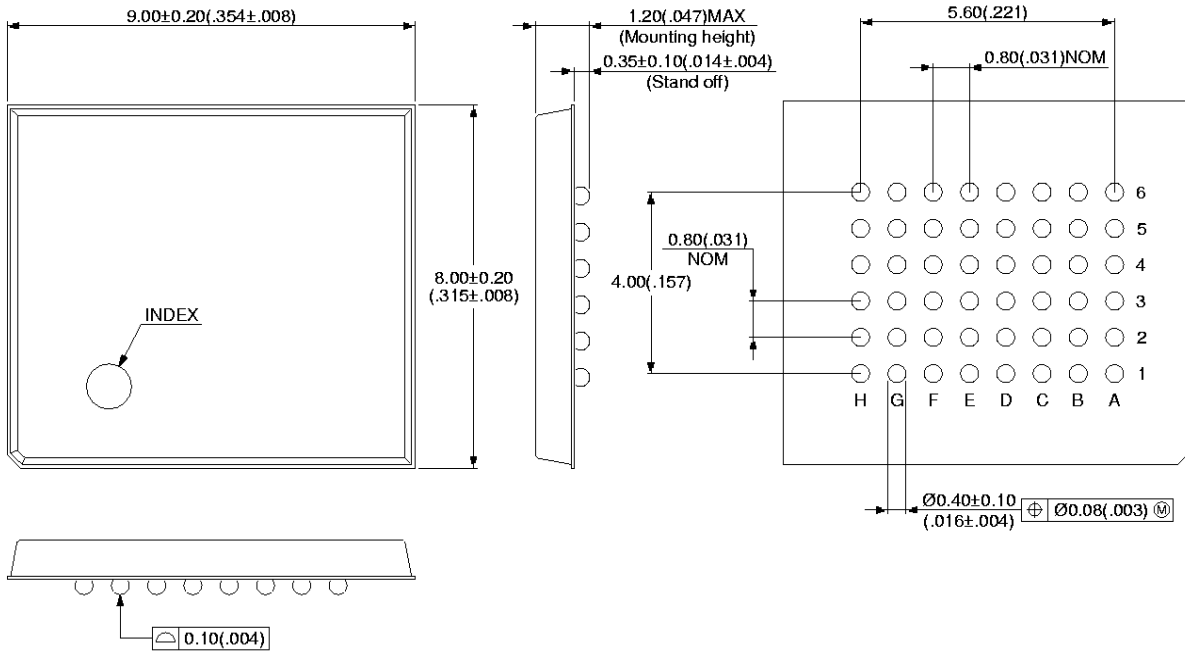
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Dimensions in mm (inches)

MBM29LV160T-90-X/-12-X/MBM29LV160B-90-X/-12-X

48-pin plastic FBGA
(BGA-48P-M03)

Note: The actual shape of corners may differ from the dimension.



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Dimensions in mm (inches)

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