6. ELECTRICAL SPECIFICATIONS

6.1 Normal Operation Mode

Corresponding Electrical Specifications

Part Number	V_{DD} = 5.0 V ± 10 %	V_{DD} = 3.0 to 3.6 V
μPD70P3000GC-25-7EA	Electrical specifications specified	Outside guaranteed operating range
μPD70P3000GC-33-7EA	Electrical specifications specified	Electrical specifications specified

6.1.1 When V_{DD} = 5.0 V ± 10 %

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage	V_{DD}	V_{DD} pin	−0.5 to +7.0	V
	CV_{DD}	CV_{DD} pin	−0.5 to +7.0	V
	CV_{SS}	CV_{SS} pin	−0.5 to +0.5	V
Input voltage	V_{I1}	Except X1 pin, V_{DD} = 5.0 V ± 10 %	−0.5 to V_{DD} + 0.3	V
	V_{I2}	V_{PP} pin in PROM programming mode, V_{DD} = 5.0 V ± 10 %	−0.5 to +13.5	V
Clock input voltage	V_X	X1 pin, V_{DD} = 5.0 V ± 10 %	−0.5 to V_{DD} + 1.0	V
Output current, low	I_{OL}	1 pin	4.0	mA
		Total of all pins	100	mA
Output current, high	I_{OH}	1 pin	−4.0	mA
		Total of all pins	−100	mA
Output voltage	V_O	V_{DD} = 5.0 V ± 10 %	−0.5 to V_{DD} + 0.3	V
Operating ambient temperature	T_A	When operating at 25 MHz	−40 to +85	°C
		When operating at 33 MHz	−20 to +70	°C
Storage temperature	T_{stg}		−65 to +150	°C

Cautions 1. Do not directly connect the output (or I/O) pins of two or more IC products, and do not directly connect them to V_{DD}, V_{CC}, or GND pin. Open-drain pins and open-collector pins may be directly connected to one another however. Moreover, an external circuit that is designed to prevent contention of output can be connected to pins that go into a high-impedance state.

2. Should the absolute maximum rating of even one of the above parameters be exceeded even momentarily, the quality of the product may be degraded. The absolute maximum ratings are, therefore, the values exceeding which the product may be physically damaged. Use the product so that these values are never exceeded.

The normal operating ranges of ratings and conditions in which the quality of the product is guaranteed are specified in the following DC Characteristics and AC Characteristics.

Capacitance (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

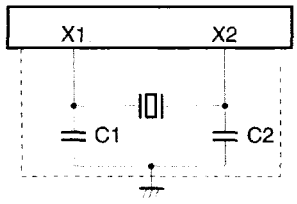
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	fc = 1 MHz			15	pF
I/O capacitance	C_{IO}	Pins other than tested pin: 0 V			15	pF
Output capacitance	C_O				15	pF

Operating Conditions

Operation Mode	Internal Operating Clock Frequency (ϕ)	Operating Temperature (T_A)	Supply Voltage (V_{DD})
Direct mode	0 to 25 MHz	−40 to +85 °C	5.0 V ± 10 %
	0 to 33 MHz	−20 to +70 °C	
PLL mode	Self oscillation frequency to 25 MHz	−40 to +85 °C	5.0 V ± 10 %
	Self oscillation frequency to 33 MHz	−20 to +70 °C	

Recommended Oscillation Circuit

(a) Ceramic resonator connection (TDK, Murata Mfg.: T_A = −40 to +85 °C, Kyocera: T_A = −20 to +80 °C)



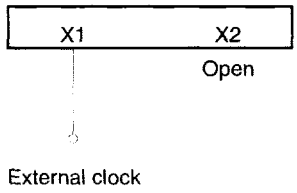
Manufacturer	Part Number	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constants		Oscillation Voltage Renge		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
TDK Corp.	FCR2.0MC3	2.0	Provided	Provided	4.5	5.5	0.26
	CCR3.2MC3	3.2	Provided	Provided	4.5	5.5	0.62
	FCR5.0MC5	5.0	Provided	Provided	4.5	5.5	0.30
	CCR5.0MC3	5.0	Provided	Provided	4.5	5.5	0.38
	CCR6.6MC3	6.6	Provided	Provided	4.5	5.5	0.32
Kyocera Corp.	KBR-2.0MS	2.0	82	82	4.5	5.5	1.2
	KBR-2.7MS	2.7	68	68	4.5	5.5	0.8
	KBR-3.2MS	3.2	47	47	4.5	5.5	0.3
	KBR-5.0MSA	5.0	33	33	4.5	5.5	0.4
	KBR-6.6MS	6.6	33	33	4.5	5.5	0.2
Murata Mfg. Co., Ltd.	CSA5.00MG	5.0	30	30	4.5	5.5	0.13
	CST5.00MGW	5.0	Provided	Provided	4.5	5.5	0.13
	CSA6.60MTZ	6.6	30	30	4.5	5.5	0.10
	CST6.60MTW	6.6	Provided	Provided	4.5	5.5	0.10

Cautions 1. Connect the oscillation circuit as closely to X2 pin as possible.

2. Do not route any other signal lines in the range indicated by the broken line in the above figure.

3. Thoroughly evaluate the matching between the μPD70P3000 and resonator.

(b) External clock input



Caution Input CMOS level voltage to the X1 pin.

DC Characteristics (T_A = −40 to +85 °C, V_{DD} = 5.0 V ± 10 %, V_{SS} = 0 V): μPD70P3000GC-25
(T_A = −20 to +70 °C, V_{DD} = 5.0 V ± 10 %, V_{SS} = 0 V): μPD70P3000GC-33

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, high		V_{IH}	Except X1 and **Note 1**	2.2		V_{DD}	V
			Note 1	0.8 V_{DD}		V_{DD}	V
Input voltage, low		V_{IL}	Except X1 and **Note 1**	0		+0.8	V
			Note 1	0		0.2 V_{DD}	V
X1 clock input voltage, high		V_{XH}	Direct mode	0.8 V_{DD}		V_{DD}	V
			PLL mode	0.8 V_{DD}		V_{DD}	V
X1 clock input voltage, low		V_{XL}	Direct mode	0		0.6	V
			PLL mode	0		0.6	V
Schmitt trigger input threshold voltage		V_T^+	**Note 1**, rising		3.0		V
		V_T^-	**Note 1**, falling		2.0		V
Schmitt trigger input hysteresis width		$V_T^+ - V_T^-$	**Note 1**	0.5			V
Output voltage, high		V_{OH}	I_{OH} = −2.5 mA	0.7 V_{DD}			V
			I_{OH} = −100 μA	V_{DD} − 0.4			V
Output voltage, low		V_{OL}	I_{OL} = 2.5 mA			0.45	V
Input leakage current, high		I_{LIH}	V_I = V_{DD}			10	μA
Input leakage current, low		I_{LIL}	V_I = 0 V			−10	μA
Output leakage current, high		I_{LOH}	V_O = V_{DD}			10	μA
Output leakage current, low		I_{LOL}	V_O = 0 V			−10	μA
Supply current	Operating	I_{DD1}	Direct mode		1.6 × ϕ + 14	2.5 × ϕ + 15	mA
			PLL mode		1.7 × ϕ + 16	2.7 × ϕ + 18	mA
	In HALT mode	I_{DD2}	Direct mode		0.5 × ϕ + 3	0.7 × ϕ + 10	mA
			PLL mode		0.6 × ϕ + 5	0.9 × ϕ + 13	mA
	In IDLE mode	I_{DD3}	Direct mode		8 × ϕ + 300	10 × ϕ + 500	μA
			PLL mode		0.1 × ϕ + 2	0.2 × ϕ + 3	mA
	In STOP mode	I_{DD4}	**Note 2**		1	50	μA
			Note 3			200	μA

Notes 1. RESET, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26, P27, P31/SI, P32/SCK, P36, P37, MODE0, MODE1, CKSEL

2. When operating at 25 MHz: −40 °C ≤ T_A ≤ +50 °C
When operating at 33 MHz: −20 °C ≤ T_A ≤ +50 °C

3. When operating at 25 MHz: 50 °C < T_A ≤ 85 °C
When operating at 33 MHz: 50 °C < T_A ≤ 70 °C

Remarks 1. TYP. value is a value for your reference at T_A = 25 °C and V_{DD} = 5.0 V.

2. ϕ: Internal operating clock frequency

Data Retention Characteristics (T_A = –40 to +85 °C): μPD70P3000GC-25
(T_A = –20 to +70 °C): μPD70P3000GC-33

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Data hold voltage	V_{DDDR}	STOP mode		1.5		5.5	V
Data hold current	I_{DDDR}	V_{DD} = V_{DDDR}	**Note 1**		0.2 V_{DDDR}	50	μA
			Note 2		0.2 V_{DDDR}	200	μA
Supply voltage rise time	t_{RVD}			200			μs
Supply voltage fall time	t_{FVD}			200			μs
Supply voltage hold time (vs. STOP mode setting)	t_{HVD}			0			ms
STOP mode release signal input time	t_{DREL}			0			ns
Data hold input voltage, high	V_{IHDR}	**Note 3**		0.9 V_{DDDR}		V_{DDDR}	V
Data hold input voltage, low	V_{ILDR}	**Note 3**		0		0.1 V_{DDDR}	V

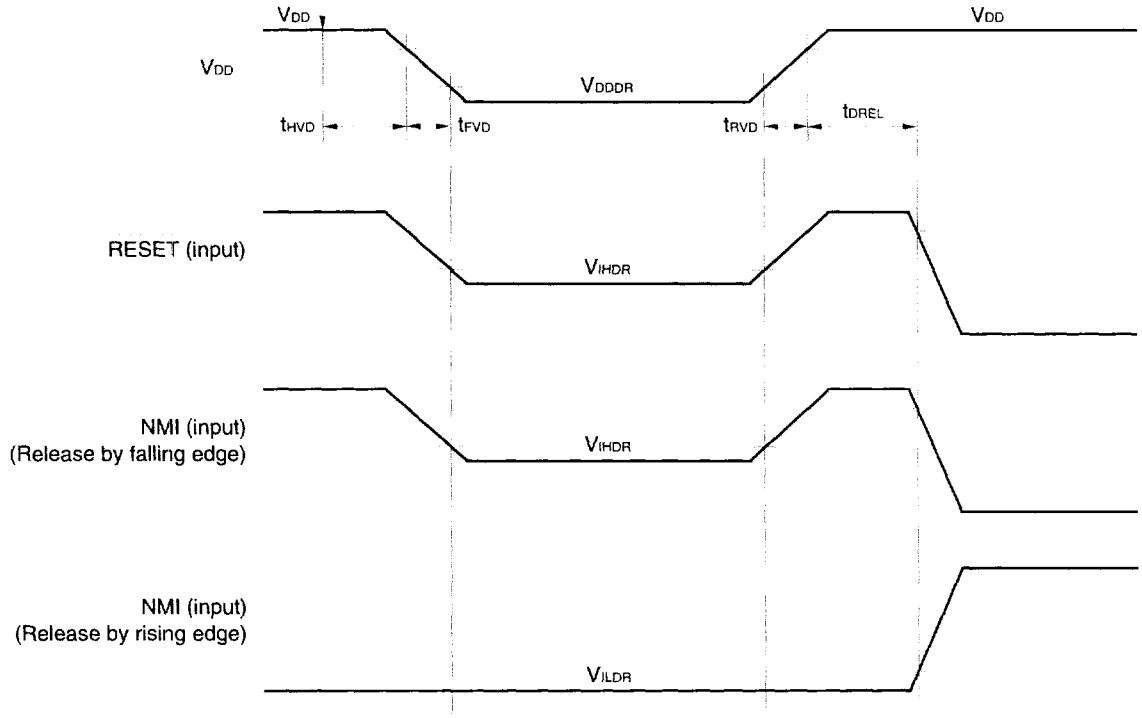
Notes 1. When operating at 25 MHz: –40 °C ≤ T_A ≤ +50 °C
When operating at 33 MHz: –20 °C ≤ T_A ≤ +50 °C

2. When operating at 25 MHz: 50 °C < T_A ≤ 85 °C
When operating at 33 MHz: 50 °C < T_A ≤ 70 °C

3. RESET, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INT03, P26, P27, P31/SI, P32/SCK, P36, P37, MODE0, MODE1, CKSEL, X1

Remark TYP. value is a value for your reference at T_A = 25 °C and V_{DD} = 5.0 V.

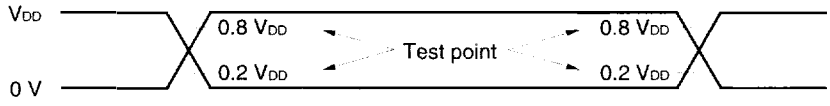
STOP mode is set (at fifth clock after PSC register has been set).



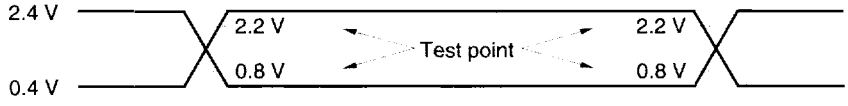
AC Characteristics (T_A = −40 to +85 °C, V_{DD} = 5.0 V ± 10 %, V_{SS} = 0 V): μPD70P3000GC-25
(T_A = −20 to +70 °C, V_{DD} = 5.0 V ± 10 %, V_{SS} = 0 V): μPD70P3000GC-33

AC test input wave

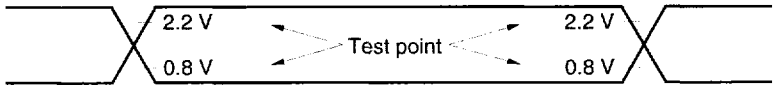
(a) RESET, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26, P27, P31/SI, P32/SCK, P36, P37, MODE0, MODE1, CKSEL, X1



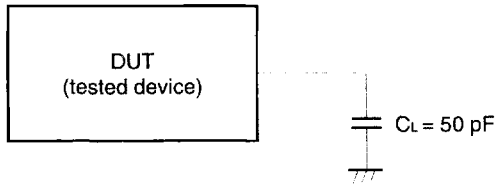
(b) Other than (a)



AC test output test point



Load condition



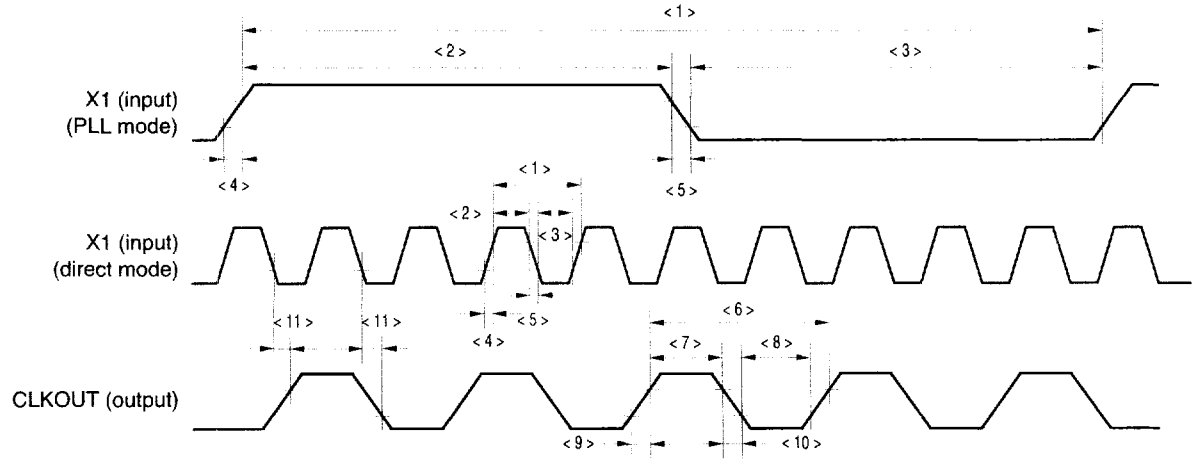
Caution If the load capacitance exceeds 50 pF due to the circuit configuration, decrease the load capacitance of this device to less then 50 pF by using a buffer.

(1) Clock timing

Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
X1 input cycle	<1>	t_{CYX}	Direct mode	20	DC	15	DC	ns
			PLL mode	200	315	150	334	ns
X1 input width, high	<2>	t_{WXH}	Direct mode	7		6		ns
			PLL mode	80		60		ns
X1 input width, low	<3>	t_{WXL}	Direct mode	7		6		ns
			PLL mode	80		60		ns
X1 input rise time	<4>	t_{XR}	Direct mode		7		7	ns
			PLL mode		15		10	ns
X1 input fall time	<5>	t_{XF}	Direct mode		7		7	ns
			PLL mode		15		10	ns
CPU operating frequency	—	ϕ		0	25	0	33	MHz
CLKOUT output cycle	<6>	t_{CYK}		40	DC	30	DC	ns
CLKOUT width, high	<7>	t_{WKH}		0.5 T – 5		0.5 T – 5		ns
CLKOUT width, low	<8>	t_{WKL}		0.5 T – 5		0.5 T – 5		ns
CLKOUT rise time	<9>	t_{XR}			5		5	ns
CLKOUT fall time	<10>	t_{XF}			5		5	ns
X1 ↓→ CLKOUT delay time	<11>	t_{DXK}	Direct mode	3	17	3	17	ns

Remark T = t_{CYK}

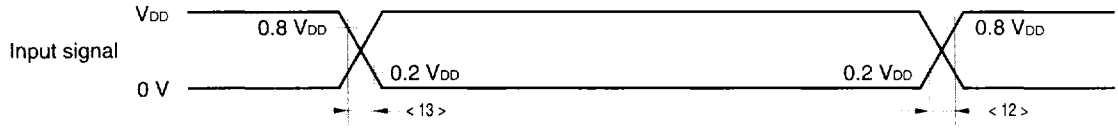
Parameter	Symbol		Condition	μPD70P3000-25	μPD70P3000-33	Unit
				TYP.	TYP.	
Self oscillation frequency	—	ϕ_P	PLL mode	2.8	2.8	MHz



(2) Input waveform

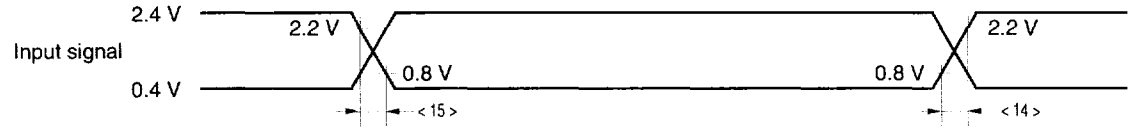
(a) RESET, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26, P27, P31/SI, P32/SCK, P36, P37, MODE0, MODE1, CKSEL, X1

Parameter	Symbol	Condition	μPD70P3000-25		μPD70P3000-33		Unit
			MIN.	MAX.	MIN.	MAX.	
Input rise time	<12> t_{IR2}			20		20	ns
Input fall time	<13> t_{IF2}			20		20	ns



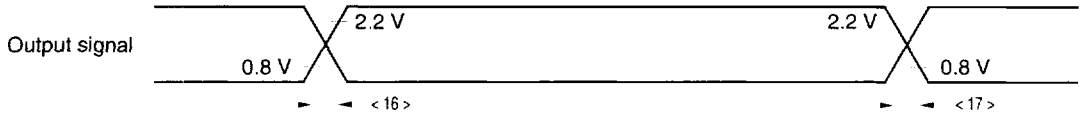
(b) Other than (a)

Parameter	Symbol	Condition	μPD70P3000-25		μPD70P3000-33		Unit
			MIN.	MAX.	MIN.	MAX.	
Input rise time	<14> t_{IR1}			10		10	ns
Input fall time	<15> t_{IF1}			10		10	ns



(3) Output waveform (other than CLKOUT)

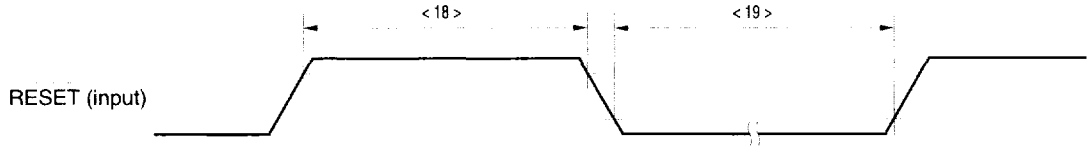
Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
Output rise time	<16>	t_{OR}			10		10	ns
Output fall time	<17>	t_{OF}			10		10	ns



(4) Reset timing

Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
RESET width, high	<18>	t_{WRSH}		500		500		ns
RESET width, low	<19>	t_{WRSL}	On power application, or on releasing STOP mode	500 + T_{OST}		500 + T_{OST}		ns
			Except on power application, or except on releasing STOP mode	500		500		ns

Remark T_{OST}: oscillation stabilization time



(5) Read timing (1/2)

Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
CLKOUT ↑→ address delay time	<20>	t_{DKA}		3	20	3	20	ns
CLKOUT ↑→ address float delay time	<21>	t_{FKA}		3	15	3	15	ns
CLKOUT ↓→ ASTB delay time	<22>	t_{DKST}		3	15	3	15	ns
CLKOUT ↓→ DSTB delay time	<23>	t_{DKD}		3	15	3	15	ns
CLKOUT ↑→ status delay time	<24>	t_{DKS}		3	15	3	15	ns
Data input setup time (vs. CLKOUT ↑)	<25>	t_{SIDK}		5		5		ns
Data input hold time (vs. CLKOUT ↑)	<26>	t_{HKID}		5		5		ns
WAIT setup time (vs. CLKOUT ↓)	<27>	t_{SWTK}		5		5		ns
WAIT hold time (vs. CLKOUT ↓)	<28>	t_{HKWT}		5		5		ns
Address hold time (vs. CLKOUT ↑)	<29>	t_{HKA}		0		0		ns
Address setup time (vs. ASTB ↓)	<30>	t_{SAST}		0.5 T – 10		0.5 T – 10		ns
Address hold time (vs. ASTB ↓)	<31>	t_{HSTA}		0.5 T – 10		0.5 T – 10		ns
DSTB ↓→ address float delay time	<32>	t_{FDA}			0		0	ns
Data input setup time (vs. address)	<33>	t_{SAID}			(2 + n) T – 20		(2 + n) T – 20	ns
Data input setup time (vs. DSTB ↓)	<34>	t_{SDID}			(1 + n) T – 20		(1 + n) T – 20	ns
ASTB ↓→ DSTB ↓ delay time	<35>	t_{DSTD}		0.5 T – 10		0.5 T – 10		ns
Data input hold time (vs. DSTB ↑)	<36>	t_{HDID}		0		0		ns
DSTB ↑→ address output delay time	<37>	t_{DDA}		(1 + i) T		(1 + i) T		ns
DSTB ↑→ ASTB ↑ delay time	<38>	t_{DDSTH}		0.5 T – 10		0.5 T – 10		ns
DSTB ↑→ ASTB ↓ delay time	<39>	t_{DDSTL}		(1.5 + i) T – 10		(1.5 + i) T – 10		ns
Status setup time (vs. ASTB ↓)	<40>	t_{SSST}		0.5 T – 10		0.5 T – 10		ns
Status hold time (vs. ASTB ↑)	<41>	t_{HSTS}		0.5 T – 10		0.5 T – 10		ns
DSTB width, low	<42>	t_{WDL}		(1 + n) T – 10		(1 + n) T – 10		ns
ASTB width, high	<43>	t_{WSTH}		T – 10		T – 10		ns
WAIT setup time (vs. address)	<44>	t_{SAWT1}	n ≥ 1		1.5 T – 20		1.5 T – 20	ns
	<45>	t_{SAWT2}			(1.5 + n) T – 20		(1.5 + n) T – 20	ns
WAIT hold time (vs. address)	<46>	t_{HAWT1}	n ≥ 1	(0.5 + n) T		(0.5 + n) T		ns
	<47>	t_{HAWT2}		(1.5 + n) T		(1.5 + n) T		ns
WAIT setup time (vs. ASTB ↓)	<48>	t_{SSTWT1}	n ≥ 1		T – 15		T – 15	ns
	<49>	t_{SSTWT2}			(1 + n) T – 15		(1 + n) T – 15	ns
WAIT hold time (vs. ASTB ↓)	<50>	t_{HSTWT1}	n ≥ 1	nT		nT		ns
	<51>	t_{HSTWT2}		(1 + n) T		(1 + n) T		ns

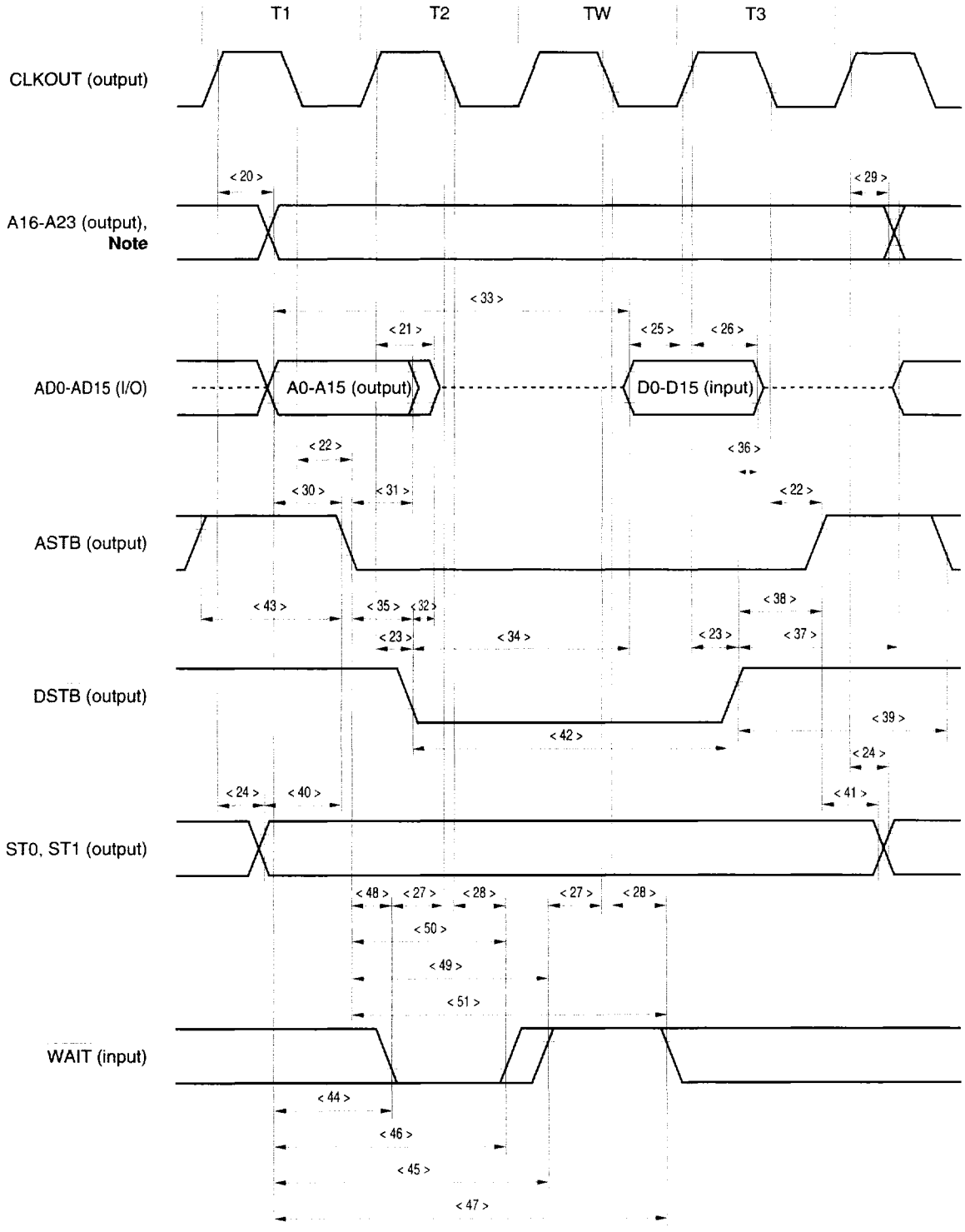
Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

3. i indicates the number of idle states (0 or 1) t be inserted in the read cycle.

4. Be sure to observe at least one of data input hold times t_{HKID} (<26>) and t_{HDID} (<36>).

(5) Read Timing (2/2): 1 wait



Note R/W (output), UBEN (output), LBEN (output)

Remark The broken line indicates the high-impedance state.

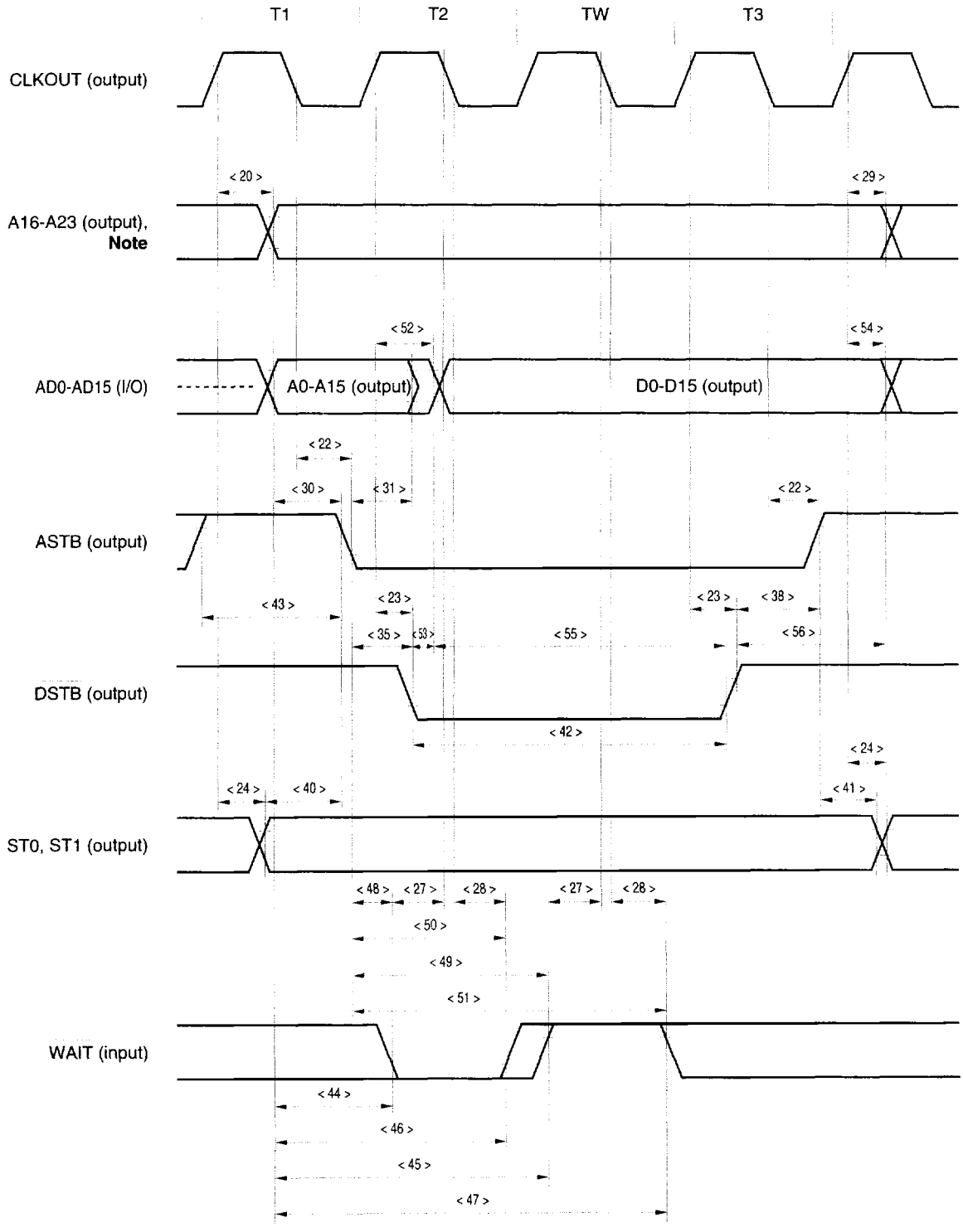
(6) Write timing (1/2)

Parameter		Symbol	Condition	μPD70P3000-25		μPD70P3000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
CLKOUT ↑→ address delay time	<20>	t_{DKA}		3	20	3	20	ns
CLKOUT ↓→ ASTB delay time	<22>	t_{DKST}		3	15	3	15	ns
CLKOUT ↑→ DSTB delay time	<23>	t_{DKD}		3	15	3	15	ns
CLKOUT ↑→ status delay time	<24>	t_{DKS}		3	15	3	15	ns
WAIT setup time (vs. CLKOUT ↓)	<27>	t_{SWTK}		5		5		ns
WAIT hold time (vs. CLKOUT ↓)	<28>	t_{HKWT}		5		5		ns
Address hold time (vs. CLKOUT ↑)	<29>	t_{HKA}		0		0		ns
Address setup time (vs. ASTB ↓)	<30>	t_{SAST}		0.5 T – 10		0.5 T – 10		ns
Address hold time (vs. ASTB ↓)	<31>	t_{HSTA}		0.5 T – 10		0.5 T – 10		ns
ASTB ↓→ DSTB ↓ delay time	<35>	t_{DSTD}		0.5 T – 10		0.5 T – 10		ns
DSTB ↑→ ASTB ↑ delay time	<38>	t_{DDSTH}		0.5 T – 10		0.5 T – 10		ns
Status setup time (vs. ASTB ↓)	<40>	t_{SSST}		0.5 T – 10		0.5 T – 10		ns
Status hold time (vs. ASTB ↑)	<41>	t_{HSTS}		0.5 T – 10		0.5 T – 10		ns
DSTB width, low	<42>	t_{WDL}		(1 + n) T – 10		(1 + n) T – 10		ns
ASTB width, high	<43>	t_{WSTH}		T – 10		T – 10		ns
WAIT setup time (vs. address)	<44>	t_{SAWT1}	n ≥ 1		1.5 T – 20		1.5 T – 20	ns
	<45>	t_{SAWT2}			(1.5 + n) T – 20		(1.5 + n) T – 20	ns
WAIT hold time (vs. address)	<46>	t_{HAWT1}	n ≥ 1	(0.5 + n) T		(0.5 + n) T		ns
	<47>	t_{HAWT2}		(1.5 + n) T		(1.5 + n) T		ns
WAIT setup time (vs. ASTB ↓)	<48>	t_{SSTWT1}	n ≥ 1		T – 15		T – 15	ns
	<49>	t_{SSTWT2}			(1 + n) T – 15		(1 + n) T – 15	ns
WAIT hold time (vs. ASTB ↓)	<50>	t_{HSTWT1}	n ≥ 1	nT		nT		ns
	<51>	t_{HSTWT2}		(1 + n) T		(1 + n) T		ns
CLKOUT ↑→ data output delay time	<52>	t_{DKOD}			20		20	ns
DSTB ↓→ data output delay time	<53>	t_{DDOD}			10		10	ns
Data output hold time (vs. CLKOUT ↑)	<54>	t_{HKOD}		0		0		ns
Data output setup time (vs. DSTB ↑)	<55>	t_{SODD}		(1 + n) T – 15		(1 + n) T – 15		ns
Data output hold time (vs. DSTB ↑)	<56>	t_{HDOD}		T – 10		T – 10		ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

(6) Write timing (2/2): 1 wait



Note R/W (output), UBEN (output), LBEN (output)

Remark The broken line indicates the high-impedance state.

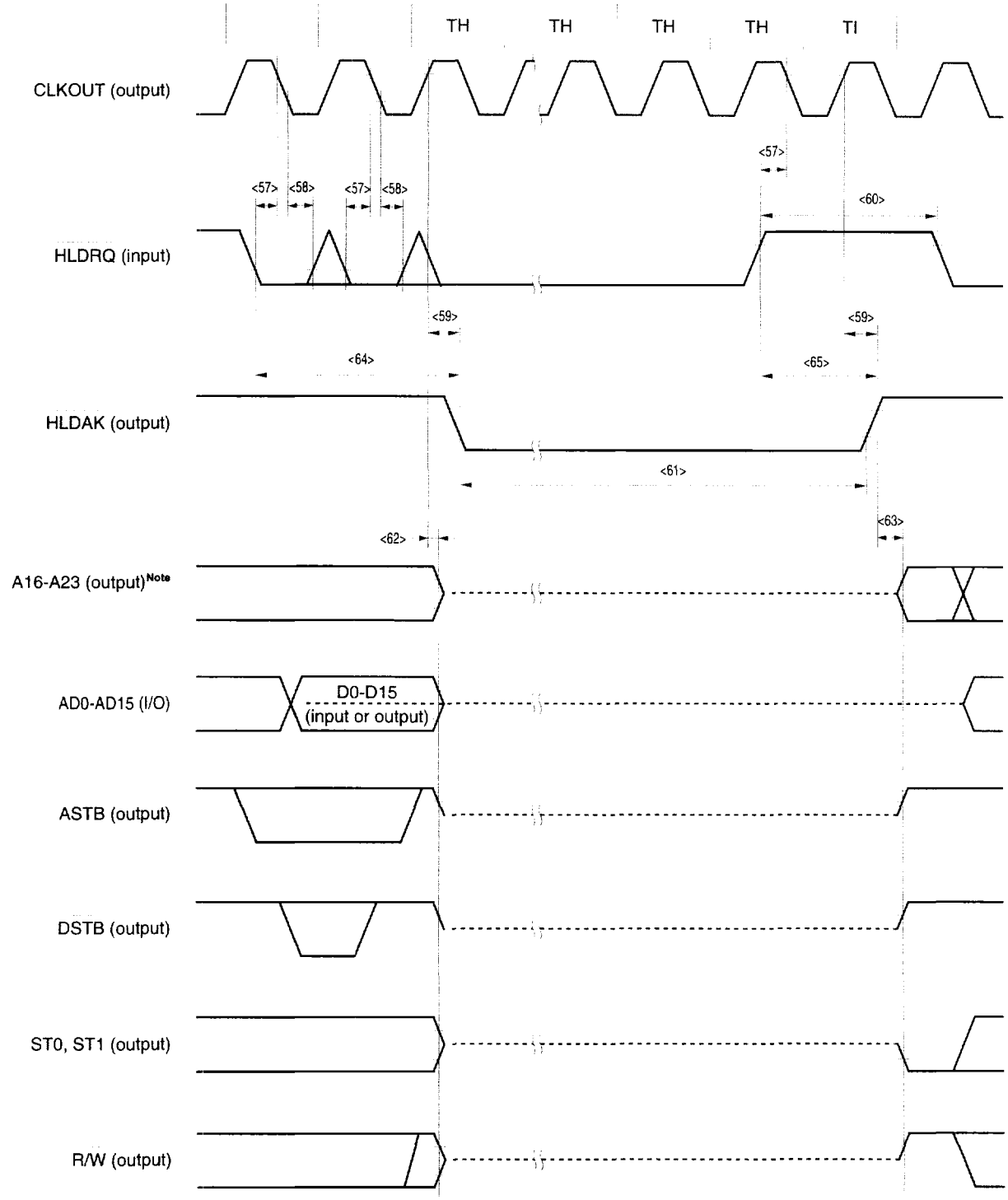
(7) Bus hold timing (1/2)

	Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
					MIN.	MAX.	MIN.	MAX.	
	HLDRQ setup time (vs. CLKOUT ↓)	<57>	t_{SHOK}		5		5		ns
	HLDRQ hold time (vs. CLKOUT ↓)	<58>	t_{HKHQ}		5		5		ns
	CLKOUT ↑→ HLDAK delay time	<59>	t_{DKHA}			20		20	ns
	HLDRQ width, high	<60>	t_{WHQH}		T + 10		T + 10		ns
	HLDAK width, low	<61>	t_{WHAL}		T – 10		T – 10		ns
★	CLKOUT ↑→ bus float delay time	<62>	t_{DKF}			20		20	ns
	HLDAK ↑→ bus output delay time	<63>	t_{DHAC}		–3		–3		ns
	HLDRQ ↓→ HLDAK ↓ delay time	<64>	t_{DHQHA1}			(2 n + 7.5) T + 20		(2 n + 7.5) T + 20	ns
	HLDRQ ↑→ HLDAK ↑ delay time	<65>	t_{DHQHA2}		0.5 T	1.5 T + 20	0.5 T	1.5 T + 20	ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

(7) Bus hold timing (2/2)



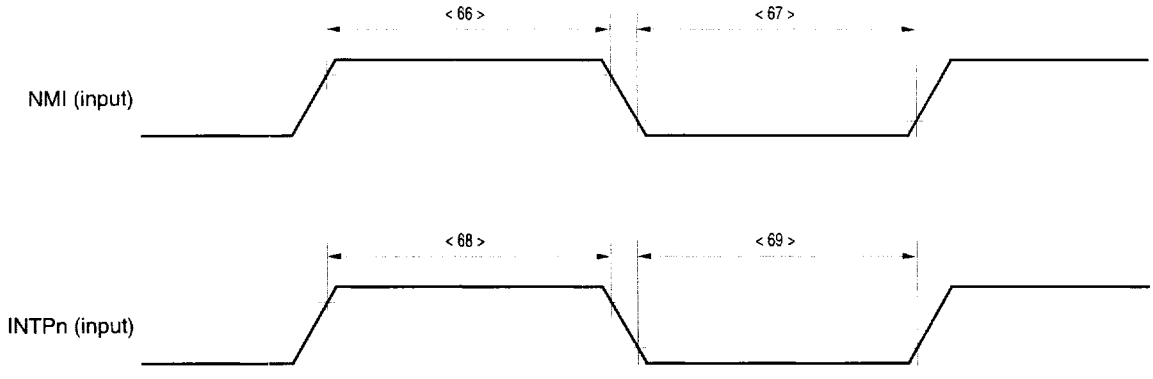
★ **Note** UBEN (output) and LBEN (output)

Remark The broken line indicates the high-impedance state.

(8) Interrupt timing

Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
NMI width, high	<66>	t_{WNIH}		500		500		ns
NMI width, low	<67>	t_{WNIL}		500		500		ns
INTPn width, high	<68>	t_{WITH}	n = 00, 01, 02, 03, 10, 11, 12, 13	3 T + 10		3 T + 10		ns
INTPn width, low	<69>	t_{WITL}	n = 00, 01, 02, 03, 10, 11, 12, 13	3 T + 10		3 T + 10		ns

Remark T = t_{CYK}



Remark n = 00, 01, 02, 03, 10, 11, 12, 13

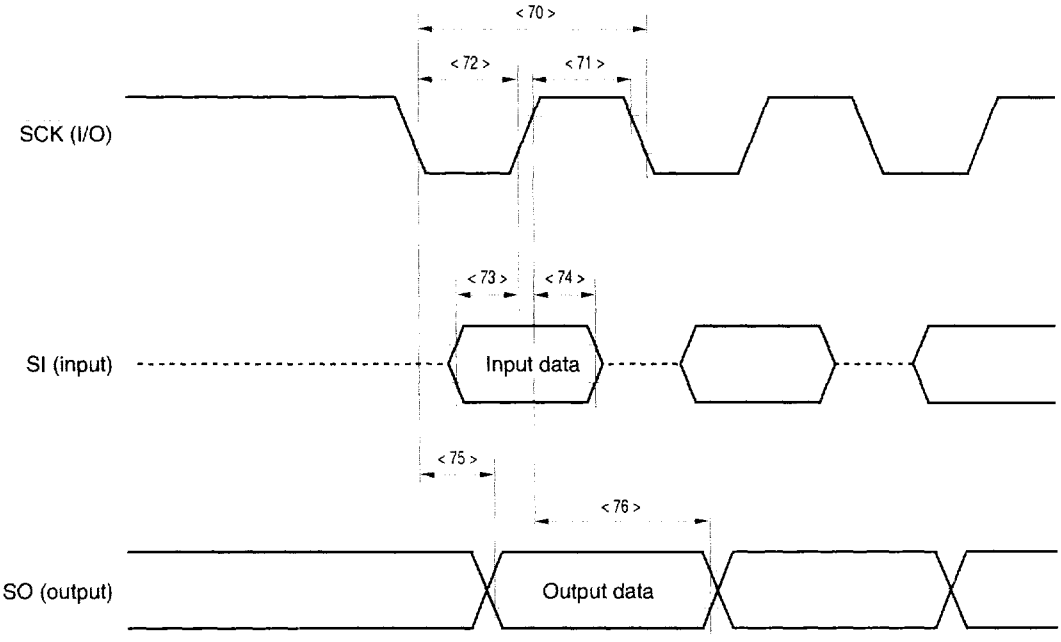
(9) CSI timing

(a) Master mode

Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
SCK cycle	<70>	t_{CYSK}	Output	160		120		ns
SCK width, high	<71>	t_{WSKH}	Output	0.5 t_{CYSK} – 20		0.5 t_{CYSK} – 20		ns
SCK width, low	<72>	t_{WSKL}	Output	0.5 t_{CYSK} – 20		0.5 t_{CYSK} – 20		ns
SI setup time (vs. SCK ↑)	<73>	t_{SSISK}		30		30		ns
SI hold time (vs. SCK ↑)	<74>	t_{HSKSI}		0		0		ns
SO output delay time (vs. SCK ↓)	<75>	t_{DSKSO}			18		18	ns
SO output hold time (vs. SCK ↑)	<76>	t_{HSKSO}		0.5 t_{CYSK} – 5		0.5 t_{CYSK} – 5		ns

(b) Slave mode

Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
SCK cycle	<70>	t_{CYSK}	Input	160		120		ns
SCK width, high	<71>	t_{WSKH}	Input	50		30		ns
SCK width, low	<72>	t_{WSKL}	Input	50		30		ns
SI setup time (vs. SCK ↑)	<73>	t_{SSISK}		10		10		ns
SI hold time (vs. SCK ↑)	<74>	t_{HSKSI}		10		10		ns
SO output delay time (vs. SCK ↓)	<75>	t_{DSKSO}			30		30	ns
SO output hold time (vs. SCK ↑)	<76>	t_{HSKSO}		t_{WSKH}		t_{WSKH}		ns

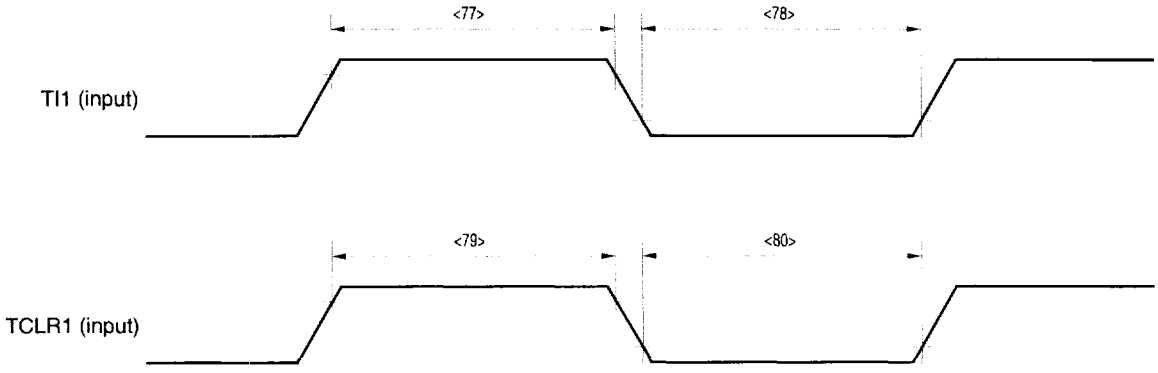


Remark The broken line indicates the high-impedance state.

(10) RPU timing

Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
TI1 width, high	<77>	t_{WTIH}		3 T + 10		3 T + 10		ns
TI1 width, low	<78>	t_{WTIL}		3 T + 10		3 T + 10		ns
TCLR1 width, high	<79>	t_{WTCH}		3 T + 10		3 T + 10		ns
TCLR1 width, low	<80>	t_{WTCL}		3 T + 10		3 T + 10		ns

Remark T = t_{CYK}



6.1.2 When V_{DD} = 3.0 to 3.6 V

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage	V_{DD}	V_{DD} pin	−0.5 to +7.0	V
	CV_{DD}	CV_{DD} pin	−0.5 to +7.0	V
	DVss	CVss pin	−0.5 to +0.5	V
Input voltage	V_{I1}	Except X1 pin, V_{DD} = 3.0 to 3.6 V	−0.5 to V_{DD} + 0.3	V
	V_{I2}	V_{PP} pin in PROM programming mode, V_{DD} = 3.0 to 3.6 V	−0.5 to +13.5	V
Clock input voltage	V_X	X1 pin, V_{DD} = 3.0 to 3.6 V	−0.5 to V_{DD} + 1.0	V
Output current, low	I_{OL}	1 pin	4.0	mA
		Total of all pins	100	mA
Output current, high	I_{OH}	1 pin	−4.0	mA
		Total of all pins	−100	mA
Output voltage	V_O	V_{DD} = 3.0 to 3.6 V	−0.5 to V_{DD} + 0.3	V
Operating ambient temperature	T_A		−20 to +70	°C
Storage temperature	T_{stg}		−65 to +150	°C

Cautions 1. Do not directly connect the output (or I/O) pins of two or more IC products, and do not directly connect them to V_{DD}, Vcc, or GND pin. Open-drain pins and open-collector pins may be directly connected to one another however. Moreover, an external circuit that is designed to prevent contention of output can be connected to pins that go into a high-impedance state.

2. Should the absolute maximum rating of even one of the above parameters be exceeded even momentarily, the quality of the product may be degraded. The absolute maximum ratings are, therefore, the values exceeding which the product may be physically damaged. Use the product so that these values are never exceeded.

The normal operating ranges of ratings and conditions in which the quality of the product is guaranteed are specified in the following DC Characteristics and AC Characteristics.

Capacitance (T_A = 25 °C, V_{DD} = Vss = 0 V)

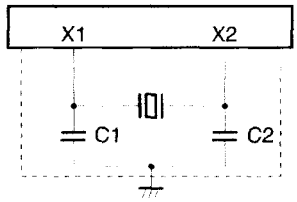
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	fc = 1 MHz			15	pF
I/O capacitance	C_{IO}	Pins other than tested pin: 0 V			15	pF
Output capacitance	C_O				15	pF

Operating Conditions

Operation Mode	Internal Operating Clock Frequency (φ)	Operating Temperature (T_A)	Supply Voltage (V_{DD})
Direct mode	0 to 12 MHz	−20 to +70 °C	3.0 to 3.6 V
PLL mode	Self oscillation frequency to 12 MHz	−20 to +70 °C	3.0 to 3.6 V

Recommended Oscillation Circuit

(a) Ceramic resonator connection (T_A = –40 to + 85 °C)



Manufacturer	Part Number	Oscillation Frequency fxx (MHz)	Recommended Circuit Constants C1 (pF)	Recommended Circuit Constants C2 (pF)	Oscillation Voltage Renge MIN. (V)	Oscillation Voltage Renge MAX. (V)	Oscillation Stabilization Time (MAX.) TOST (ms)
TDK Corp	FCR2.0MC3	2.0	Provided	Provided	3.0	3.6	0.26
	CCR3.2MC3	3.2	Provided	Provided	3.0	3.6	0.62
Murata Mfg. Co., Ltd.	CSA2.00MG	2.0	30	30	2.7	3.6	0.24
	CST2.00MG	2.0	Provided	Provided	2.7	3.6	0.24
	CSA2.70MG	2.7	30	30	2.7	3.6	0.16
	CST2.70MGW	2.7	Provided	Provided	2.7	3.6	0.16
	CSA3.20MG	3.2	30	30	2.7	3.6	0.13
	CST3.20MGW	3.2	Provided	Provided	2.7	3.6	0.13

Cautions 1. *Connect the oscillation circuit as closely to X2 pin as possible.*

2. *Do not route any other signal lines in the range indicated by the broken line in the above figure.*

3. Thoroughly evaluate the matching between the μPD70P3000 and resonator.

(b) External clock input

External clock

Caution Input CMOS level voltage to the X1 pin.

DC Characteristics (T_A = −20 to +70 °C, V_{DD} = 3.0 to 3.6 V, V_{SS} = 0 V)

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, high		V_{IH}	Except X1 and **Note**	0.7 V_{DD}		V_{DD}	V
			Note	0.8 V_{DD}		V_{DD}	V
Input voltage, low		V_{IL}	Except X1 and **Note**	0		0.2 V_{DD}	V
			Note	0		0.2 V_{DD}	V
X1 clock input voltage, high		V_{XH}	Direct mode	0.8 V_{DD}		V_{DD}	V
			PLL mode	0.8 V_{DD}		V_{DD}	V
X1 clock input voltage, low		V_{XL}	Direct mode	0		0.6	V
			PLL mode	0		0.6	V
Schmitt trigger input threshold voltage		V_{T}^{+}	**Note**, rising		3.0		V
		V_{T}^{-}	**Note**, falling		2.0		V
Schmitt trigger input hysteresis width		$V_{T}^{+} - V_{T}^{-}$	**Note**	0.5			V
Output voltage, high		V_{OH}	I_{OH} = −2.5 mA	0.7 V_{DD}			V
			I_{OH} = −100 μA	V_{DD} − 0.5			V
Output voltage, low		V_{OL}	I_{OL} = 2.5 mA			0.45	V
Input leakage current, high		I_{LIH}	V_I = V_{DD}			10	μA
Input leakage current, low		I_{LIL}	V_I = 0 V			−10	μA
Output leakage current, high		I_{LOH}	V_O = V_{DD}			10	μA
Output leakage current, low		I_{LOL}	V_O = 0 V			−10	μA
Supply current	Operating	I_{DD1}	Direct mode		1.0 × ϕ + 9.5	1.5 × ϕ + 10	mA
			PLL mode		1.1 × ϕ + 11	1.8 × ϕ + 12	mA
	In HALT mode	I_{DD2}	Direct mode		0.3 × ϕ + 2	0.5 × ϕ + 6.5	mA
			PLL mode		0.4 × ϕ + 3.5	0.6 × ϕ + 8.5	mA
	In IDLE mode	I_{DD3}	Direct mode		5.3 × ϕ + 200	6.5 × ϕ + 325	μA
			PLL mode		0.07 × ϕ + 1.5	0.15 × ϕ + 2	mA
	In STOP mode	I_{DD4}	−20 °C ≤ T_A ≤ 50 °C		1	40	μA
			50 °C < T_A ≤ 70 °C			200	μA

Note RESET, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26, P27, P31/SI, P32/SCK, P36, P37, MODE0, MODE1, CKSEL

Remarks 1. TYP. value is a value for your reference at T_A = 25 °C and V_{DD} = 3.3 V.

2. ϕ : Internal operating clock frequency

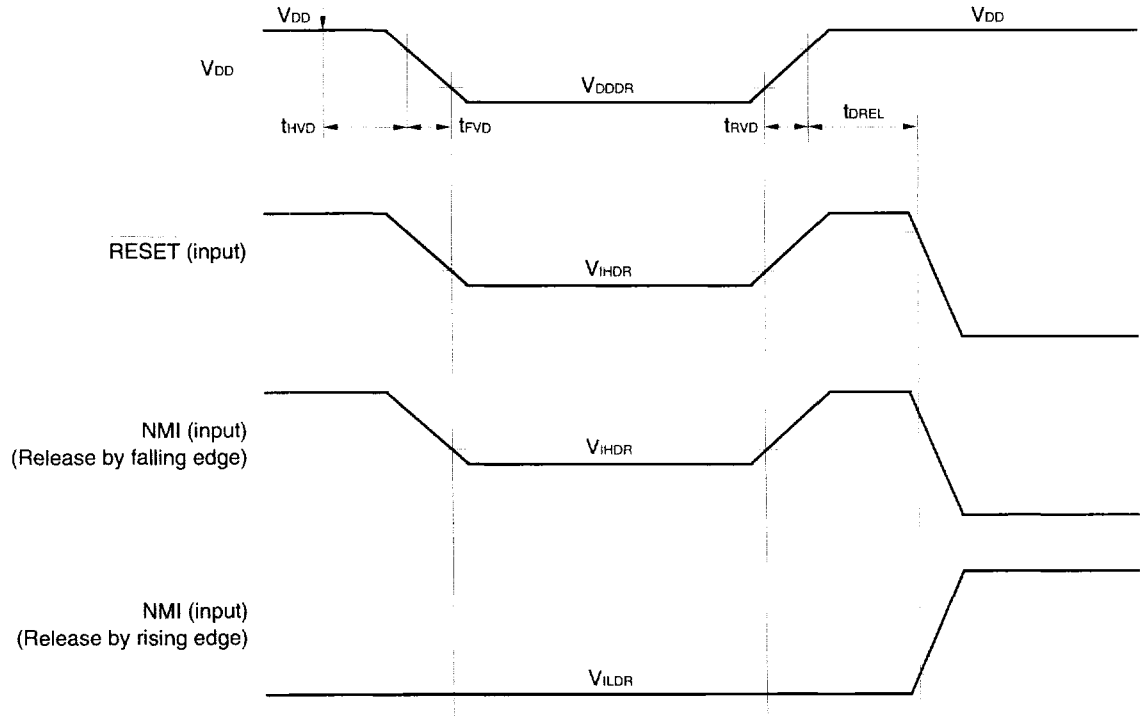
Data Retention Characteristics (T_A = –20 to +70 °C)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Data hold voltage	V_{DDDR}	STOP mode		1.5		3.6	V
Data hold current	I_{DDDR}	$V_{DD} = V_{DDDR}$	–20 °C ≤ T_A ≤ +50 °C		0.2 V_{DDDR}	40	μA
			50 °C < T_A ≤ 70 °C		0.2 V_{DDDR}	200	μA
Supply voltage rise time	t_{RVD}			200			μs
Supply voltage fall time	t_{FVD}			200			μs
Supply voltage hold time (vs. STOP mode setting)	t_{HVD}			0			ms
STOP mode release signal input time	t_{DREL}			0			ns
Data hold input voltage, high	V_{IHDR}	**Note**		0.9 V_{DDDR}		V_{DDDR}	V
Data hold input voltage, low	V_{ILDR}	**Note**		0		0.1 V_{DDDR}	V

Note RESET, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INT03, P26, P27, P31/SI, P32/SCK, P36, P37, MODE0, MODE1, CKSEL, X1

Remark TYP. value is a value for your reference at T_A = 25 °C and V_{DD} = 3.3 V.

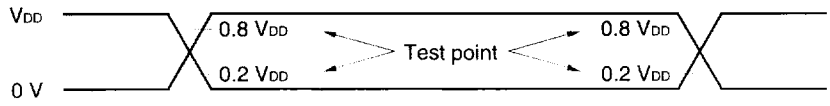
STOP mode is set (at fifth clock after PSC register has been set).



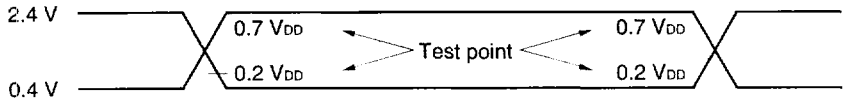
AC Characteristics (T_A = –20 to +70 °C, V_{DD} = 3.0 to 3.6 V, V_{SS} = 0 V)

AC test input wave

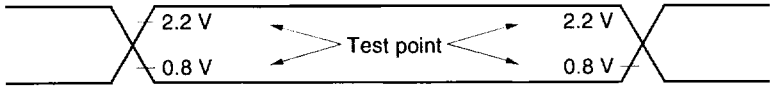
(a) RESET, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26, P27, P31/SI, P32/SCK, P36, P37, MODE0, MODE1, CKSEL, X1



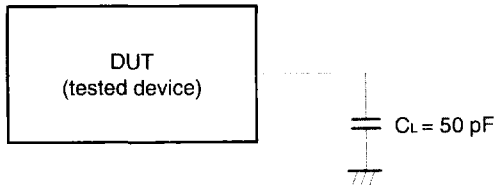
(b) Other than (a)



AC test output test point



Load condition



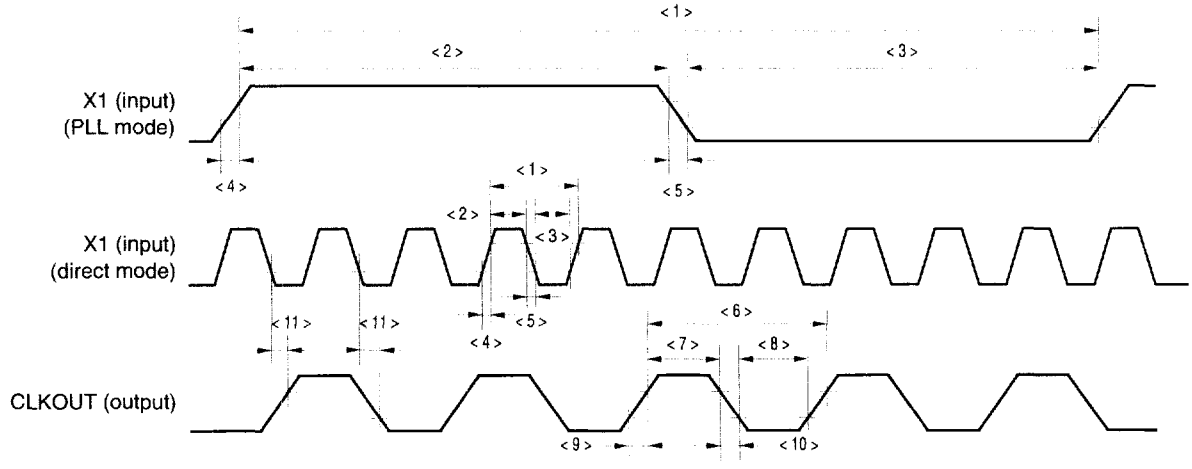
Caution If the load capacitance exceeds 50 pF due to the circuit configuration, decrease the load capacitance of this device to less then 50 pF by using a buffer.

(1) Clock timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
X1 input cycle	<1>	t_{CYX}	Direct mode	41	DC	ns
			PLL mode	416	500	ns
X1 input width, high	<2>	t_{WXH}	Direct mode	7		ns
			PLL mode	170		ns
X1 input width, low	<3>	t_{WXL}	Direct mode	7		ns
			PLL mode	170		ns
X1 input rise time	<4>	t_{XR}	Direct mode		7	ns
			PLL mode		15	ns
X1 input fall time	<5>	t_{XF}	Direct mode		7	ns
			PLL mode		15	ns
CPU operating frequency	—	ϕ		0	12	MHz
CLKOUT output cycle	<6>	t_{CYK}		82	DC	ns
CLKOUT width, high	<7>	t_{WKH}		0.5 T – 15		ns
CLKOUT width, low	<8>	t_{WKL}		0.5 T – 15		ns
CLKOUT rise time	<9>	t_{XR}			15	ns
CLKOUT fall time	<10>	t_{XF}			15	ns
X1 ↓→ CLKOUT delay time	<11>	t_{DXK}	Direct mode	3	30	ns

Remark T = t_{CYK}

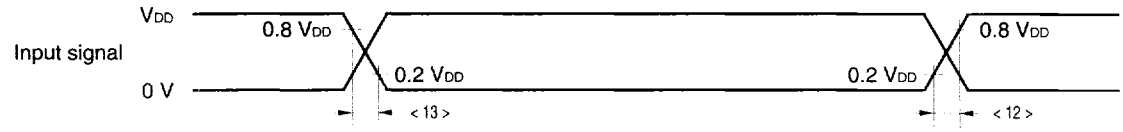
Parameter	Symbol		Condition	TYP.	Unit
Self-running oscillation frequency	—	ϕ_P	PLL mode	2.8	MHz



(2) Input waveform

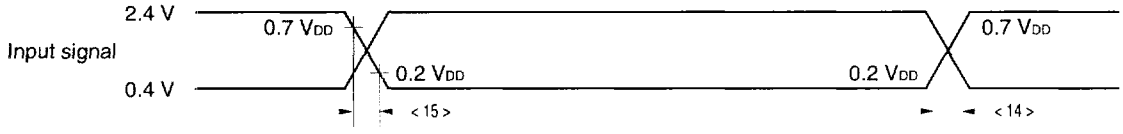
(a) RESET, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26, P27, P31/SI, P32/SCK, P36, P37, MODE0, MODE1, CKSEL, X1

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input rise time	<12> t_{IR2}			20	ns
Input fall time	<13> t_{IF2}			20	ns



(b) Other than (a)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input rise time	<14> t_{IR1}			10	ns
Input fall time	<15> t_{IF1}			10	ns



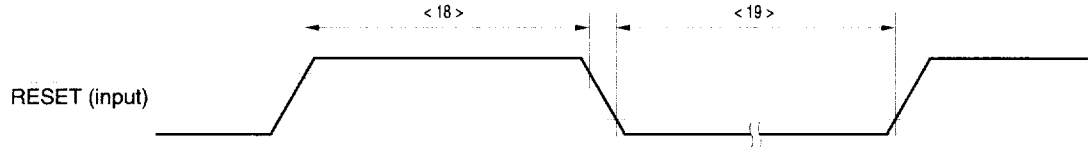
(3) Output waveform (other than CLKOUT)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Output rise time	<16> t_{OR}			20	ns
Output fall time	<17> t_{OF}			20	ns

(4) Reset timing

Parameter	Symbol	Condition	MIN.	MAX.	Unit
RESET width, high	<18> t_{WRSH}		500		ns
RESET width, low	<19> t_{WRSL}	On power application, or on releasing STOP mode	500 + T_{OST}		ns
		Except on power application, or except on releasing STOP mode	500		ns

Remark T_{OST}: oscillation stabilization time



[MEMO]

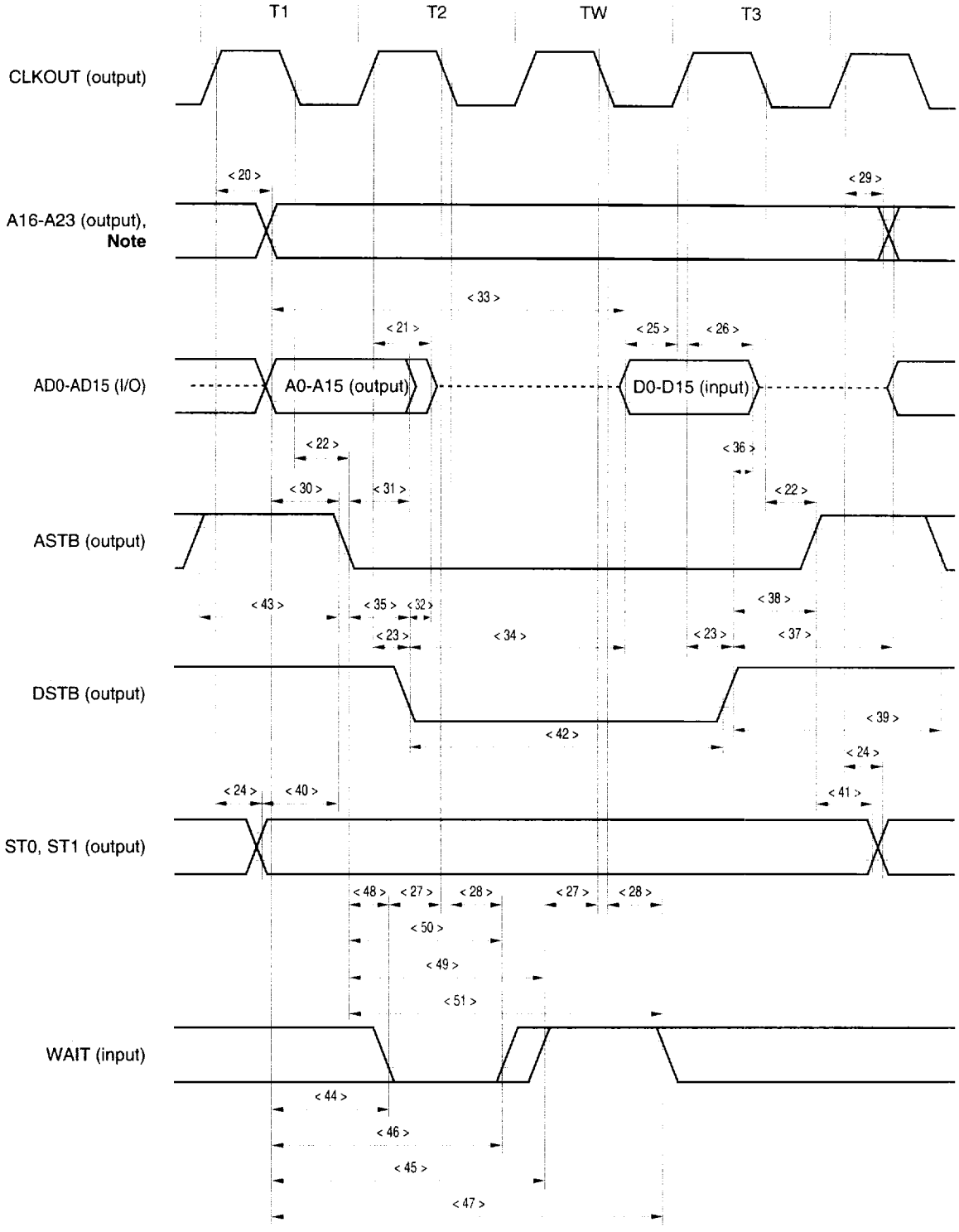
(5) Read timing (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
CLKOUT ↑→ address delay time	<20>	t_{DKA}		3	32	ns
CLKOUT ↑→ address float delay time	<21>	t_{FKA}		3	32	ns
CLKOUT ↓→ ASTB delay time	<22>	t_{DKST}		3	32	ns
CLKOUT ↓→ DSTB delay time	<23>	t_{DKD}		3	32	ns
CLKOUT ↑→ status delay time	<24>	t_{DKS}		3	32	ns
Data input setup time (vs. CLKOUT ↑)	<25>	t_{SIDK}		5		ns
Data input hold time (vs. CLKOUT ↑)	<26>	t_{HKID}		5		ns
WAIT setup time (vs. CLKOUT ↓)	<27>	t_{SWTK}		7		ns
WAIT hold time (vs. CLKOUT ↓)	<28>	t_{HKWT}		7		ns
Address hold time (vs. CLKOUT ↑)	<29>	t_{HKA}		0		ns
Address setup time (vs. ASTB ↓)	<30>	t_{SAST}		0.5 T – 25		ns
Address hold time (vs. ASTB ↓)	<31>	t_{HSTA}		0.5 T – 25		ns
DSTB ↓→ address float delay time	<32>	t_{FDA}			0	ns
Data input setup time (vs. address)	<33>	t_{SAID}			(2 + n) T – 45	ns
Data input setup time (vs. DSTB ↓)	<34>	t_{SDID}			(1 + n) T – 35	ns
ASTB ↓→ DSTB ↓ delay time	<35>	t_{DSTD}		0.5 T – 15		ns
Data input hold time (vs. DSTB ↑)	<36>	t_{HDID}		0		ns
DSTB ↑→ address output delay time	<37>	t_{DDA}		(1 + i) T		ns
DSTB ↑→ ASTB ↑ delay time	<38>	t_{DDSTH}		0.5 T – 15		ns
DSTB ↑→ ASTB ↓ delay time	<39>	t_{DDSTL}		(1.5 + i) T – 15		ns
Status setup time (vs. ASTB ↓)	<40>	t_{SSST}		0.5 T – 15		ns
Status hold time (vs. ASTB ↑)	<41>	t_{HSTS}		0.5 T – 20		ns
DSTB width, low	<42>	t_{WDL}		(1 + n) T – 15		ns
ASTB width, high	<43>	t_{WSTH}		T – 20		ns
WAIT setup time (vs. address)	<44>	t_{SAWT1}	n ≥ 1		1.5 T – 50	ns
	<45>	t_{SAWT2}			(1.5 + n) T – 50	ns
WAIT hold time (vs. address)	<46>	t_{HAWT1}	n ≥ 1	(0.5 + n) T		ns
	<47>	t_{HAWT2}		(1.5 + n) T		ns
WAIT setup time (vs. ASTB ↓)	<48>	t_{SSTWT1}	n ≥ 1		T – 35	ns
	<49>	t_{SSTWT2}			(1 + n) T – 35	ns
WAIT hold time (vs. ASTB ↓)	<50>	t_{HSTWT1}	n ≥ 1	nT		ns
	<51>	t_{HSTWT2}		(1 + n) T		ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.
3. i indicates the number of idle states (0 or 1) t be inserted in the read cycle.
4. Be sure to observe at least one of data input hold times t_{HKID} (<26>) and t_{HDID} (<36>).

(5) Read Timing (2/2): 1 wait



Note R/W (output), UBEN (output), LBEN (output)

Remark The broken line indicates the high-impedance state.

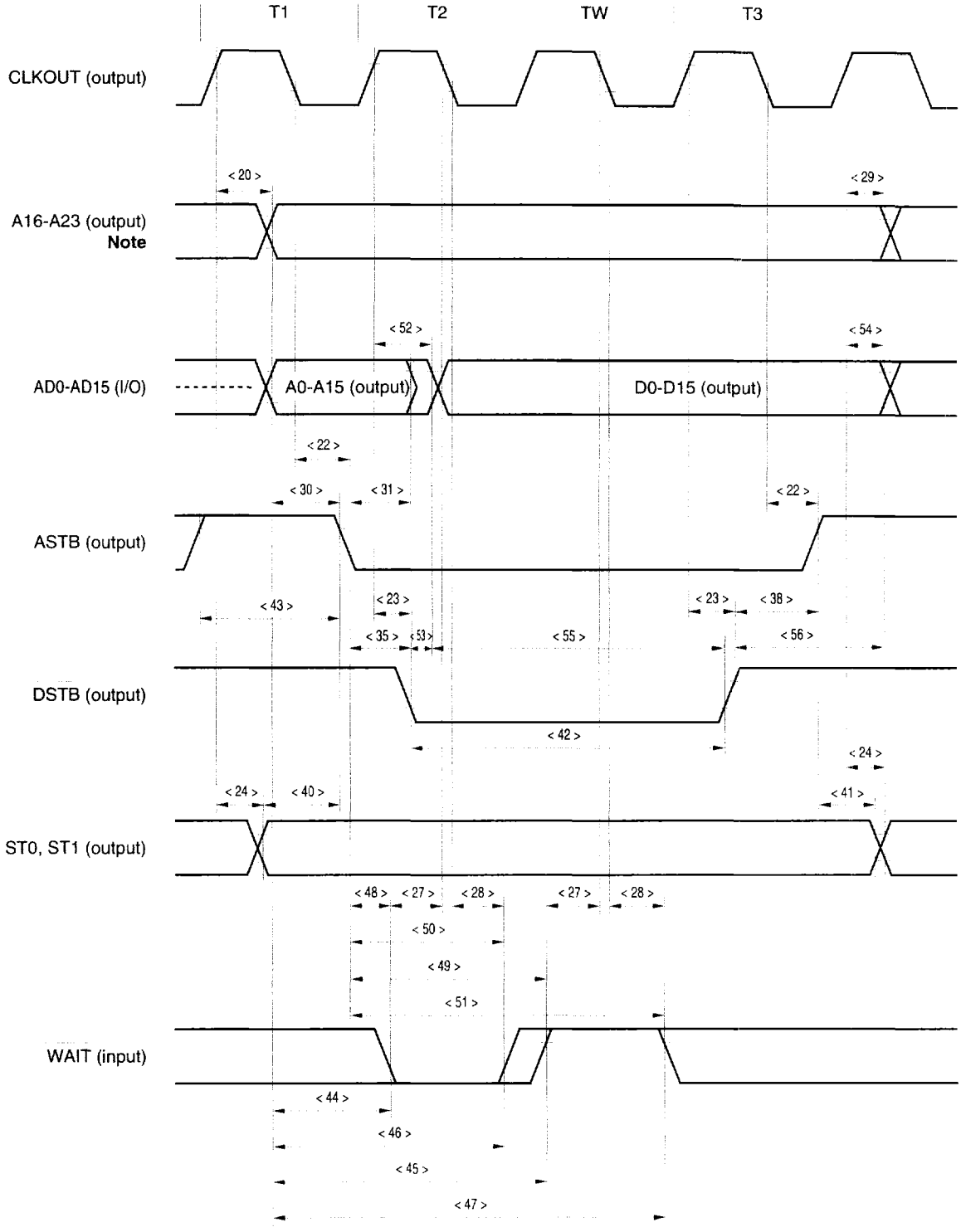
(6) Write timing (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
CLKOUT ↑→ address delay time	<20>	t_{DKA}		3	32	ns
CLKOUT ↓→ ASTB delay time	<22>	t_{DKST}		3	32	ns
CLKOUT ↑→ DSTB delay time	<23>	t_{DKD}		3	32	ns
CLKOUT ↑→ status delay time	<24>	t_{DKS}		3	32	ns
WAIT setup time (vs. CLKOUT ↓)	<27>	t_{SWTK}		7		ns
WAIT hold time (vs. CLKOUT ↓)	<28>	t_{HKWT}		7		ns
Address hold time (vs. CLKOUT ↑)	<29>	t_{HKA}		0		ns
Address setup time (vs. ASTB ↓)	<30>	t_{SAST}		0.5 T – 25		ns
Address hold time (vs. ASTB ↓)	<31>	t_{HSTA}		0.5 T – 15		ns
ASTB ↓→ DSTB ↓ delay time	<35>	t_{DSTD}		0.5 T – 15		ns
DSTB ↑→ ASTB ↑ delay time	<38>	t_{DDSTH}		0.5 T – 15		ns
Status setup time (vs. ASTB ↓)	<40>	t_{SSST}		0.5 T – 15		ns
Status hold time (vs. ASTB ↑)	<41>	t_{HSTS}		0.5 T – 20		ns
DSTB width, low	<42>	t_{WDL}		(1 + n) T – 15		ns
ASTB width, high	<43>	t_{WSTH}		T – 20		ns
WAIT setup time (vs. address)	<44>	t_{SAWT1}	n ≥ 1		1.5 T – 50	ns
	<45>	t_{SAWT2}			(1.5 + n) T – 50	ns
WAIT hold time (vs. address)	<46>	t_{HAWT1}	n ≥ 1	(0.5 + n) T		ns
	<47>	t_{HAWT2}		(1.5 + n) T		ns
WAIT setup time (vs. ASTB ↓)	<48>	t_{SSTWT1}	n ≥ 1		T – 35	ns
	<49>	t_{SSTWT2}			(1 + n) T – 35	ns
WAIT hold time (vs. ASTB ↓)	<50>	t_{HSTWT1}	n ≥ 1	nT		ns
	<51>	t_{HSTWT2}		(1 + n) T		ns
CLKOUT ↑→ data output delay time	<52>	t_{DKOD}			32	ns
DSTB ↓→ data output delay time	<53>	t_{DDOD}			20	ns
Data output hold time (vs. CLKOUT ↑)	<54>	t_{HKOD}		0		ns
Data output setup time (vs. DSTB ↑)	<55>	t_{SODD}		(1 + n) T – 30		ns
Data output hold time (vs. DSTB ↑)	<56>	t_{HDOD}		T – 15		ns

Remarks 1. $T = t_{CYK}$

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

(6) Write timing (2/2): 1 wait



Note R/W (output), UBEN (output), LBEN (output)

Remark The broken line indicates the high-impedance state.

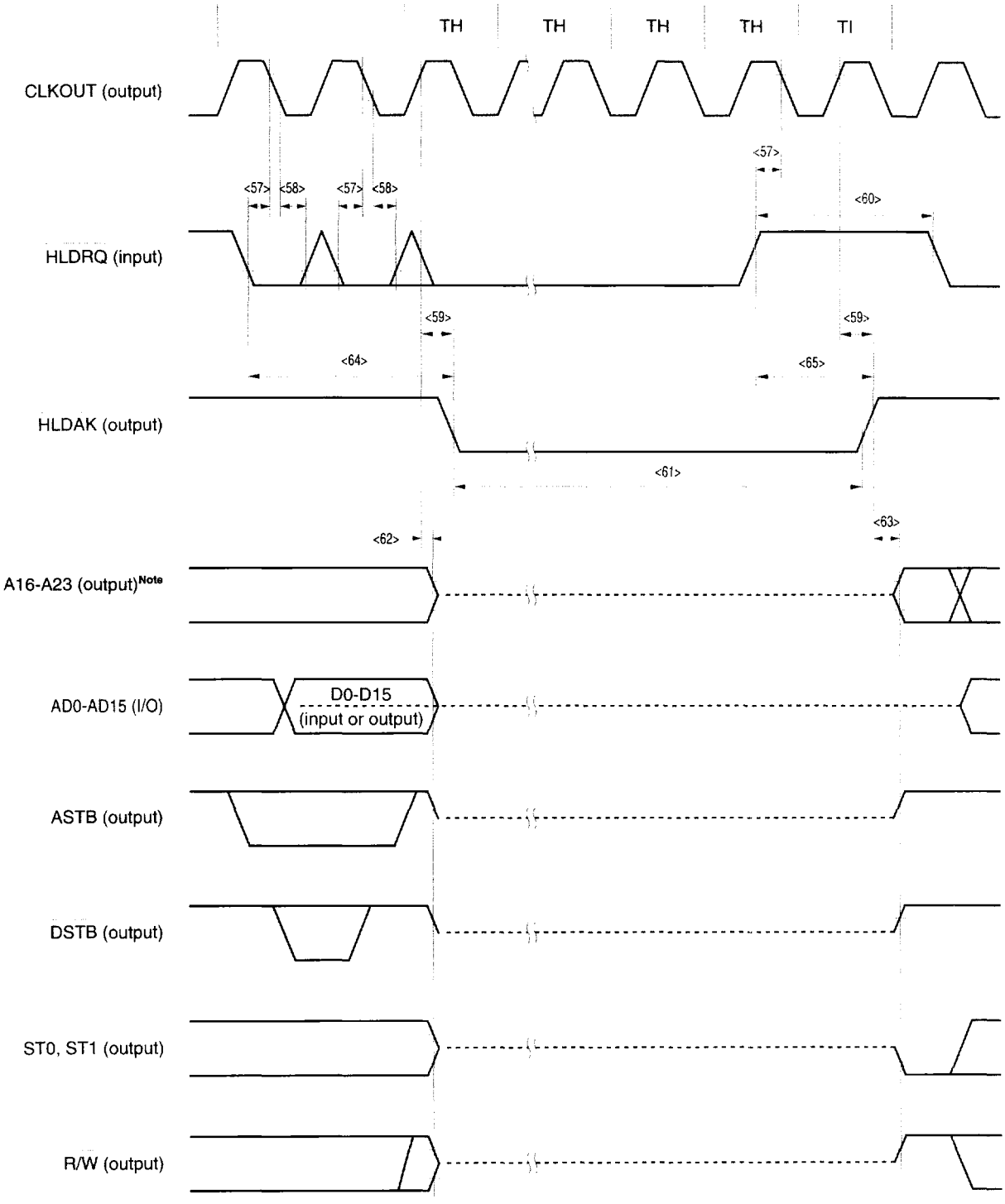
(7) Bus hold timing (1/2)

	Parameter	Symbol		Condition	MIN.	MAX.	Unit
	HLDRQ setup time (vs. CLKOUT ↓)	<57>	t_{SHOK}		7		ns
	HLDRQ hold time (vs. CLKOUT ↓)	<58>	t_{HKHQ}		7		ns
	CLKOUT ↑→ HLDAK delay time	<59>	t_{DKHA}			32	ns
	HLDRQ width, high	<60>	t_{WHQH}		T + 15		ns
	HLDAK width, low	<61>	t_{WHAL}		T – 15		ns
★	CLKOUT ↑→ bus float delay time	<62>	t_{DKF}			32	ns
	HLDAK ↑→ bus output delay time	<63>	t_{DHAC}		–5		ns
	HLDRQ ↓→ HLDAK ↓ delay time	<64>	t_{DHQHA1}			(2 n + 7.5) T + 40	ns
	HLDRQ ↑→ HLDAK ↑ delay time	<65>	t_{DHQHA2}		0.5 T	1.5 T + 40	ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

(7) Bus hold timing (2/2)



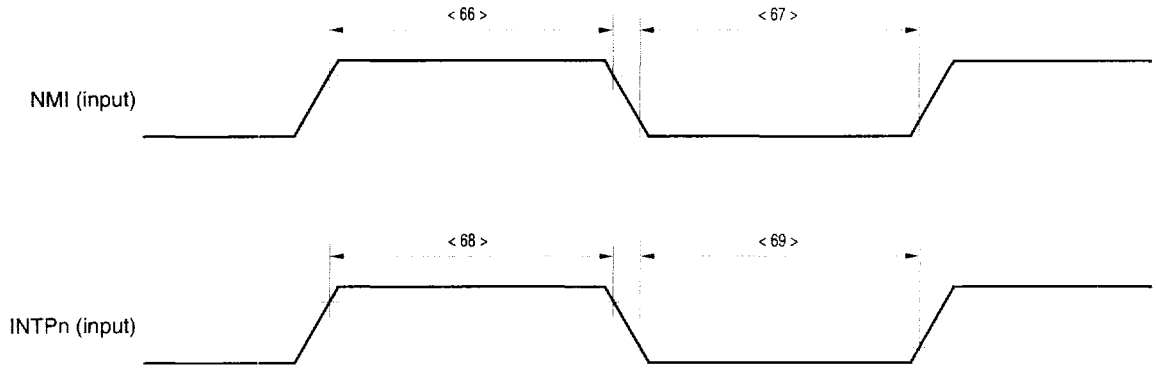
★ **Note** UBEN (output) and LBEN (output)

Remark The broken line indicates the high-impedance state.

(8) Interrupt timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
NMI width, high	<66>	t_{WNIH}		500		ns
NMI width, low	<67>	t_{WNIL}		500		ns
INTPn width, high	<68>	t_{WITH}	n = 00, 01, 02, 03, 10, 11, 12, 13	3 T + 10		ns
INTPn width, low	<69>	t_{WITL}	n = 00, 01, 02, 03, 10, 11, 12, 13	3 T + 10		ns

Remark T = t_{CYK}



Remark n = 00, 01, 02, 03, 10, 11, 12, 13

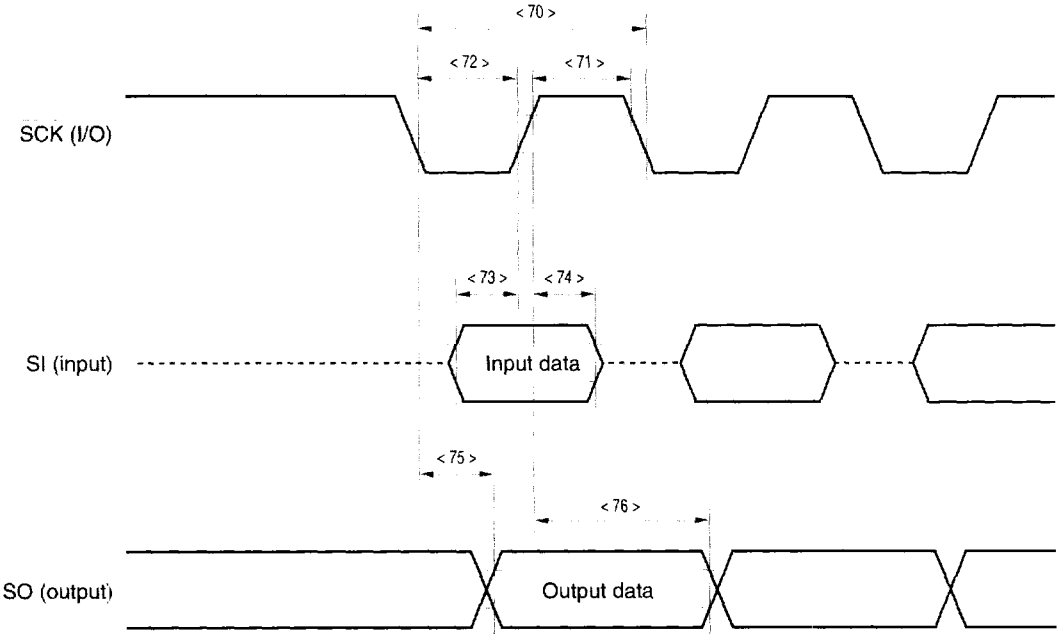
(9) CSI timing

(a) Master mode

Parameter	Symbol		Condition	MIN.	MAX.	Unit
SCK cycle	<70>	t_{CYSK}	Output	330		ns
SCK width, high	<71>	t_{WSKH}	Output	0.5 t_{CYSK} − 40		ns
SCK width, low	<72>	t_{WSKL}	Output	0.5 t_{CYSK} − 40		ns
SI setup time (vs. SCK ↑)	<73>	t_{SSISK}		60		ns
SI hold time (vs. SCK ↑)	<74>	t_{HSKSI}		0		ns
SO output delay time (vs. SCK ↓)	<75>	t_{DSKSO}			40	ns
SO output hold time (vs. SCK ↑)	<76>	t_{HSKSO}		0.5 t_{CYSK} − 15		ns

(b) Slave mode

Parameter	Symbol		Condition	MIN.	MAX.	Unit
SCK cycle	<70>	t_{CYSK}	Input	330		ns
SCK width, high	<71>	t_{WSKH}	Input	110		ns
SCK width, low	<72>	t_{WSKL}	Input	110		ns
SI setup time (vs. SCK ↑)	<73>	t_{SSISK}		20		ns
SI hold time (vs. SCK ↑)	<74>	t_{HSKSI}		20		ns
SO output delay time (vs. SCK ↓)	<75>	t_{DSKSO}			60	ns
SO output hold time (vs. SCK ↑)	<76>	t_{HSKSO}		t_{WSKH}		ns

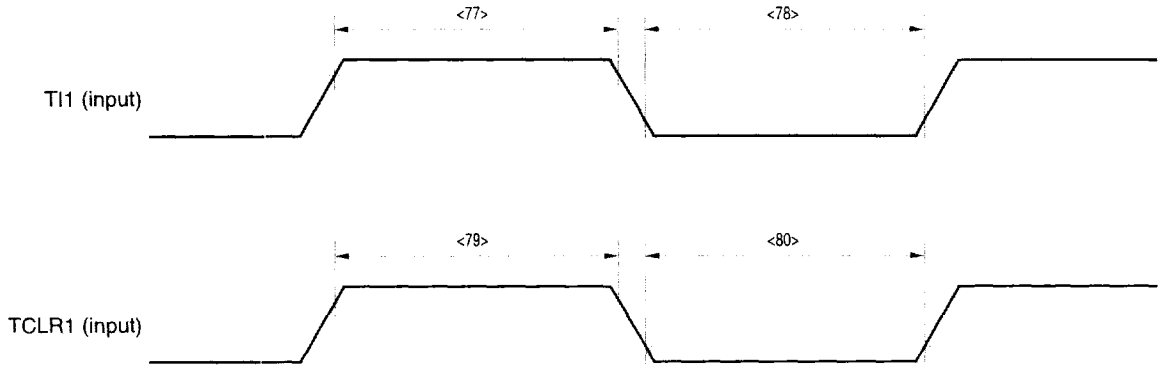


Remark The broken line indicates the high-impedance state.

(10) RPU timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
TI1 width, high	<77>	t_{WTIH}		3 T + 10		ns
TI1 width, low	<78>	t_{WTIL}		3 T + 10		ns
TCLR1 width, high	<79>	t_{WTCH}		3 T + 10		ns
TCLR1 width, low	<80>	t_{WTCL}		3 T + 10		ns

Remark T = t_{CYK}



6.2 PROM Programming Mode

DC Programming Characteristics

PROM write mode (T_A = 25 ± 5 °C, V_{DD} = 6.5 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V)

Parameter	Symbol	Symbol[Note]	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		0.7 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL}	V_{IL}		0		0.3 V_{DD}	V
Output voltage, high	V_{OH}	V_{OH}	I_{OH} = −1 mA	V_{DD} − 1.0			V
Output voltage, low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 ≤ V_{IN} ≤ V_{DD}	−10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		12.2	12.5	12.8	V
V_{DD} supply voltage	V_{DD}	V_{CC}		6.25	6.5	6.75	V
V_{PP} supply current	I_{PP}	I_{PP}	PGM = V_{IL}			50	mA
V_{DD} supply current	I_{DD}	I_{CC}				50	mA

Note Symbol of corresponding μPD27C1001A

PROM read mode (T_A = 25 ± 5 °C, V_{DD} = 5.0 ± 0.5 V, V_{PP} = V_{DD} ± 0.6 V)

Parameter	Symbol	Symbol[Note]	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		0.7 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL}	V_{IL}		0		0.3 V_{DD}	V
Output voltage, high	V_{OH1}	V_{OH1}	I_{OH} = −1 mA	V_{DD} − 1.0			V
	V_{OH2}	V_{OH2}	I_{OH} = −100 μA	V_{DD} − 0.5			V
Output voltage, low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 ≤ V_{IN} ≤ V_{DD}	−10		+10	μA
Output leakage current	I_{LO}	I_{LO}	0 ≤ V_{OUT} ≤ V_{DD}, OE = V_{IH}	−10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		V_{DD} − 0.6	V_{DD}	V_{DD} + 0.6	V
V_{DD} supply voltage	V_{DD}	V_{CC}		4.5	5.0	5.5	V
V_{PP} supply current	I_{PP}	I_{PP}	V_{PP} = V_{DD}			100	μA
V_{DD} supply current	I_{DD}	I_{CCA1}	CE = V_{IL}, V_{IN} = V_{IH}			50	mA

Note Symbol of corresponding μPD27C1001A

AC Programming Characteristics

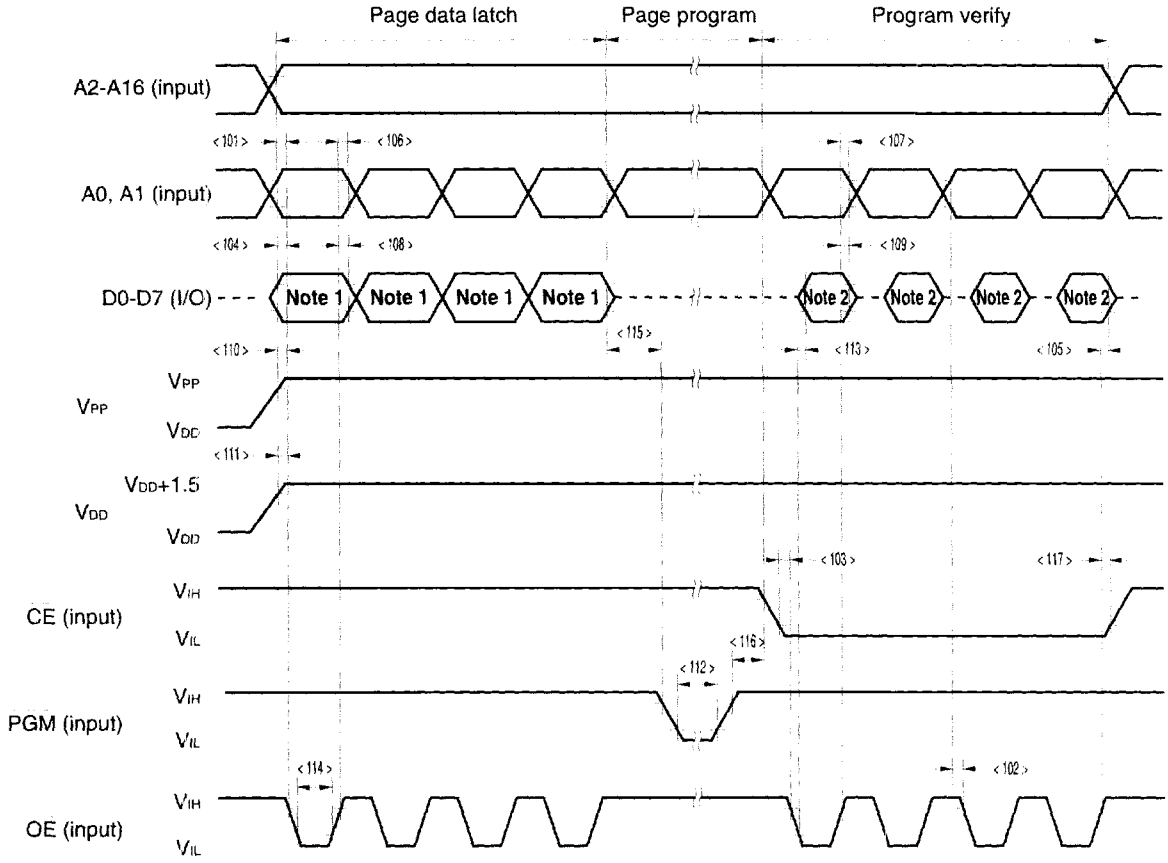
(1) PROM write mode timing (page program mode)

(T_A = 25 ± 5 °C, V_{DD} = 6.5 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V) (1/2)

Parameter	Symbol		Symbol[Note]	Condition	MIN.	TYP.	MAX.	Unit
Address setup time (vs. OE ↓)	<101>	t_{AS}	t_{AS}		2			μs
OE setup time	<102>	t_{OES}	t_{OES}		2			μs
CE setup time (vs. OE ↓)	<103>	t_{CES}	t_{CES}		2			μs
Input data setup time (vs. OE ↓)	<104>	t_{DS}	t_{DS}		2			μs
Address hold time (vs. OE ↑)	<105>	t_{AH}	t_{AH}		2			μs
	<106>	t_{AHL}	t_{AHL}		2			μs
	<107>	t_{AHV}	t_{AHV}		0			μs
Input data hold time (vs. OE ↑)	<108>	t_{DH}	t_{DH}		2			μs
OE ↑→ data output float delay time	<109>	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (vs. OE ↓)	<110>	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (vs. OE ↓)	<111>	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	<112>	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
OE ↓→ valid data delay time	<113>	t_{OE}	t_{OE}				1	μs
OE pulse width in data latch	<114>	t_{LW}	t_{LW}		1			μs
PGM setup time	<115>	t_{PGMS}	t_{PGMS}		2			μs
CE hold time	<116>	t_{CEH}	t_{CEH}		2			μs
OE hold time	<117>	t_{OEH}	t_{OEH}		2			μs

Note Symbol of corresponding μPD27C1001A

(1) PROM write mode timing (page program mode) (2/2)



Notes 1. D0-D7 (input)

2. D0-D7 (output)

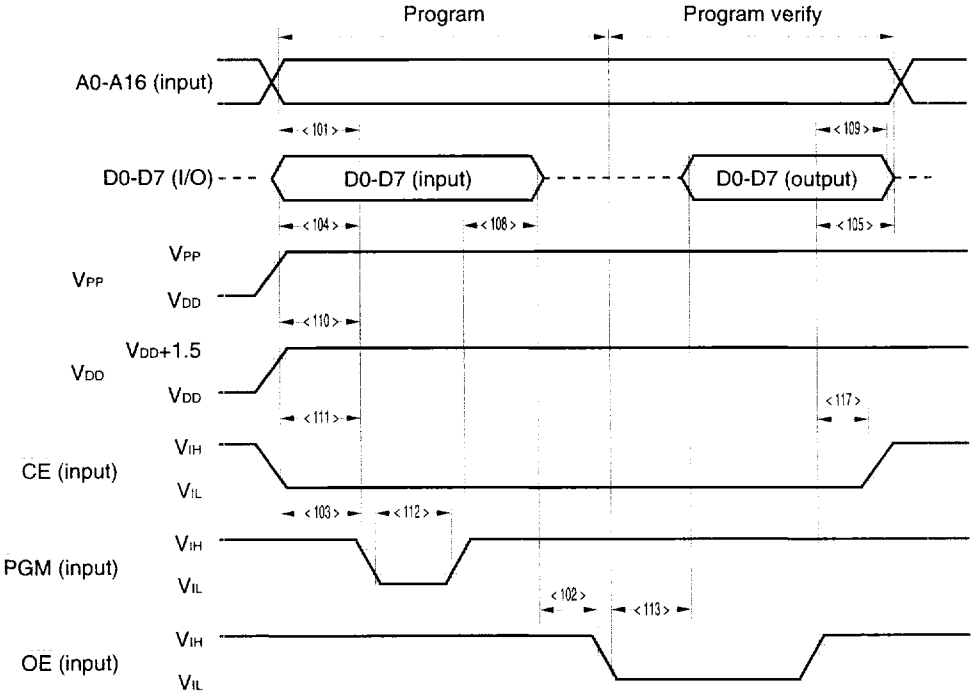
Remark The broken line indicates the high-impedance state.

(2) PROM write mode timing (byte program mode)

(T_A = 25 ± 5 °C, V_{DD} = 6.5 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V)

Parameter		Symbol	Symbol[Note]	Condition	MIN.	TYP.	MAX.	Unit
Address setup time (vs. PGM ↓)	<101>	t_{AS}	t_{AS}		2			μs
OE setup time	<102>	t_{OES}	t_{OES}		2			μs
CE setup time (vs. PGM ↓)	<103>	t_{CES}	t_{CES}		2			μs
Input data setup time (vs. PGM ↓)	<104>	t_{DS}	t_{DS}		2			μs
Address hold time (vs. OE ↑)	<105>	t_{AH}	t_{AH}		2			μs
Input data hold time (vs. PGM ↑)	<108>	t_{DH}	t_{DH}		2			μs
OE ↑→ data output float delay time	<109>	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (vs. PGM ↓)	<110>	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (vs. PGM ↓)	<111>	t_{VDS}	t_{VDS}		1.0			ms
Program pulse width	<112>	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
OE ↓→ valid data delay time	<113>	t_{OE}	t_{OE}				1	μs
OE hold time	<117>	t_{OEH}	—		2			μs

Note Symbol of the corresponding μPD27C1001A



Cautions 1. Apply V_{DD} before V_{PP}, and turn off V_{DD} after V_{PP}.

2. Keep V_{PP} to less than +13.5 V including overshoot.

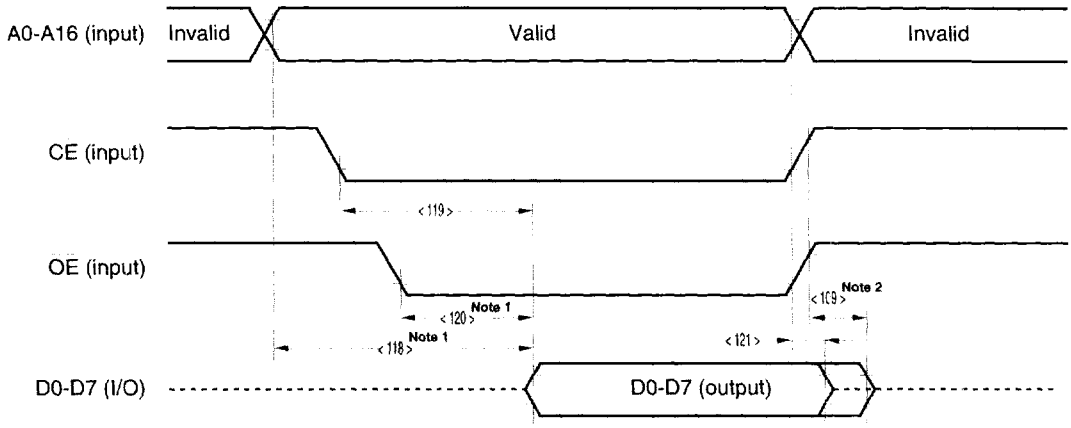
3. If the device is pulled out of the socket while +12.5 V is applied to V_{PP}, the reliability may be degraded.

Remark The broken line indicates the high-impedance state.

(3) PROM read mode timing (T_A = 25 ± 5 °C, V_{DD} = 5.0 ± 0.5 V, V_{PP} = V_{DD} ± 0.6 V)

Parameter	Symbol		Symbol[Note]	Condition	MIN.	TYP.	MAX.	Unit
Address → data output delay time	<118>	t_{ACC}	t_{ACC}	CE = OE = V_{IL}			1	μs
CE ↓→ data output delay time	<119>	t_{CE}	t_{CE}	OE = V_{IL}			1	μs
OE ↓→ data output delay time	<120>	t_{OE}	t_{OE}	CE = V_{IL}			1	μs
OE ↑→ data output float delay time	<109>	t_{DF}	t_{DF}	CE = V_{IL}	0		60	ns
Address → data hold time	<121>	t_{OH}	t_{OH}	CE = OE = V_{IL}	0			ns

Note Symbol of the corresponding μPD27C1001A



Notes 1. To read within the range of t_{ACC} (< 118 >), the delay time of OE input from the falling of CE must be t_{ACC}-t_{OE} (< 118 > - < 120 >) max.

2. t_{DF} (< 109 >) is the time after either OE or CE first reaches V_{IH}.

Remark The broken line indicates the high-impedance state.

(4) PROM programming mode setting timing (T_A = 25 °C, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PROM programming mode setup time	<122> t_{SMA}		10			μs