RF9801

DUAL-BAND EGSM900/DCS1800/GSM/ GPRS/LINEAR EDGE TRANSMIT MODULE

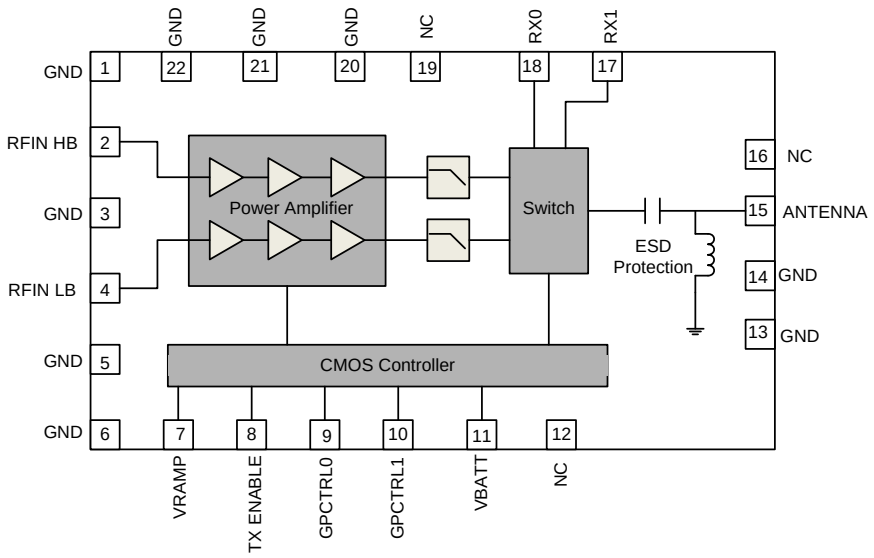
Package Style: Module 6.63mmx5.24mmx1.0mm

Features

- Dual Mode Operation
- Proven PowerStar® Architecture
- Integrated Power Flattening Circuit
- Integrated V_{RAMP} Filter
- Digital Bias Control
- Edge Low Current Mode
- No External Routing
- Symmetrical RX Ports
- High Gain Supports Low Drive Level
- Pin Compatibility with RF716X Family
- Robust 8kV ESD Protection at Antenna Port
- Integrated V_{BATT} Tracking Circuit

Applications

- EGSM900/DCS1800 Products
- 3V Dual-Band GSM/GPRS/ EDGE Handsets
- Mobile GPRS/EDGE Data Products
- Portable Battery-Powered Equipment
- GPRS Class 12 Compliant



Functional Block Diagram

Product Description

The RF9801 is a dual band (EGSM900/DCS1800) GSM/GPRS/Linear Edge, Class 12 compliant Transmit Module with two symmetrical receive ports. This transmit module builds upon RFMD's successful RF716X family incorporating full EDGE capability while maintaining a common footprint for ease of phone platform design. The RF9801 continues to build upon RFMD's leading patented PowerStar® Architecture to include such features as Power Flattening Circuit, V_{RAMP} Filtering, V_{BATT} Tracking, and EDGE Low Power Mode. The module includes a multi-function CMOS controller, GaAs HBT power amplifier, and pHEMT front end antenna switch. The amplifier devices are manufactured on RFMD's Advance Gallium Arsenide Heterojunction Bipolar Transistor (GaAs HBT) Process, which is designed to operate either in saturated mode for GMSK or linear mode for EDGE 8PSK signaling. The highly integrated transmit module simplifies the phone design by eliminating the need for complicated control loop design, output RF spectrum, (ORFS) optimization, harmonic filtering, and component matching, all of which combine to provide best in class RF performance, solution size, and ease of implementation for cellular phone systems. The RF ports are 50Ω matched and the antenna port includes ESD protection circuitry which meets the stringent 8kV industry standards requiring no additional components. All of these eliminated factors help to improve the customer's product time to market.

Optimum Technology Matching® Applied

☑ GaAs HBT	☐ SiGe BiCMOS	☑ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☑ Si CMOS	☐ RF MEMS
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.3 to +6.0	V
Power Control Voltage (V_{RAMP})	-0.3 to +1.8	V
Input RF Power	+10	dBm
Max Duty Cycle	50	%
Output Load VSWR	20:1	
Operating Case Temperature	-20 to +85	°C
Storage Temperature	-55 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
ESD					
ESD RF Ports			1000	V	HBM, JESD22-A114
			1000	V	CDM, JEDEC JESD22-C101
ESD Antenna Port			8	KV	IEC 61000-4-2
ESD Any Other Port			1000	V	HBM, JESD22-A114
			1000	V	CDM, JEDEC JESD22-C101
Overall Power Control V_{RAMP}					
Power Control "ON"			1.8	V	Max. P_{OUT}
Power Control "OFF"		0.25		V	Min. P_{OUT}
V_{RAMP} Input Capacitance		15	20	pF	DC to 200kHz
V_{RAMP} Input Current			10	µA	$V_{RAMP}=V_{RAMP\ MAX}$
Power Control Range		50		dB	$V_{RAMP}=0.25V$ to $V_{RAMP\ MAX}$
Overall Power Supply					
Power Supply Voltage	3.2	3.6	4.2	V	Operating Limits
Power Supply Current		1	20	µA	$P_{IN}<-30dBm$, TX Enable=Low, $V_{RAMP}=0.25V$, Temp=-20°C to +85°C, $V_{BATT}=4.2V$
Overall Control Signals					
GpCtrl0, GpCtrl1 "Low"	0	0	0.5	V	
GpCtrl0, GpCtrl1 "High"	1.25	2.0	3.0	V	
GpCtrl0, GpCtrl1 "High Current"		1	2	uA	
TX Enable "Low"	0	0	0.5	V	
TX Enable "High"	1.25	2.0	3.0	V	
TX Enable "High Current"		1	2	uA	
RF Port Input and Output Impedance		50		Ω	

Table 1: Module Control + Antenna Switch Logic

TX_EN	GpCtrl1	GpCtrl0	Control Mode
0	0	0	Standby
0	1	0	RX 0
0	1	1	RX 1
1	1	0	TX EGSM900 GMSK
1	1	1	TX DCS1800 GMSK
1	0	0	TX EGSM900 8PSK
1	0	1	TX DCS1800 8PSK

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
EGSM900 Band GMSK Mode					Nominal Conditions used unless otherwise stated. V_{BATT}=3.6V, P_{IN}=1dBm, Temp=+25°C, Duty Cycle=25%. All unused ports=50Ω. Refer to logic table for mode of operation.
Operating Frequency Range	880		915	MHz	
Input Power	-2	+1	+4	dBm	Full P_{OUT} guaranteed at minimum drive level.
Input VSWR		2:1	3:1		Over P_{OUT} range (5dBm to 33dBm)
Maximum Output Power	33.0	33.7		dBm	Duty Cycle=25%, Pulse Width=1154µs
	31			dBm	V_{BATT}=3.2V to 4.2V, P_{IN}=-2dBm to +4dBm, Temp=-20°C to +85°C, Duty Cycle=50%, Pulse Width=2308µs, V_{RAMP}≤1.8V
Minimum Power Into 3:1 VSWR	30.0			dBm	Minimum power delivered to the load over 360° phase sweep.
Power Added Efficiency	36	41		%	Set V_{RAMP}=V_{RAMP} rated for P_{OUT}=33dBm
2nd Harmonic		-40*	-33	dBm	V_{RAMP}=V_{RAMP} rated for P_{OUT}=33dBm. *Typical value measured from worst case harmonic frequency across the band.
3rd Harmonic		-40*	-33	dBm	V_{RAMP}=V_{RAMP} rated for P_{OUT}=33dBm. *Typical value measured from worst case harmonic frequency across the band.
All other harmonics up to 12.75GHz			-33	dBm	V_{RAMP}=V_{RAMP} rated for P_{OUT}=33dBm
Non-Harmonic Spurious up to 12.75GHz			-36	dBm	V_{RAMP}=V_{RAMP} rated for P_{OUT}=33dBm, also over all power levels (5dBm to 33dBm)
Forward Isolation 1		-54	-41	dBm	TX Enable=Low, P_{IN}=4dBm, V_{RAMP}=0.25V
Forward Isolation 2		-28	-15	dBm	TX Enable=High, P_{IN}=4dBm, V_{RAMP}=0.25V
Output Noise Power					
925MHz to 935MHz		-87	-77	dBm	P_{OUT}=33dBm, RBW=100kHz
935MHz to 960MHz		-89	-83	dBm	
1805MHz to 1880MHz		-115	-87	dBm	
Output Load VSWR Stability (Spurious Emissions)			-36	dBm	VSWR=12:1; all phase angles P_{OUT}≤33dBm into 50Ω load; load switched to VSWR=12:1
Output Load VSWR Ruggedness	No damage or permanent degradation to device				VSWR=20:1; all phase angles P_{OUT}=33dBm into 50Ω load; load switched to VSWR=20:1

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
EGSM900 Band 8PSK Mode					Nominal Conditions used unless otherwise stated. V_{BATT}=3.6V, Temp=+25°C, Duty Cycle=25%, Pin adjusted for required P_{OUT}. All unused ports =50Ω. Refer to logic table for mode of operation.
Operating Frequency Range	880		915	MHz	
Max Linear Output Power	27.5			dBm	Meets ACPR and EVM. Nominal Conditions.
	26.0			dBm	Meets ACPR and EVM. Extreme Conditions: V_{BATT}=3.2V to 4.2V, Temp=-20°C to +85°C.
	15.0			dBm	Meets ACPR and EVM. Extreme Conditions; Low Power Mode.V_{RAMP}=0V
Gain: High Power Mode	30.5	33.5	35.5	dB	P_{OUT}=27.5dBm, V_{RAMP}=1.8V
Gain: Low Power Mode		31.5		dB	P_{OUT}=5dBm, V_{RAMP}=0V
Current: High Power Mode		900	1300	mA	P_{OUT}=27.5dBm, V_{RAMP}=1.8V
Current: Low Power Mode		300		mA	P_{OUT}=5dBm, V_{RAMP}=0V
Efficiency: High Power Mode	12	18		%	P_{OUT}=27.5dBm, V_{RAMP}=1.8V
ACPR (400kHz): High Power Mode BW=30kHz		-60	-57	dBc	P_{OUT}=5dBm to 27.5dBm, V_{RAMP}=1.8V
		-60	-56	dBc	P_{OUT}=5dBm to 26.0dBm, V_{RAMP}=1.8V V_{BATT}=3.2V to 4.2V Temp=-20°C to +85°C
EVM (RMS): High Power Mode		1	4	%	P_{OUT}=5dBm to 27.5dBm, V_{RAMP}=1.8V
			5	%	P_{OUT}: 5dBm to 26.0dBm, V_{RAMP}=1.8V V_{BATT}=3.2V to 4.2V Temp=-20°C to +85°C
Output Noise Power					
925MHz to 935MHz		-86	-77	dBm	P_{OUT}=27.5dBm, RBW=100kHz
935MHz to 960MHz		-86	-83	dBm	
1805MHz to 1880MHz		-115	-87	dBm	
Output Load VSWR Stability (Spurious Emissions)			-36	dBm	VSWR=12:1; all phase angles P_{OUT}≤27.5dBm into 50Ω load; Load switched to VSWR=12:1

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
DCS1800 Band GMSK Mode					Nominal Conditions used unless otherwise stated. V_{BATT}=3.6V, P_{IN}=1dBm, Temp=+25°C, Duty Cycle=25%, Pin adjusted for required P_{OUT}. All unused ports=50Ω. Refer to logic table for mode of operation.
Operating Frequency Range	1710		1785	MHz	
Input Power	-2	+1	+4	dBm	Full P_{OUT} guaranteed at minimum drive level.
Input VSWR		2:1	2.5:1		Over P_{OUT} range (0dBm to 30dBm)
Maximum Output Power	30.0	31.0		dBm	Duty Cycle=25%, Pulse Width=1154µs
	28			dBm	V_{BATT}=3.2V to 4.2V, P_{IN}=-2dBm to +4dBm, Temp=-20°C to +85°C, Duty Cycle=50%, Pulse Width=2308µs, V_{RAMP}≤1.8V
Minimum Power Into 3:1 VSWR	27.0			dBm	The measured delivered output power to the load with the mismatch loss already taken into account with 1dB variation margin.
Power Added Efficiency	32	36		%	Set V_{RAMP}=V_{RAMP} rated for P_{OUT}=30dBm
2nd Harmonic		-40*	-33	dBm	V_{RAMP}=V_{RAMP} rated for P_{OUT}=30dBm. *Typical value measured from worst case harmonic frequency across the band.
3rd Harmonic		-40*	-33	dBm	V_{RAMP}=V_{RAMP} rated for P_{OUT}=30dBm. *Typical value measured from worst case harmonic frequency across the band.
All other harmonics up to 12.75GHz			-33	dBm	V_{RAMP}=V_{RAMP} rated for P_{OUT}=30dBm
Non-Harmonic Spurious up to 12.75GHz			-36	dBm	V_{RAMP}=V_{RAMP} rated for P_{OUT}=30dBm, also over all power levels (0dBm to 30dBm)
Forward Isolation 1		-70	-53	dBm	TX Enable=Low, P_{IN}=4dBm, V_{RAMP}=0.25V
Forward Isolation 2		-30	-15	dBm	TX Enable=High, P_{IN}=4dBm, V_{RAMP}=0.25V
Output Noise Power					
925MHz to 935MHz		-98	-77	dBm	P_{OUT}=30dBm, RBW=100kHz
935MHz to 960MHz		-98	-83	dBm	
1805MHz to 1880MHz		-92	-79	dBm	
Output Load VSWR Stability (Spurious Emissions)			-36	dBm	VSWR=12:1; all phase angles P_{OUT}≤30dBm into 50Ω load; Load switched to VSWR=12:1
Output Load VSWR Ruggedness	No damage or permanent degradation to device				VSWR=12:1; all phase angles P_{OUT}≤30dBm into 50Ω load; Load switched to VSWR=12:1

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
DCS1800 Band 8PSK Mode					Nominal Conditions used unless otherwise stated. V_{BATT}=3.6V, Temp=+25°C, Duty Cycle=25%, Pin adjusted for required P_{OUT}. All unused ports =50Ω. Refer to logic table for mode of operation.
Operating Frequency Range	1710		1785	MHz	
Max Linear Output Power	26.5			dBm	Meets ACPR and EVM. Nominal Conditions.
	25.0			dBm	Meets ACPR and EVM. Extreme Conditions: V_{BATT}=3.2V to 4.2V, Temp=-20°C to +85°C.
	13.0			dBm	Meets ACPR and EVM. Extreme Conditions; Low Power Mode.V_{RAMP}=0V
Gain: High Power Mode	31.5	34.5	36.5	dB	P_{OUT}=26.5dBm, V_{RAMP}=1.8V
Gain: Low Power Mode		32.0		dB	P_{OUT}=0dBm, V_{RAMP}=0V
Current: High Power Mode		975	1300	mA	P_{OUT}=26.5dBm, V_{RAMP}=1.8V
Current: Low Power Mode		250		mA	P_{OUT}=0dBm, V_{RAMP}=0V
Efficiency: High Power Mode	9.5	13		%	P_{OUT}=26.5dBm, V_{RAMP}=1.8V
ACPR (400kHz): High Power Mode BW=30kHz		-66	-57	dBc	P_{OUT}=0dBm to 26.5dBm, V_{RAMP}=1.8V
		-66	-56	dBc	P_{OUT}=0dBm to 25.0dBm, V_{RAMP}=1.8V V_{BATT}=3.2V to 4.2V Temp=-20°C to +85°C
EVM (RMS): High Power Mode		1	4	%	P_{OUT}=0dBm to 26.5dBm, V_{RAMP}=1.8V
			5	%	P_{OUT}: 0dBm to 25.0dBm, V_{RAMP}=1.8V V_{BATT}=3.2V to 4.2V Temp=-20°C to +85°C
Output Noise Power					
925MHz to 935MHz		-95	-77	dBm	P_{OUT}=26.5dBm, RBW=100kHz
935MHz to 960MHz		-95	-80	dBm	
1805MHz to 1880MHz		-90	-80	dBm	
Output Load VSWR Stability (Spurious Emissions)			-36	dBm	VSWR=12:1; all phase angles P_{OUT}≤26.5dBm into 50Ω load; Load switched to VSWR=12:1

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
RX Section					Nominal Conditions used unless otherwise stated. V_{BATT}=3.6V, P_{IN}=1dBm, Temp=+25°C, Duty Cycle=25%. All unused ports=50Ω. Refer to logic table for mode of operation.
Insertion Loss GSM900 ANT-RX0/ RX1		1.1	1.3	dB	Freq=925MHz to 960MHz. See Note 1.
In-Band Ripple GSM900 ANT-RX0/RX1		0.2		dB	Freq=925MHz to 960MHz
Input VSWR GSM900 ANT-RX0/RX1		1.5:1			Freq=925MHz to 960MHz
Insertion Loss DCS1800 ANT-RX0/RX1		1.3	1.6	dB	Freq=1805MHz to 1880MHz. See Note 1.
In-Band Ripple DCS1800 ANT-RX0/RX1		0.2		dB	Freq=1805MHz to 1880MHz
Input VSWR DCS1800 ANT-RX0/RX1		1.5:1			Freq=1805MHz to 1880MHz
TX Section					
Switch Leakage P_{OUT} at RX Port GSM900 ANT-RX0/RX1		0.5	8.0	dBm	GSM900 TX mode: Freq=880MHz to 915MHz, V_{RAMP}=V_{RAMP} rated for P_{OUT}=33dBm at antenna port. See Note 2.
Switch Leakage P_{OUT} at RX Port DCS1800 ANT-RX0/RX1		3.0	6.0	dBm	DCS1800 TX mode: Freq=1710MHz to 1785MHz, V_{RAMP}=V_{RAMP} rated for P_{OUT}=30dBm at antenna port. See Note 2.

Note 1: The insertion loss values listed are the values guaranteed at the DUT port reference plane (i.e. excludes external mismatch and resistive trace losses).
Note 2: Isolation specification set to ensure at least the following isolation at rated power:
Calculation Example using typical values: P_{OUT} at Antenna-P_{OUT} at RX Port. Isolation LB=33-8=25dB, HB=30-6=24dB.

Pin	Function	Description
1	GND	Pin connected to module Ground.
2	RFIN HB	RF input to the DCS1800 band. This is a 50Ω input.
3	GND	Pin connected to module Ground.
4	RFIN LB	RF input to the GSM900 band. This is a 50Ω input.
5	GND	Pin connected to module Ground.
6	GND	Pin connected to module Ground.
7	VRAMP	V_{RAMP} ramping signal from DAC. A simple RC filter is integrated into the RF9801 module. V_{RAMP} may or may not require additional filtering depending on the baseband selected.
8	TX ENABLE	This signal enables the PA module for operation with a logic high. The switch is put in TX mode determined by GpCtrl0 and GpCtrl1.
9	GPCTRL0	Control pin that together with GpCtrl1 selects mode of operation.
10	GPCTRL1	Control pin that together with GpCtrl0 selects mode of operation.
11	VBATT	Power supply for the module. This should be connected to the battery terminal using as wide a trace as possible.
12	NC	No connection.
13	GND	Pin connected to module Ground.
14	GND	Pin connected to module Ground.
15	ANTENNA	Antenna port.
16	NC	No connection.
17	RX1	RX1 port of antenna switch. This is a 50Ω output. RX1 is interchangeable with RX0.
18	RX0	RX0 port of antenna switch. This is a 50Ω output. RX0 is interchangeable with RX1.
19	NC	No connection.
20	GND	Pin connected to module Ground.
21	GND	Pin connected to module Ground.
22	GND	Pin connected to module Ground.
23	GND	Pin connected to module Ground.

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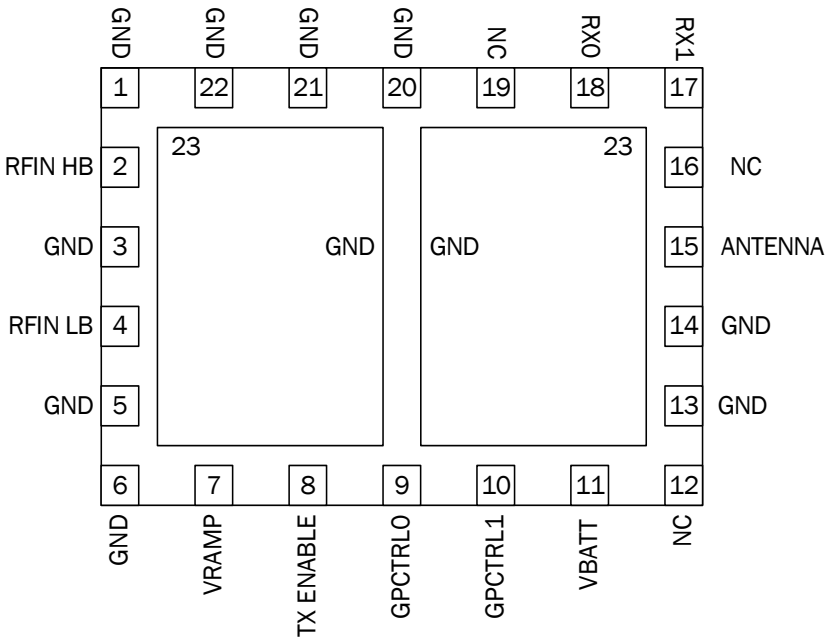
Pin Out

(Top View)



Theory of Operation

Overview

The RF9801 is designed for use as the final portion of the transmit section in mobile phones covering the EGSM900 and DCS1800 frequency bands. The RF9801 is a high power, dual mode GSM/EDGE, power amplifier module containing RFMD's patented PowerStar® Architecture. The module includes a multi-function CMOS controller, GaAs HBT power amplifier, and pHEMT front end antenna switch. The integrated power control loop can be driven directly from the baseband DAC to provide a very predictable power output which enables handset manufacturers to achieve simple and efficient phone calibration in production.

Additional Features

Power Flattening Circuit

When a mismatch is presented to the antenna of the phone, the output impedance presented to the PA also varies resulting in variation of output power and current. This can compromise the PA's ability to maintain the minimum output power required for calls, and limit the total radiated power (TRP), to meet the requirements of governmental agencies and cellular service providers. The PFC sets a reference voltage into 50Ω and the Internal feedback loop corrects for impedance variation by reducing the power and current variation into mismatch conditions.

V_{RAMP} Filtering:

The V_{RAMP} control voltage is received from the Baseband DAC. The DAC signal is usually in the form of a staircase waveform related to the DAC bit resolution and the timing of the power steps. The staircase waveform usually requires some filtering to smooth out the waveform and reduce any unwanted spectral components showing up in the switching spectra of the RF output signal. A simple RC filter maybe integrated into the Baseband, Transmit module or with discrete components between the two.

V_{BATT} Tracking/V_{RAMP} Limiter

This circuit monitors the relationship of the battery voltage and V_{RAMP}/V_{CC} used to control the PA. At low V_{BATT} levels the FET pass-device which controls V_{CC} can enter into a saturation region which can increase switching transients. The saturation detection circuit automatically monitors the battery voltage and produces a correction so that V_{CC} is reduced, thus preventing the power control loop from reaching saturation and inducing switching transients.

EDGE Low Power Option

In EDGE mode the PA operates in the linear region and the P_{OUT} is controlled by the P_{IN}. Since the phone tends to operate most of its time in the lower to mid power ranges the bias can be adjusted to optimize efficiency. The RF9801 quiescent current can be changed in the power amplifier when operating at lower output power levels by adjusting V_{RAMP}.

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Modes of Operation: Saturated GMSK and Linear EDGE

The design of a dual mode power amplifier module is a challenging process involving many circuit compromises and performance tradeoffs to allow best performance in both the saturated and linear operating regions. This is most demanding in achieving best performance between GSM efficiency and EDGE linearity requirements.

In GSM mode, the GMSK modulation is a constant envelope and the useful data is entirely included in the phase of the signal. Since the constant envelope is not sensitive to amplitude non-linearities caused by the PA, the amplifier can operate in saturation mode (deep class AB or class C) for optimum efficiency.

In EDGE mode, the 8PSK signal has information encoded in both amplitude and phase, which requires a linear power amplifier (Class A) to transfer the 8PSK modulation with minimal distortion.

In a dual mode module, tuning of the load line must be balanced between GSM efficiency and EDGE linearity. The result is slightly lower GSM efficiency than a single mode (saturated only) power amplifier module. Figure 1 shows the Power Amplifier operating regions in GSM and EDGE mode.

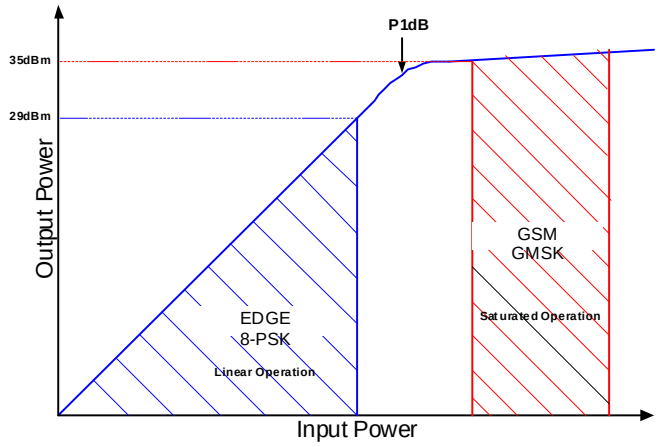

Figure 1. Power Amplifier Operating Regions in GSM/EDGE Mode

GSM (saturated) MODE:
In GSM mode, RF9801 operates as a traditional PowerStar® module. The basic circuit diagram is shown in the Figure 2.

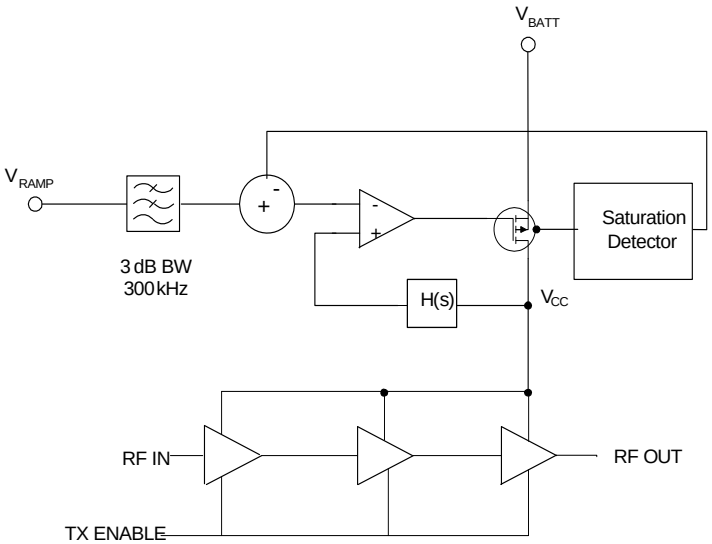

Figure 2. Basic PowerStar® Circuit Diagram

The control circuit receives a DAC voltage (V_{RAMP}) to set the required output power for the phone. The PowerStar® I architectures multiples the V_{RAMP} voltage level and regulates it at the collector (V_{CC}) of all three stages of the amplifier, holding the stages in saturation. The base bias is fixed at a point that is at least deep class AB or class C. By holding the PA in saturation, performance sensitivity is essentially eliminated to temperature, frequency, voltage and input drive level ensuring robust performance within the ETSI power vs time mask.

The regulation of power is demonstrated in Equation 1. The equation shows that load impedance affects output power, but to a lesser degree than the V_{CC} supply variations. Since the architecture regulates V_{CC}, the dominant cause of power variation is eliminated. The control loop provides a very linear relationship between V_{RAMP} and P_{OUT}.

$$P_{OUT} = 10\log\frac{(2 \cdot V_{CC} - V_{SAT})}{8 \cdot R1 \cdot 10^{-3}}$$

Equation 1. Output Power versus Voltage Relationship

The RF signal applied at the RFIN pin must be a constant amplitude signal and should be high enough to saturate the amplifier in the GSM mode. The input power (P_{IN}) range is indicated in the specifications. Power levels below this range will result in reduced maximum output power and the potential for more variation of output power over extreme conditions. Higher input power is unnecessary and will require more current in the circuitry driving the power amplifier further into saturation which could also result in lower output power.

EDGE (Linear) MODE
In EDGE mode, Vramp is fixed and the output power is directly controlled by input power.

The RF signal applied to the RFIN pin must be accurately controlled to produce the desired output amplitude and burst ramping. The RFIN power must be maintained so that the amplifier is operating in its linear region. If the input drive is too high, the amplifier will begin to saturate causing the ACPR and EVM performance to degrade. The most sensitive of these is typically the +/-400kHz offset ACPR. As the amplifier approaches saturation, this will be the first parameter to show significant degradation.

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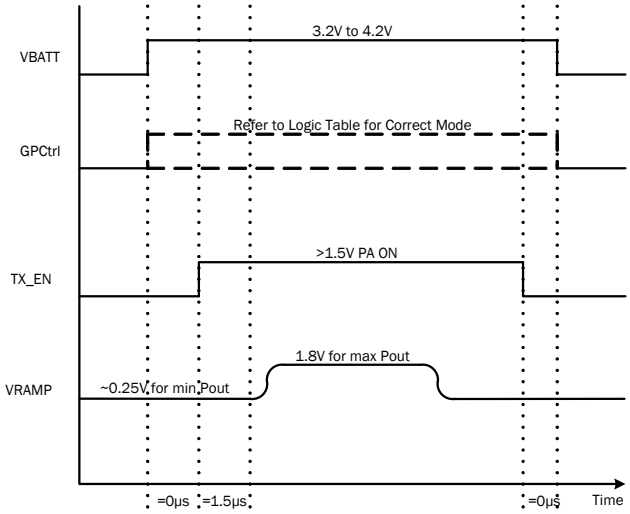
Since the PAM operates as a gain block in EDGE mode, gain variation over extreme conditions must be considered when determining the output power that a specific input power will produce. Special attention must be given to ensure that the output power of the PA does not go higher than the maximum linear output that the PA can provide with acceptable EVM and ACPR performance.

A large portion of the total current in a linear amplifier is necessary to bias the transistors so that the output remains in the linear region. In an EDGE system where there is a range of power control levels, an amplifier biased to operate at a high power will be very inefficient at low power levels. Conversely, an amplifier biased to operate at a low power will not be linear at high power levels. Refer to the low power mode feature.

Power On (Timing) Sequence

In the Power-On Sequence, there are some important set-up times associated with the control signals of the TxM. Refer to the logic table for control signal functions. One of the critical relationships is the settling time between TXEN going high and when V_{RAMP} can begin to increase. This time is often referred to as the "pedestal" and is required so that the internal power control loop and bias circuitry can settle after being turned on. The PowerStar® architecture usually requires approximately 1µs to 2µs for proper settling of the power control loop.

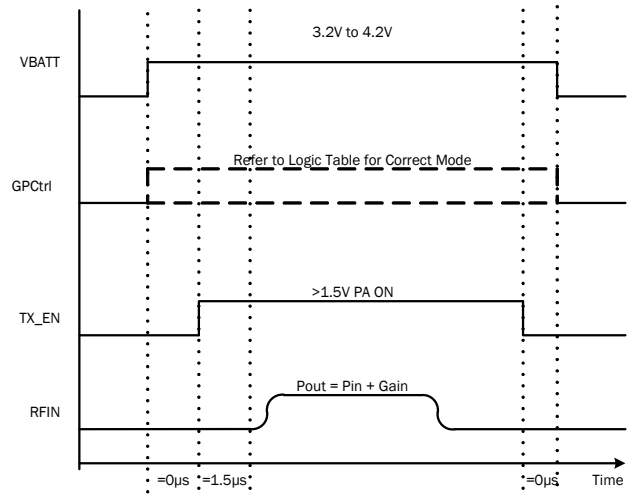


GMSK Power On Sequence:

1. Apply VBATT
2. Apply CPCtrl
3. Apply minimum VRAMP (~0.25V)
4. Apply TX_EN
5. Apply VRAMP for desired output power. (Refer to power ramping section)

RFIN can be applied at any time. For good transient response it must be applied before power ramp begins.

The Power Down Sequence is the reverse order of the Power On Sequence.



8PSK Power On Sequence:

1. Apply VBATT
2. Apply CPCtrl
3. Apply TX_EN
4. Ramp RFIN amplitude for desired output power

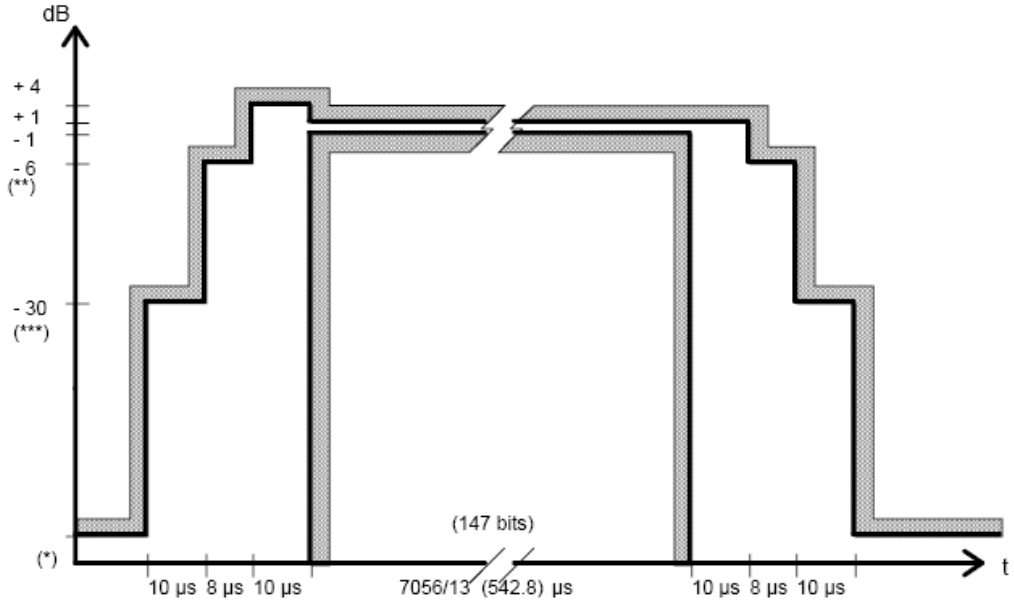
VRAMP is a constant DC input and can be applied anytime after Vbatt.

The Power Down Sequence is the reverse order of the Power On Sequence.

Power Ramping

The V_{RAMP} waveform must be created such that the output power falls into the ETSI power versus time mask. The ability to ramp the RF output power to meet ETSI switching transient and time mask requirements partially depends upon the predictability of output power versus V_{RAMP} response of the power amplifier. The PowerStar® control loop is very capable of meeting switching transient requirements with the proper raised cosine waveform applied to the V_{RAMP} input. Ramps usually fall within the 12µs to 14µs time to control switching transients at high power levels. Faster ramps usually have a steeper transition creating higher transients. Slower ramps may have difficulty meeting the time mask. Optimization needs to include all power levels as the time mask requirements change with P_{OUT} levels.

The diagram below is the ETSI time mask for a single GSM timeslot.



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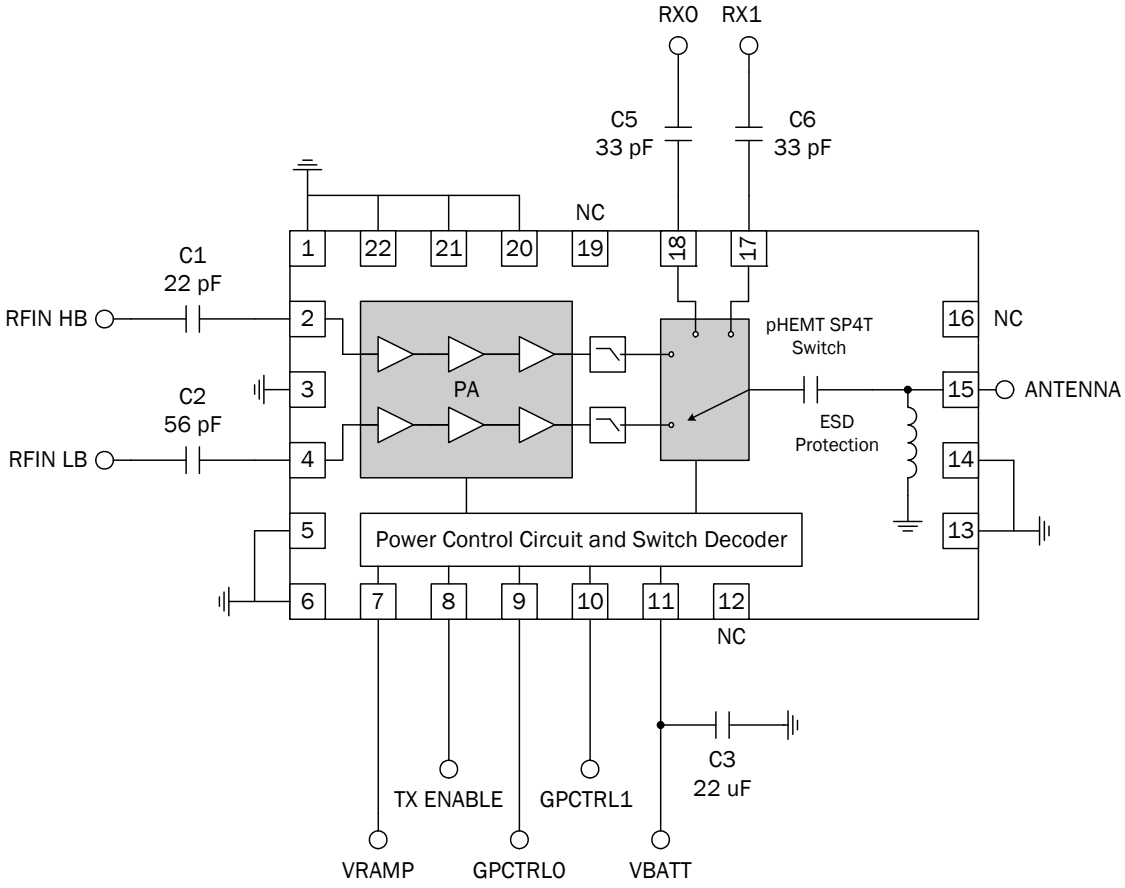
Application Schematic



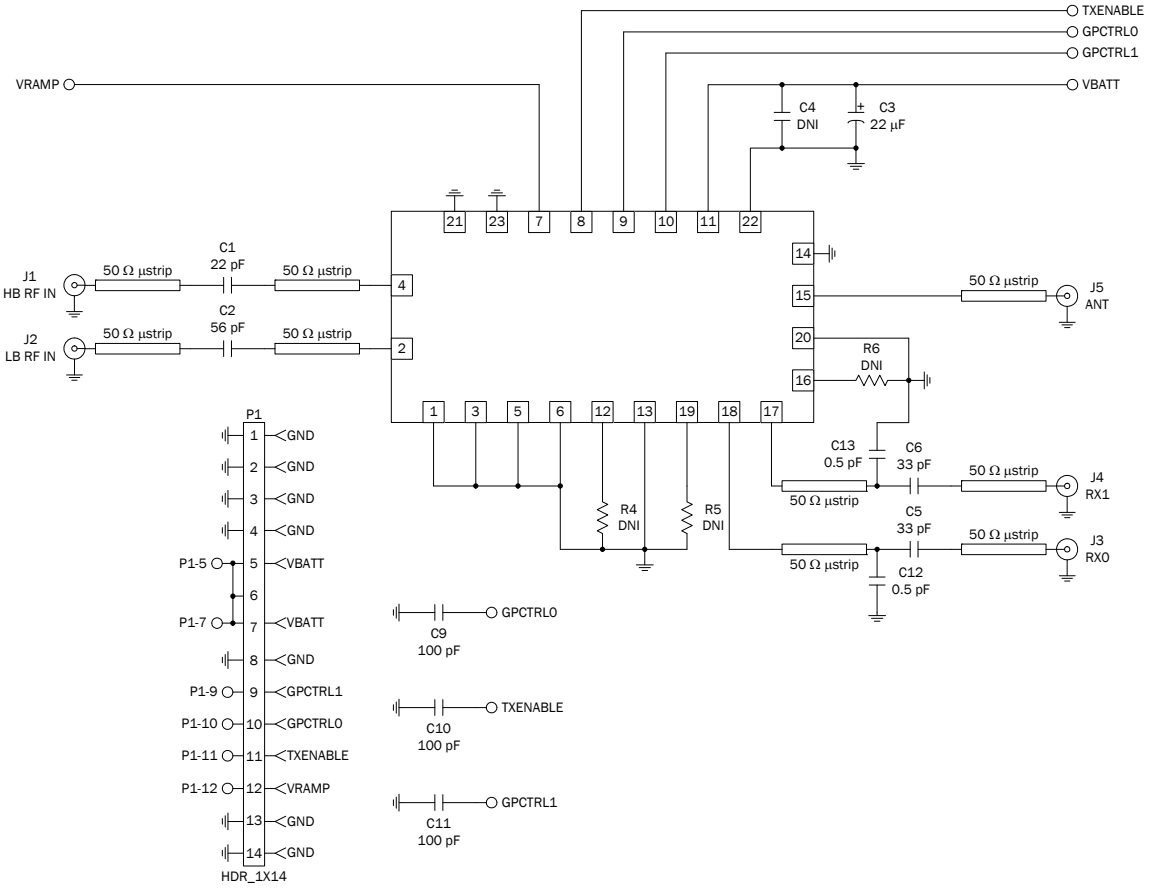
Notes:

V_{BATT} capacitor value may change depending on application.

RXO and RX1 usually connect to SAW filters; C4 and C5 may not be needed as some SAW filters contain their own DC blocking capability.

If placing an attenuation network on the input to the power amplifier, ensure that it is positioned on the transceiver side of capacitor C1 (or C2) to prevent adversely affecting the base biasing of the power amplifier.

Evaluation Board Schematic



Notes:

C4 is an optional bypass capacitor that is not used on the EVB. C9, C10, and C11 are optional decoupling capacitors which may not be needed in application.

RX0 and RX1 usually connect to SAW filters. C5 and C6 may not be needed.

R4, R5, and R6 are not placed.

C12 and C13 are optimization caps to show best case insertion loss.

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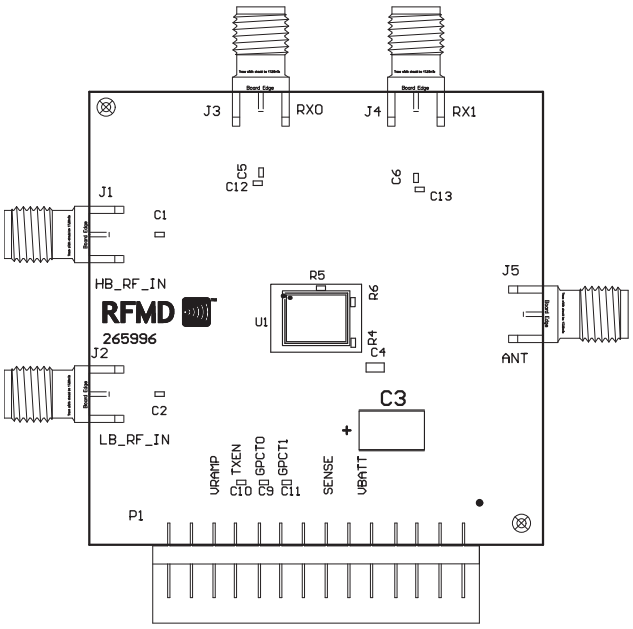
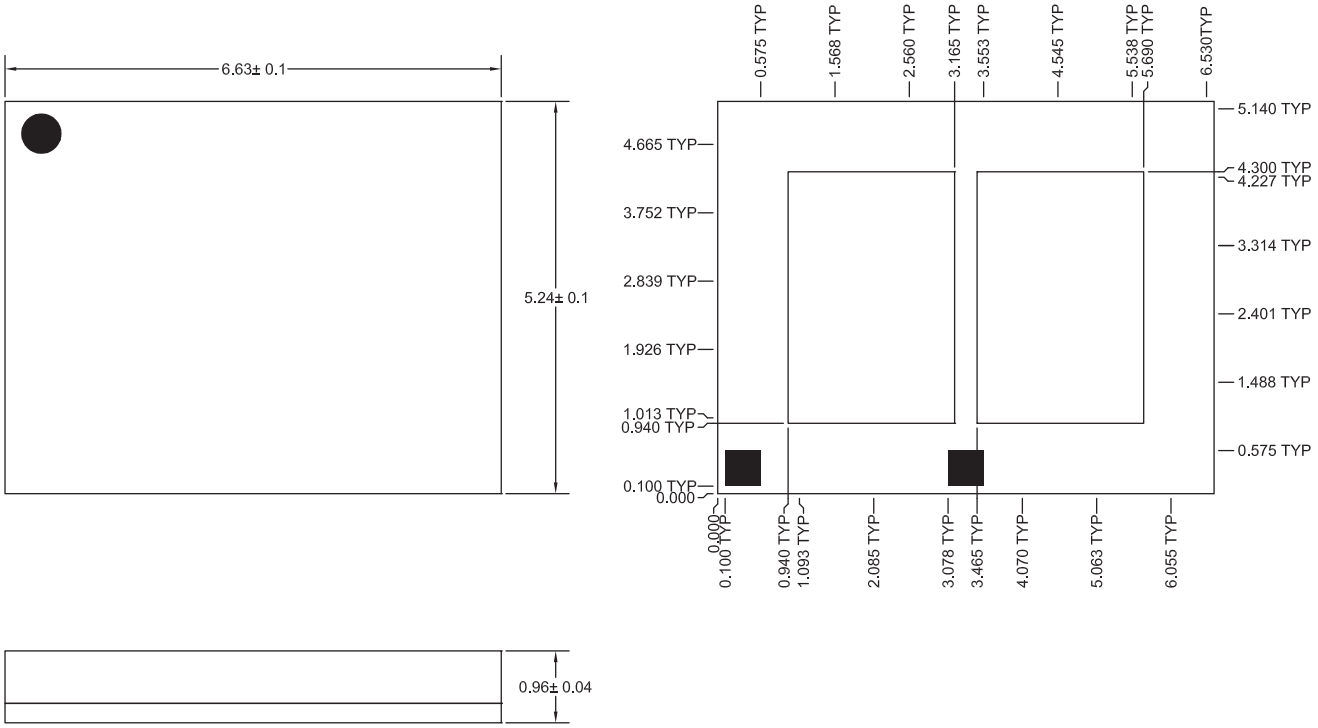
Evaluation Board Layout
Board Size 2.0” x 2.0”



Notes: All inputs, outputs, and antenna traces are 50Ω micro strip.

Package Drawing



Notes:
Shaded areas represent Pin 1 location

Notes:

YY indicates year, WW indicates work week, and Trace Code is a sequential number assigned at device assembly.

Shaded areas represent Pin 1 location.

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PCB Design Requirements

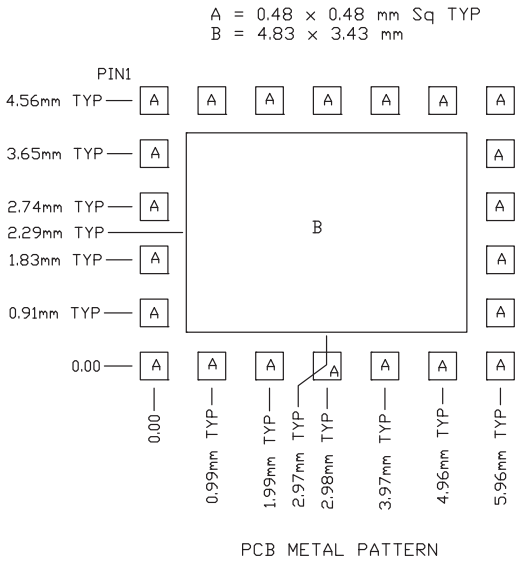
PCB Surface Finish

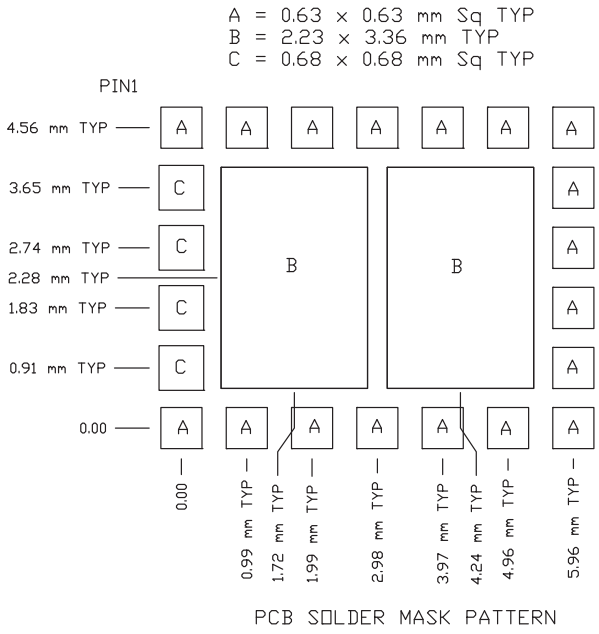
The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

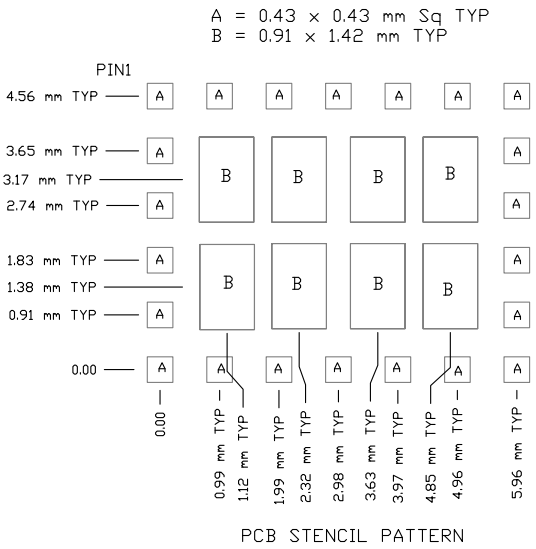
PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land and Solder Mask Pattern







Tape and Reel

Carrier tape basic dimensions are based on EIA 481. The pocket is designed to hold the part for shipping and loading onto SMT manufacturing equipment, while protecting the body and the solder terminals from damaging stresses. The individual pocket design can vary from vendor to vendor, but width and pitch will be consistent.

Carrier tape is wound or placed onto a shipping reel either 330mm (13 inches) in diameter or 178mm (7 inches) in diameter. The center hub design is large enough to ensure the radius formed by the carrier tape around it does not put unnecessary stress on the parts.

Prior to shipping, moisture sensitive parts (MSL level 2a-5a) are baked and placed into the pockets of the carrier tape. A cover tape is sealed over the top of the entire length of the carrier tape. The reel is sealed in a moisture barrier ESD bag with the appropriate units of desiccant and a humidity indicator card, which is placed in a cardboard shipping box. It is important to note that unused moisture sensitive parts need to be resealed in the moisture barrier bag. If the reels exceed the exposure limit and need to be rebaked, most carrier tape and shipping reels are not rated as bakeable at 125°C. If baking is required, devices may be baked according to section 4, table 4-1, of Joint Industry Standard IPC/JEDEC J-STD-033.

The table below provides information for carrier tape and reels used for shipping the devices described in this document.

Tape and Reel

RFMD Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units per Reel
RF9801TR13	13 (330)	4 (102)	12	8	Single	2500
RF9801TR7	7 (178)	2.4 (61)	12	8	Single	750

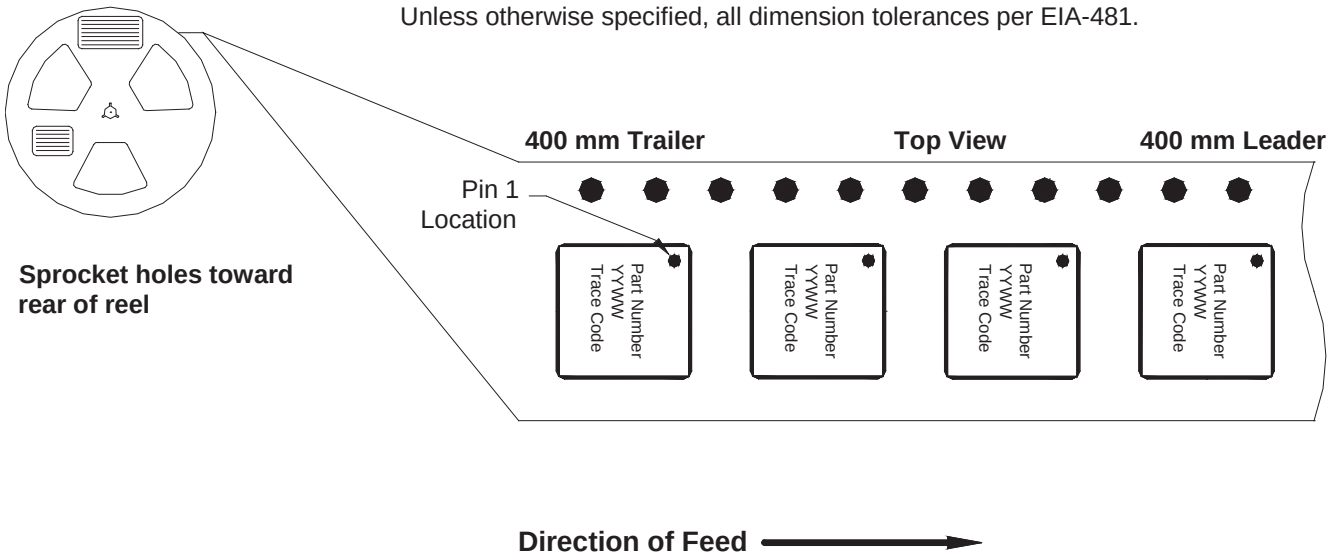


Figure 1. 5.24mmx6.63mm (Carrier Tape Drawing with Part Orientation)

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RoHS* Banned Material Content

RoHS Compliant:	Yes
Package total weight in grams (g):	0.121
Compliance Date Code:	-
Bill of Materials Revision:	-
Pb Free Category:	e4

Bill of Materials	Parts Per Million (PPM)					
	Pb	Cd	Hg	Cr VI	PBB	PBDE
Die	0	0	0	0	0	0
Molding Compound	0	0	0	0	0	0
Lead Frame	0	0	0	0	0	0
Die Attach Epoxy	0	0	0	0	0	0
Wire	0	0	0	0	0	0
Solder Plating	0	0	0	0	0	0

This RoHS banned material content declaration was prepared solely on information, including analytical data, provided to RFMD by its suppliers, and applies to the Bill of Materials (BOM) revision noted above.

* DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment

Ordering Information

RF9801	Dual-Band EGSM900/DCS1800/GSM/ GPRS/Linear Edge Transmit Module
RF9801SB	Transmit Module 5-Piece Sample Pack
RF9801PCBA-41X	Fully Assembled Evaluation Board

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