P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Very low $r_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Drain current (DC)	$-I_D$	max.	350 mA
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$r_{DS(on)}$	max.	6 Ω
Gate threshold voltage	$-V_{GS(th)}$	max.	3.5 V

MECHANICAL DATA Dimensions in mm

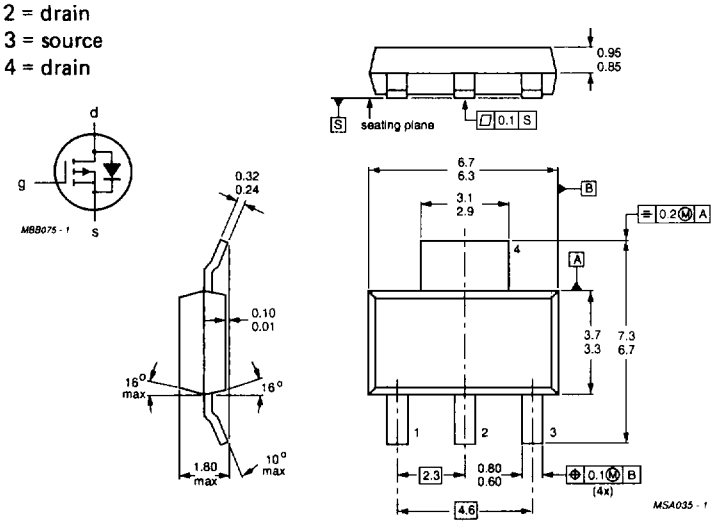
Fig.1 SOT223.

Marking code

BSP206

Pinning:

1 = gate
2 = drain
3 = source
4 = drain



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	350 mA
Drain current (peak)	$-I_{DM}$	max.	700 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 10 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60 V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1.0 μA
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$r_{DS(on)}$	typ. max.	4.5 Ω 6 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert Y_{fs} \rvert$	min. typ.	100 mS 200 mS
Input capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	55 pF 70 pF
Output capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 pF 45 pF
Feedback capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on}	typ. max.	4 ns 8 ns
	t_{off}	typ. max.	15 ns 25 ns

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

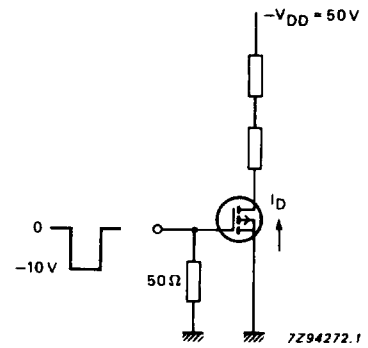


Fig.2 Switching time test circuit.

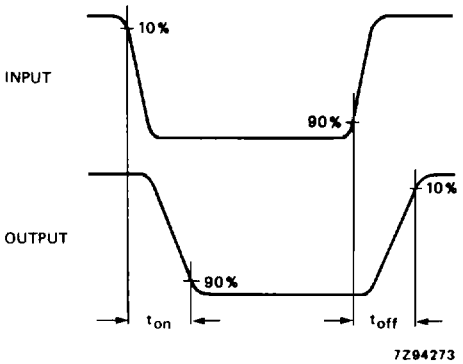


Fig.3 Input and output waveforms.

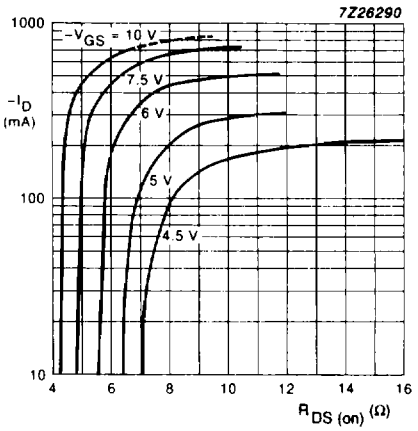


Fig.4 ON-resistance as a function of drain current; T_j = 25 °C; typical values.

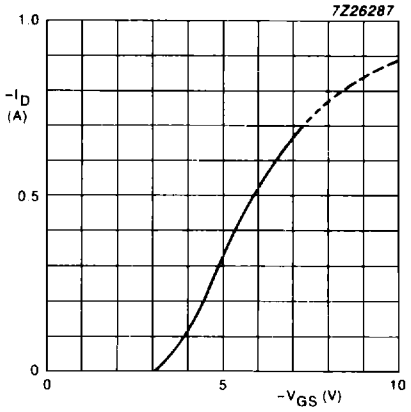


Fig.5 Transfer characteristics; $-V_{DS}$ = 10 V; T_j = 25 °C; typical values.

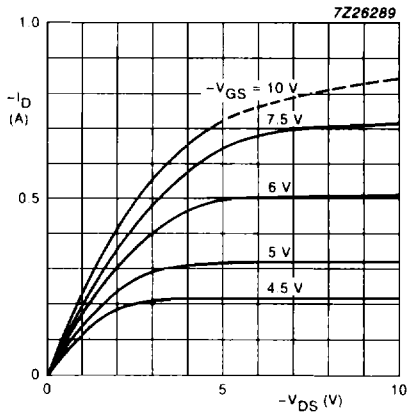


Fig.6 Output characteristics; T_j = 25 °C; typical values.

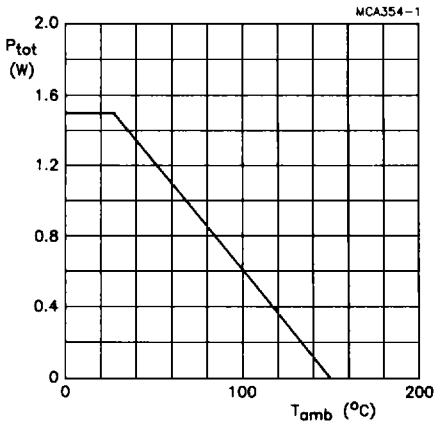


Fig.7 Power derating curve.

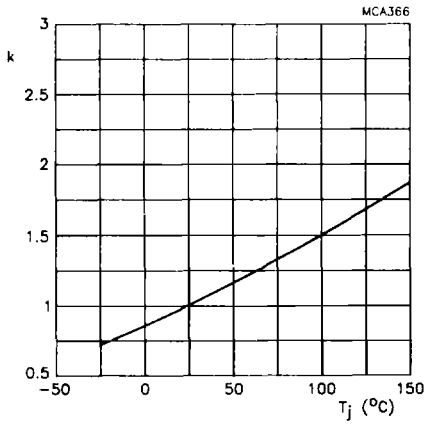


Fig.8 $k = \frac{r_{DS(on)} \text{ at } T_j}{r_{DS(on)} \text{ at } 25\ ^oC}$; at −200 mA/−10V; typical values.

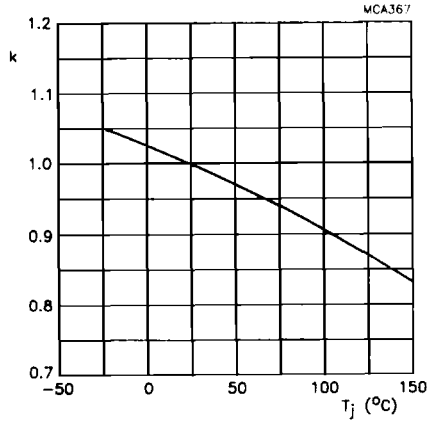


Fig.9 $k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\ ^oC}$; $-V_{GS(th)}$ at −1 mA; typical values.

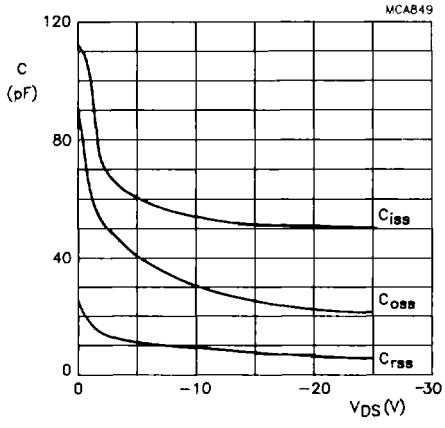


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.