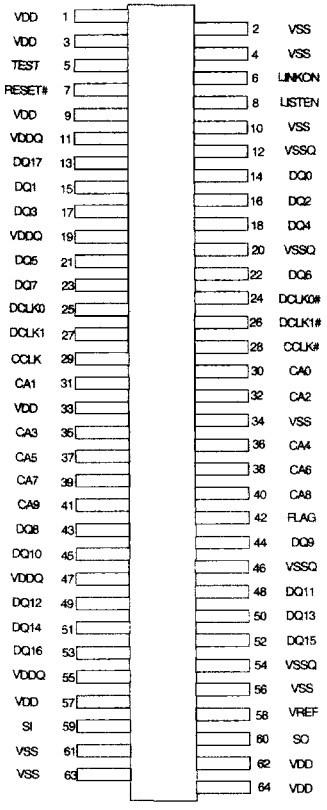
FEATURES

- Very High Speed - 600MHz data rate
- 1.2 GB/s peak I/O Bandwidth - provides very high bandwidth over narrow system memory bus
- Pipelined (Command) operation - Up to 8 transaction (in one bank,or spread across multiple banks)
- Eight (this data sheet) or more internal banks for hiding row access / precharge
- Programmable burst lengths of 4 or 8
- 100 % peak bandwidth sustainable over random row as well as random column access, even with 8 byte bursts
- Packet Oriented Protocol - Provided pin compatibility access multiple densities.
- Auto Refresh and Self Refresh
- Command Clock for commands and addresses; Bidirectional Data Clocks for read and write data
- Dual Data Clocks provide smooth handoff from one data source to another
- Programmable Offset between Data and Data Clocks
- Programmable Read Delays - Adjustable in coarse increments equal to one data bit time, and fine increments which are a fraction of a bit time ; allows for specific temporal placement of data at the memory controller data pins
- Programmable Write Delays - Adjustable in coarse increments equal to one data bit time. Allows for optimally adjusted write data placement by the memory controller
- Supports bank accesses (bank initially idle) and page accesses (bank active, row open)
- 128ms, 16K-cycle refresh
- SLIO interface Technology - Drivers: calibrated V_{OH} and V_{OL} levels, Receivers: narrow set-up and hold windows
- Single +2.5V ± 5% power supply

PIN ASSIGNMENT (TOP VIEW)
64 – Pin VSMP
(400mil width, .4/.8mm pitch)



GENERAL DESCRIPTION

The HYSLU144183PC60M SLDRAM is a synchronous, very high-speed, packet-oriented, pipelined dynamic random access memory containing 150, 994, 994 bits. The HYSLU144183PC60M SLDRAM is internally configured as eight banks of 256K x 72 ; each of the 256K x 72 banks is organized as 2048 rows by 18 columns by 72 bits . The 72 bits per column access are transferred over the I/O interface in a burst of four 18-bit words.

All transitions begin with a request packet. Read and write request packets contain the specific and write data are transferred in packets; a single

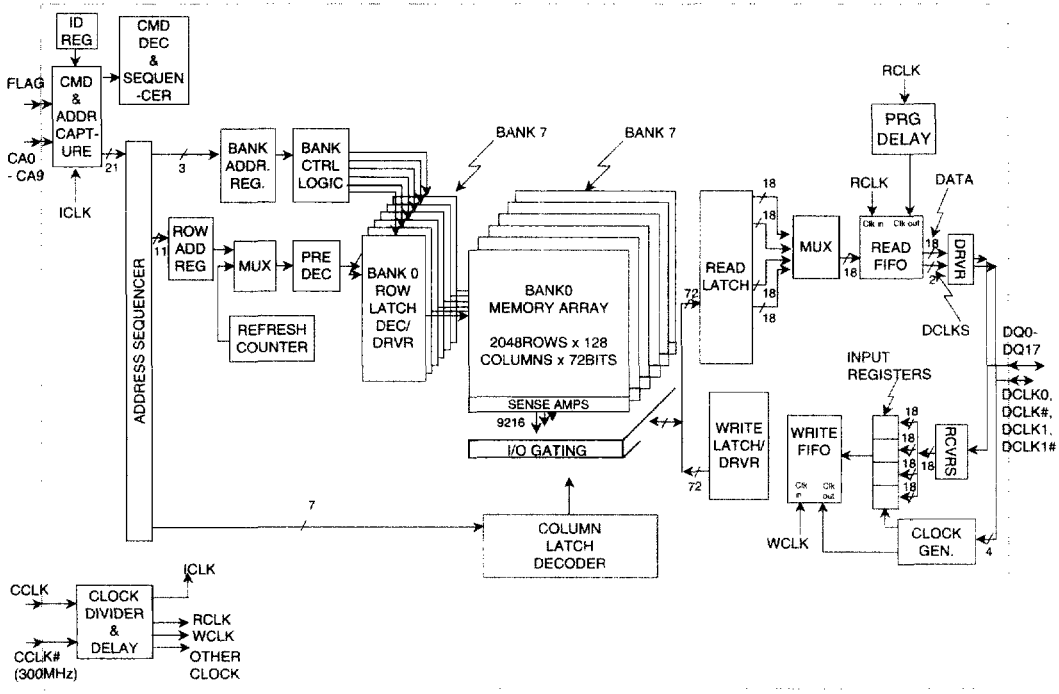
column access involves the transfer of single data packet, which is a burst of four 18-bit words. Data from either or two columns in page may be accessed with a single request packet, the latter results in a continuous burst of eight 18-bit data words, or to the open row in a active banks. Read or write requests indicate whether to leave the row open after access, or to perform a self-timed precharge at the completion of the access (auto-precharge).

The HYSLU144183PC60M uses a pipelined architecture and multiple internal banks to achieve high-speed operation and high effective bandwidth. Precharging one bank while accessing another bank will hide the precharge cycles, and provide seamless high-speed random access operation. The HYSLU144183PC60M is designed to operate in 2.5V memory systems. An auto-refresh mode is provided along with two power saving modes, standby and shutdown. The HYSLU144183PC60M includes SLIO interface technology.

SLDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a very high data rate with automatic column address generation, the ability to interleave between several internal banks in order to hide precharge time, and the capability to provide a continuous burst of data across random row and/or column location, even with 8-byte granularity.

Terminology - the term "tick" is used throughout this data sheet as the equivalent of one-half of the CCLK clock period. Also, for simplicity the clocks will be referred to and shown as CCLK, DCLK0 and DCLK1.
It should be understood that these are differential clocks and that each has a complementary signal. Any reference to a specific edge of a particular clock refers to the true version of that clock (e.g. CCLK) not the complement (e.g. CCLK#)

FUNCTIONAL BLOCK DIAGRAM



VSMP PIN NUMBER	SYMBOL	TYPE	DESCRIPTION
29,28	CCLK CCLK#	CMOS	Command Clock (differential) : CCLK is driven by the memory controller (or s separate clock chip) coincident with the leading edges of the command bits. SLDRAM command input signals are effectively sampled at each crossing of internally delayed versions of CCLK/CCLK#. Read clocks, write clocks, and other internal clocks are derived from CCLK.
25, 24, 27, 26	DCLK0 DCLK0# DCLK1 DCLK1#	SLIO Input/ Output	Date Clocks (differential) : For a read access, the specified pair of DCLK0/DCLK0# or DCLK1/DCLK1# is driven by the SLDRAM, and for write accesses, the SLDRAM provides 2 crossing on the selected DCLK pair to, and then 1 crossing coincident with, the beginning of each valid data word. During write accesses, the SLDRAM uses a delayed version of the DCLK pair received with the data to capture the data.
59,60	SI, SO	LVCOMS Input, Output	Select In, Select Out : The controller and all SLDRAM on a channel are connected in series using these pins. This connection is used to initialize the SLDRAM.
6	LINKON	LVCMOS Input	Link On : Used to enter and exit Shutdown mode.
7	RESET#	LVCMOS Input	Reset# : Provides a hardware reset; resets all logic, including the ID register. Memory contains are not affected. An SLDRAM must be initialized following hardware reset.
8	LISTEN	LVCMOS Input	Listen : Used to enter and exit Standby mode.
42	FLAG	SLIO Input	Flag : FLAG HIGH indicates the start of a valid request packet; FLAG then goes LOW for the remainder of the packet. FLAG LOW at any other time is interpreted as a NOP.
30 -32, 35 - 41	CA0 - CA9	SLIO Input	Command, Address : Commands, Addresses and /or Register Write Data be transferred on these signals, in packets of four words.
14 - 18, 21 - 23 43 - 45, 48 - 53	DQ0 - DQ17	SLIO Input/ Output	Data I/O : Data bus.
5	TEST	-	Test Pin : Should be tied to Vss during normal operation.
58	V_{REF}	-	Reference voltage
11,19,47,55	V_{DDQ}	Supply	DQ Power : Provide isolated power to DQs for improved noise immunity
12,20,46,54	V_{SSQ}	Supply	DQ Ground : Provide isolated ground to DQs for improved noise immunity
1, 3, 9, 33, 57, 62, 64	V_{DD}	Supply	Power Supply : +2.5V±5%
2,4,10,34,56, 61,63	V_{SS}	Supply	Ground.