

SPICE Device Model SiB415DK Vishay Siliconix

P-Channel 30-V (D-S) MOSFET

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

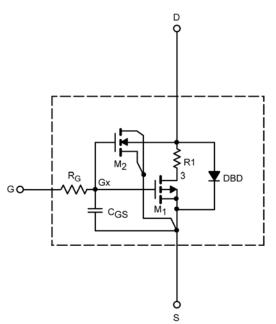
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125° C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

SUBCIRCUIT MODEL SCHEMATIC

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

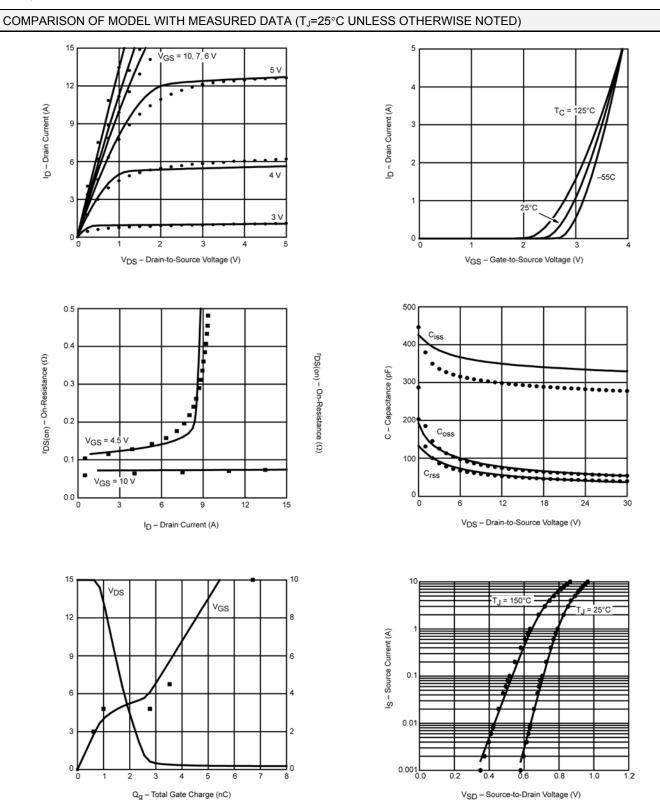


| SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED) | | | | | |
|---|---------------------|---|-------------------|------------------|------|
| Parameter | Symbol | Test Condition | Simulated Data | Measured Data | Unit |
| Static | | | | | |
| Gate Threshold Voltage | V _{GS(th)} | V_{DS} = V_{GS} , I_D = -250 μ A | 2 | | V |
| On-State Drain Current ^a | I _{D(on)} | $V_{\text{DS}} \geq -5 \text{ V}, V_{\text{GS}} = -10 \text{ V}$ | 58 | | А |
| Drain-Source On-State Resistance ^a | r _{DS(on)} | V_{GS} = -10 V, I _D = -4.17 A | 0.073 | 0.072 | Ω |
| | | V_{GS} = -4.5 V, I _D = -3.1 A | 0.124 | 0.130 | |
| Forward Transconductance ^a | 9 _{fs} | V_{DS} = -15 V, I _D = -4.17 A | 8 | 5.5 | S |
| Diode Forward Voltage ^a | V _{SD} | I _S = -3.2 A | -0.83 | -0.80 | V |
| Dynamic ^b | | • | • | | |
| Input Capacitance | C _{iss} | V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz | 345 | 295 | pF |
| Output Capacitance | C _{oss} | | 72 | 70 | |
| Reverse Transfer Capacitance | C _{rss} | | 51 | 50 | |
| Total Gate Charge | Qg | V_{DS} = -15 V, V_{GS} = -10 V, I_D = -4.17 A | 5.6 | 6.7 | nC |
| | | V_{DS} = -15 V, V_{GS} = -4.5 V, I_{D} = -4.17 A | 3 | 3.5 | |
| Gate-Source Charge | Q _{gs} | | 1 | 1 | |
| Gate-Drain Charge | Q_gd | | 1.78 | 1.78 | |

Notes a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2%. b. Guaranteed by design, not subject to production testing.



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Note: Dots and squares represent measured data.



Vishay

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