



CED3252/CEU3252

N-Channel Enhancement Mode Field Effect Transistor

FEATURES

- 30V, 25A, $R_{DS(ON)} = 28m\Omega$ @ $V_{GS} = 10V$.
 $R_{DS(ON)} = 39m\Omega$ @ $V_{GS} = 4.5V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- Lead free product is acquired.
- TO-251 & TO-252 package.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	25	A
Drain Current-Pulsed ^a	I_{DM}	100	A
Maximum Power Dissipation @ $T_C = 25^\circ C$ - Derate above $25^\circ C$	P_D	31	W
		0.25	W/ $^\circ C$
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	4	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ C/W$



CED3252/CEU3252

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30V, V_{GS} = 0V$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	1.0		3.0	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 7A$		22	28	$m\Omega$
		$V_{GS} = 4.5V, I_D = 3.5A$		30	39	$m\Omega$
Dynamic Characteristics^d						
Forward Transconductance	g_{FS}	$V_{DS} = 15V, I_D = 7A$		4		S
Input Capacitance	C_{iss}	$V_{DS} = 15V, V_{GS} = 0V, f = 1.0\text{ MHz}$		610		pF
Output Capacitance	C_{oss}			145		pF
Reverse Transfer Capacitance	C_{rss}			95		pF
Switching Characteristics^d						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15V, I_D = 7A, V_{GS} = 10V, R_{GEN} = 3\Omega$		9	20	ns
Turn-On Rise Time	t_r			3	8	ns
Turn-Off Delay Time	$t_{d(off)}$			24	50	ns
Turn-Off Fall Time	t_f			4	10	ns
Total Gate Charge	Q_g	$V_{DS} = 15V, I_D = 7A, V_{GS} = 10V$		12.3	16	nC
Gate-Source Charge	Q_{gs}			1.5		nC
Gate-Drain Charge	Q_{gd}			2.5		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current ^b	I_S				2.3	A
Drain-Source Diode Forward Voltage ^c	V_{SD}	$V_{GS} = 0V, I_S = 2.3A$			1.2	V
Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Surface Mounted on FR4 Board, $t \leq 10$ sec. c.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. d.Guaranteed by design, not subject to production testing.						



CED3252/CEU3252

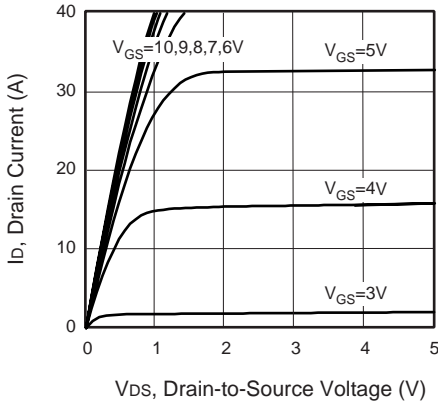


Figure 1. Output Characteristics

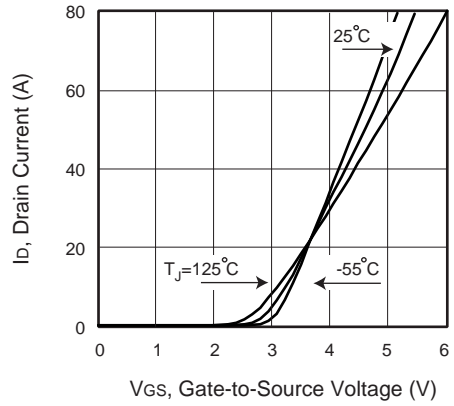


Figure 2. Transfer Characteristics

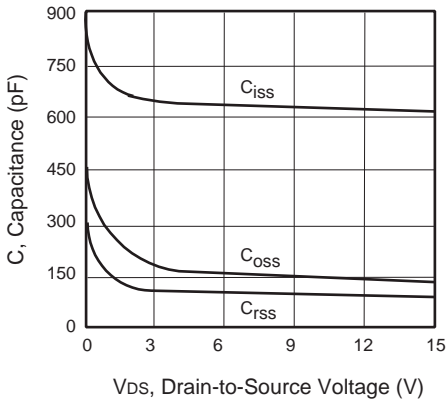


Figure 3. Capacitance

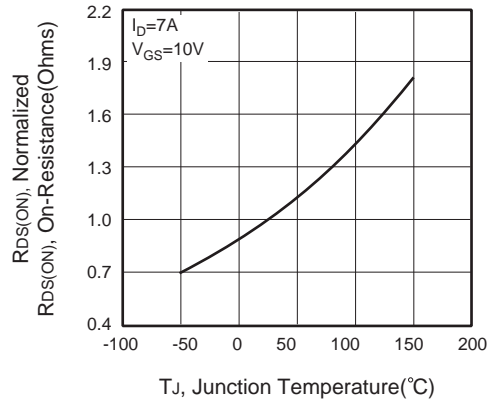


Figure 4. On-Resistance Variation with Temperature

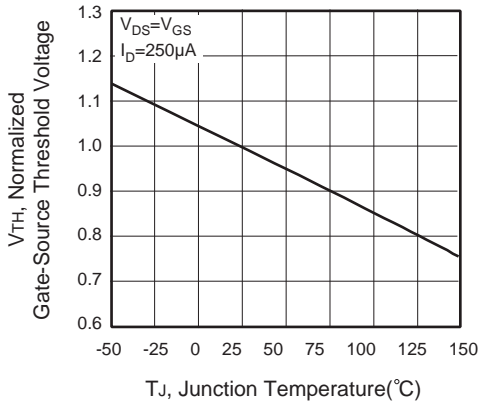


Figure 5. Gate Threshold Variation with Temperature

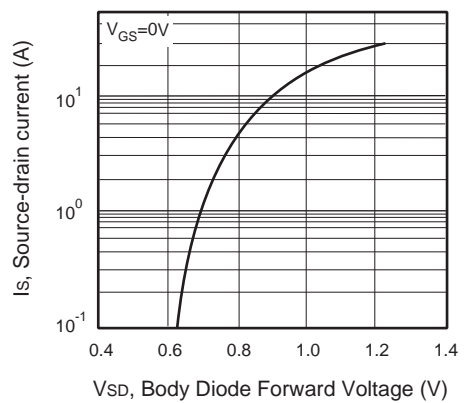


Figure 6. Body Diode Forward Voltage Variation with Source Current



CED3252/CEU3252

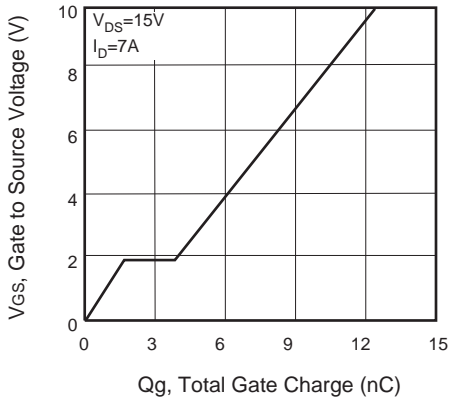


Figure 7. Gate Charge

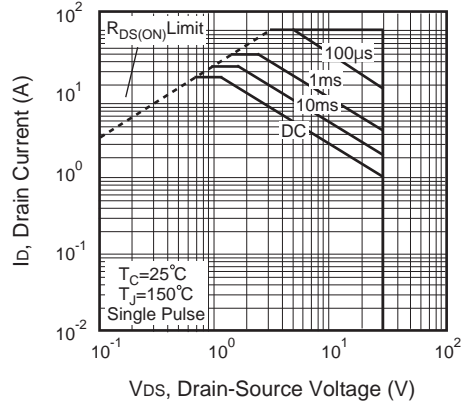


Figure 8. Maximum Safe Operating Area

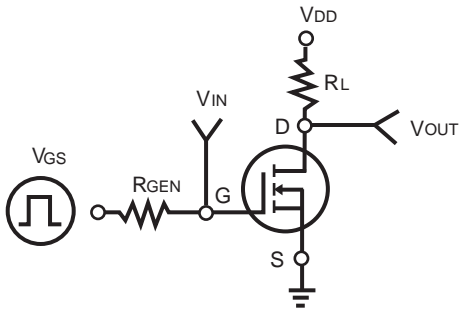


Figure 9. Switching Test Circuit

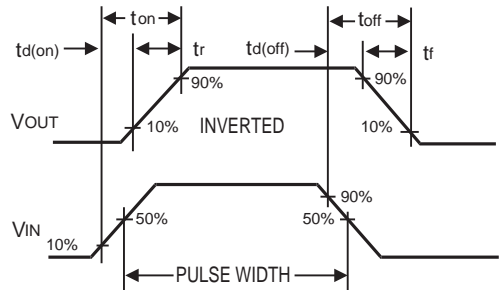


Figure 10. Switching Waveforms

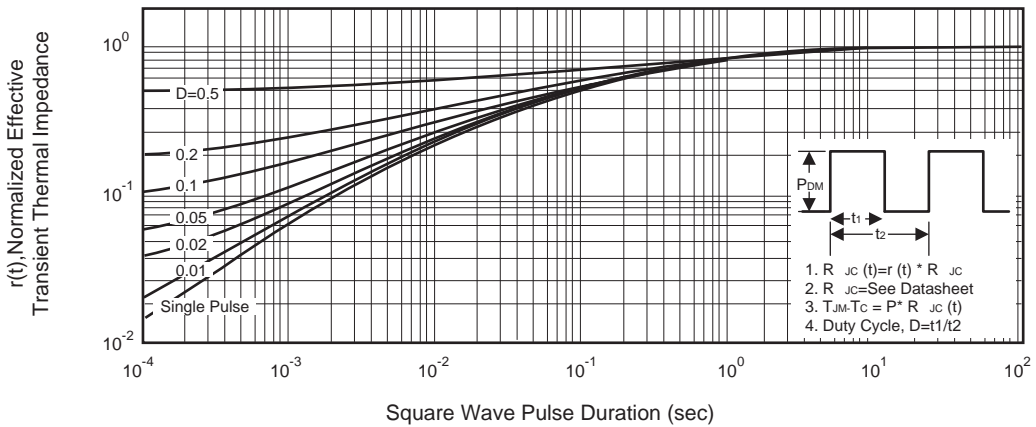


Figure 11. Normalized Thermal Transient Impedance Curve