PLESSEY Semiconductors

T-51-10-10

ZN503AJ/ZN504CJ/ZN504E

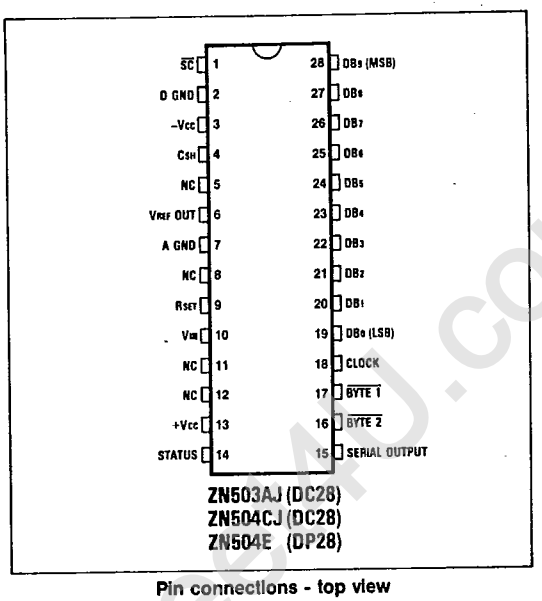
10-BIT MICROPROCESSOR-COMPATIBLE A-D CONVERTERS WITH PARALLEL/SERIAL OUTPUT

The ZN503/4 range of fast successive approximation A-D converters combine several innovations on a monolithic silicon integrated circuit. This 28 pin device consists of a current switching array (requiring no trim), successive approximation logic, 2.5V precision reference, reference amplifier, comparator and 3-state parallel and serial output buffers.

The ZN503/4 has 3 pin-programmable input ranges and only two external components are required to perform a full 10-bit A-D conversion. No user trims ae required and the provision of a serial output makes the device ideal for high resolution remote sensing applications.

FEATURES

- Choice of Linearity: ½ LSB - ZN503
  1 LSB - ZN504
- 15 microseconds Typical, 20 microseconds Guaranteed Conversion Time
- 3-State Parallel and Serial Outputs
- Only 2 External Components Required
- 3 Pin-Programmable Input Ranges
- Asynchronous START CONVERT Pulse
- Microprocessor, TTL and CMOS Compatible
- Full 8 or 16-Bit Micro-Bus Interface
- Available in 28 Pin Moulded or Ceramic DIL



ZN503AJ (DC28)
ZN504CJ (DC28)
ZN504E (DP28)

Pin connections - top view

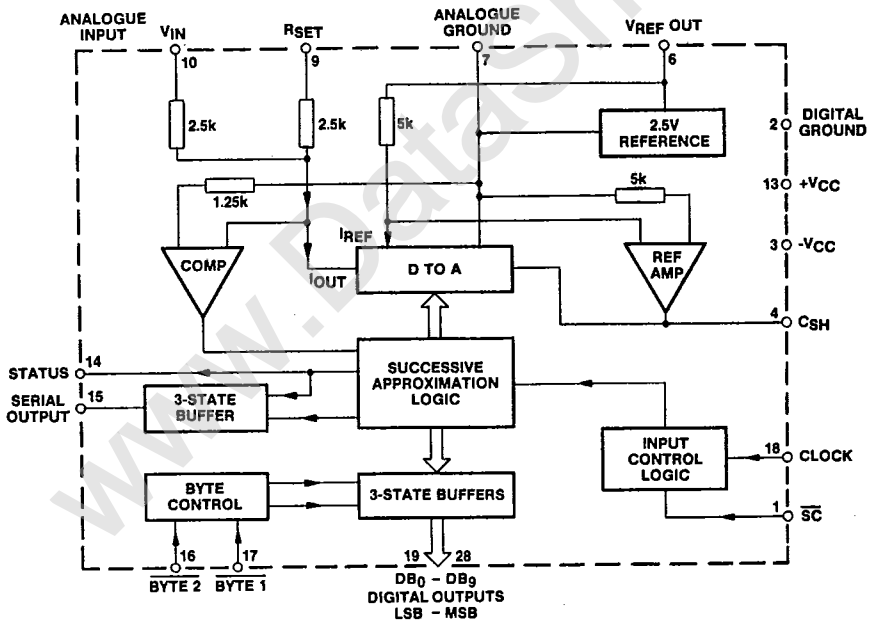


Fig.1 System diagram

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN504E	0°C to +70°C	DP28
ZN504CJ	0°C to +70°C	DC28
ZN503AJ	-55°C to +125°C	DC28

ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc+	+7V
Supply voltage Vcc-	-7V
Logic input voltage	+Vcc and 0V
Operating temperature range	0°C to +70°C (ZN504E, ZN504CJ) -55°C to +125°C (ZN503AJ)
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS (at +5 and −5V supplies and internal reference unless otherwise specified).

Parameter	Version	T_{amb} = +25°C			Over spec.		Units	Conditions
		Min.	Typ.	Max.	Min.	Max.		
	ZN503AJ							
Linearity error		–	–	±0.5	–	±0.5	LSB	
Diff. linearity error		–	–	±0.5	–	±0.5	LSB	Note 1
Unipolar offset		–	±1.0	±2.0	–	±2.0	LSB	Note 2
Bipolar offset		–	±1.0	±2.0	–	±2.0	LSB	Note 2
Gain error		–	±4.0	–	–	–	LSB	Note 2
TEMPERATURE COEFFICIENTS (T_{min} to T_{max})								
Unipolar offset			10 typ., 15 max.				ppm/°C	
Bipolar offset			10 typ., 15 max.				ppm/°C	
Gain			60 typ.				ppm/°C	
	ZN504CJ							
Linearity error		–	–	±1.0	–	±1.0	LSB	
Diff. linearity error		–	–	±0.75	–	±0.75	LSB	Note 1
Unipolar offset		–	±1.0	±2.0	–	±2.0	LSB	Note 2
Bipolar offset		–	±1.0	±2.0	–	±2.0	LSB	Note 2
Gain error		–	±4.0	±6.0	–	–	LSB	Note 2
TEMPERATURE COEFFICIENTS (T_{min} to T_{max})								
Unipolar offset			20 typ., 30 max.				ppm/°C	Note 2
Bipolar offset			20 typ., 30 max.				ppm/°C	Note 2
Gain			60 typ.				ppm/°C	Note 2
	ZN504E	Parameter values as for ZN504CJ						
	All types							
Resolution		10	–	–	–	–	bits	
Conversion time (min)		10	15	20	15	20	μs	Note 4

PLESSEY SEMICONDUCTORS

T-51-10-10

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Version	$T_{amb} = +25°C$ Min.	Typ.	Max.	Over spec Min.	Max.	Units	Conditions
Nominal analogue input ranges	All types	0 to +2.5					V	Note 5, 8
		0 to +5.0					V	Note 6, 8
		−2.5 to +2.5					V	Note 7, 8
Supply rejection		−	0.1	−	−	−	% per V	
Supply voltage $+V_{CC}$		+4.5	+5.0	+5.5	+4.5	+5.5	V	
$-V_{CC}$		−4.5	−5.0	−5.5	−4.5	−5.5	V	
Supply current $+I_{CC}$		−	36	44	−	−	mA	$+V_{CC} = +5V$
$-I_{CC}$		−	23	32	−	−	mA	$-V_{CC} = -5V$
Power consumption		−	295	380	−	−	mW	
INTERNAL VOLTAGE REFERENCE								
Output voltage	All types	−	2.480	−	−	−	V	
Output voltage tolerance	ZN503AJ	−	−	±3.0	−	−	%	
	ZN504CJ	−	−	±3.0	−	−	%	
	ZN504E	−	−	±5.0	−	−	%	
V_{REF} temp. coeff.	All types	−	−	−	26	50	ppm/°C	
Slope impedance		−	0.75	−	−	−	Ω	
Max. ext. load current		−	±2.0	−	−	−	mA	
LOGIC	All types							
$\overline{\text{START CONVERT}}$ $\overline{\text{SC}}$								
High level input voltage		2.0	−	−	2.0	−	V	
Low level input voltage		−	−	0.8	−	0.8	V	
High level input current		−	18	−	−	−	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 5.5V$
High level input current		−	8.0	−	−	−	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 2.4V$
Low level input current		−	4.0	−	−	−	μA	$V_{CC} = \pm 5.5V$ $V_{in} + 0.4V$
LOGIC	All types							
$\overline{\text{BYTE}}$ 1 and 2								
High level input voltage		2.0	−	−	2.0	−	V	
Low level input voltage		−	−	0.8	−	0.8	V	
High level input current		−	18	−	−	−	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 5.5V$
High level input current		−	12	−	−	−	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 2.4V$
Low level input current		−	2.0	−	−	−	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 0.4V$

ELECTRICAL CHARACTERISTICS (Cont.)

T-51-10-10

Parameter	Version	T_{amb} = +25°C			Over spec.		Units	Conditions
		Min.	Typ.	Max.	Min.	Max.		
CLOCK	All types							
CLOCK high period		0.5	–	–	–	–	μs	
Max. clock frequency		550	730	1100	550	730	KHz	
High level input voltage		2.0	–	–	2.0	–	V	
Low level input voltage		–	–	0.8	–	0.8	V	
High level input current		–	15	–	–	–	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 5.5V$
High level input current		–	5.0	–	–	–	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 2.4V$
Low level input current		–	1.5	–	–	–	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 0.4V$
DATA OUTPUTS								
High level output voltage	All types	2.4	–	–	2.4	–	V	$I_{OH} = -700\mu A$
Low level output voltage		–	–	0.4	–	0.4	V	$I_{OL} = 2mA$
High level output current		–	–	−700	–	–	μA	$V_{OH} = 2.4V$
Low level output current		–	–	2.0	–	–	mA	$V_{OL} = 0.4V$
3-state DISABLE output leakage		–	–	±2.0	–	–	μA	$V_{out} = 1.3V$
ENABLE/DISABLE								
Delay time TE1		100	220	260	–	–	ns	Note 3
TEO		60	80	100	–	–	ns	
TD1		100	120	140	–	–	ns	
TDO		30	60	100	–	–	ns	
$\overline{SC}$ pulse width		100	–	–	–	–	ns	
$\overline{SC}$ input to STATUS		–	180	–	–	–	ns	
STATUS OUTPUT								
High level O/P Voltage		2.4	–	–	–	–	V	$I_{OH} = 40\mu A$
Low level O/P Voltage		–	–	0.4	–	–	V	$I_{OL} = 1.6mA$
High level O/P current		–	–	−350	–	–	μA	$V_{OH} = 2.4V$
Low level O/P current		–	–	1.6	–	–	mA	$V_{OL} = 0.4V$

Note 1 No missing codes over full temperature range at appropriate accuracy.

Note 2 No user trims are available for either zero or gain error.

Note 3 Refer to Fig. 9.

Note 4 The maximum conversion time is 20μs. This corresponds to a clock rate of 550KHz based on 11 clock periods per conversion cycle (see Fig. 4). This provides an update rate of 50KHz.

Note 5 R_{set} (pin 9) connected to analogue input (pin 10).

Note 6 R_{set} (pin 9) connected to analogue ground (pin 7).

Note 7 R_{set} (pin 9) connected to $V_{REF\ OUT}$ (pin 6).

Note 8 The scaling resistors used to define the 3 analogue input ranges are fabricated on-chip to improve thermal tracking. These resistors are accurately matched but each has an absolute tolerance of typically ±30%.

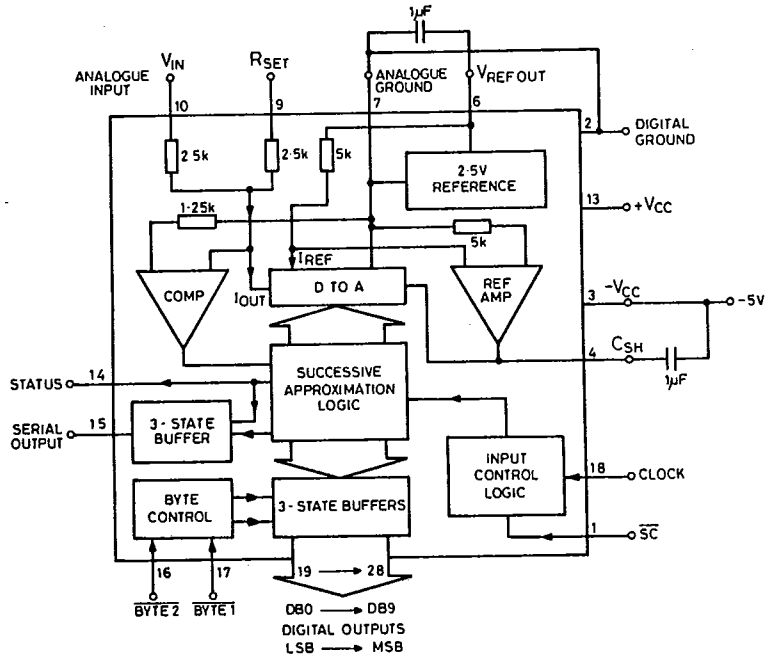


Fig. 2 Typical external components

GENERAL CIRCUIT OPERATION

The ZN503/4 utilises the successive approximation technique. Upon receipt of a negative-going pulse at the $\overline{SC}$ input the STATUS output goes low, and the D-A converter input is set to the MSB. The resulting analogue output is compared with the unknown analogue input signal by means of the comparator. If the analogue input is the larger, the MSB is left in circuit and if not the MSB is removed. On the second clock pulse this sequence is repeated for the next most significant bit and so on until all the 10-bits have been compared. On the 11th negative clock edge STATUS goes high indicating that the conversion is complete and that the data is valid.

Parallel and serial outputs

The ZN503/4 is micro-bus compatible with the 3-state parallel output buffers enabled by two byte control pins. During a conversion $\overline{BYTE}$ 1 and $\overline{BYTE}$ 2 will normally be held high to keep the 3-state buffers in their high impedance state. At the end of conversion STATUS returns high and data can be read out by taking either $\overline{BYTE}$ 1 and/or $\overline{BYTE}$ 2 low thus enabling the appropriate data outputs. $\overline{BYTE}$ 1 controls the 8 MSB's and $\overline{BYTE}$ 2 the 2 LSB's. Readout is non-destructive.

The serial output operates in a different manner in that its 3-state output buffer is enabled when STATUS is low, i.e. during a conversion. Data appears at the serial output after each bit decision and is valid at the subsequent positive edges of the clock.

CONVERSION TIMING

Parallel output

The ZN503/4 will accept a low-going $\overline{\text{START CONVERT}}$ pulse, which can be completely asynchronous with respect to the clock and will produce valid data between 10.5 and 11.5 clock pulses later depending on the relative timing of the CLOCK and $\overline{\text{START CONVERT}}$ signals.

The converter is cleared by a low-going $\overline{\text{START CONVERT}}$ pulse, which sets the most significant bit and resets all the other bits and STATUS. Whilst the $\overline{\text{START CONVERT}}$ input is low the MSB output of the D-A converter is continuously compared with the analogue input, but otherwise the converter is inhibited. After the $\overline{\text{START CONVERT}}$ input goes high again the MSB decision is made and the successive approximation routine runs to completion.

The $\overline{\text{SC}}$ pulse can be as short as 100ns; however the MSB must be allowed to settle for at least 625ns before the MSB decision is made. To ensure that this criterion is met even with short $\overline{\text{SC}}$ pulses the converter waits, after the $\overline{\text{SC}}$ input goes high, for a rising clock edge followed by a falling clock edge, the MSB decision being taken on the falling clock edge. This ensures that the MSB is allowed to settle for at least half a clock period, or 625ns at maximum clock frequency. The clock high period and the $\overline{\text{SC}}$ pulse width must comply with this settling time i.e. clock high period + $\overline{\text{SC}}$ pulse width $\geqslant$ 625ns.

During a conversion the $\overline{\text{SC}}$ input is not locked out and if it is pulsed low at any time the conversion will restart.

At the end of a conversion STATUS waits 1 clock cycle before going high, so indicating that data is valid. The data outputs can thus be enabled anytime during a conversion and valid data will be available on the rising edge of the STATUS signal.

Serial output

The serial output will remain in a high impedance state until a low going $\overline{\text{START CONVERT}}$ pulse is received, which can be completely asynchronous with respect to the clock. On the negative edge of this pulse the STATUS output goes low indicating to the user that the conversion has commenced. Whilst the $\overline{\text{START CONVERT}}$ is held low, the serial output will remain in an indeterminate state and the converter will be inhibited. Once the $\overline{\text{START CONVERT}}$ input returns high the MSB decision is made between ½ and 1½ clock periods later. The serial output data is then available on positive edges of the clock, beginning with the MSB. Once the LSB decision has been made, the output returns to a high impedance state on the next negative edge of the clock, which is indicated by the STATUS output going high. The conversion takes between 10.5 and 11.5 clock periods depending on the relative timing of the CLOCK and $\overline{\text{START CONVERT}}$ pulses.

Serial data can easily be transferred into a 10-bit shift register on positive going clock edges after the STATUS signal has gone low. If the STATUS output is used to gate the clock to the shift register, it would contain all 10-bits of valid data after the STATUS returns high. A typical circuit diagram is shown in Fig. 3.

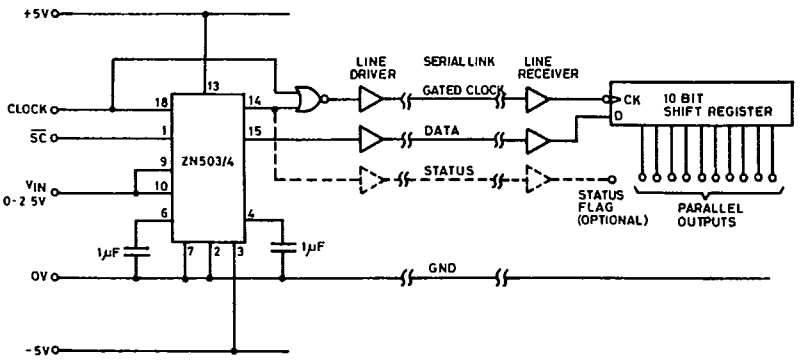


Fig. 3 A typical application of the serial output

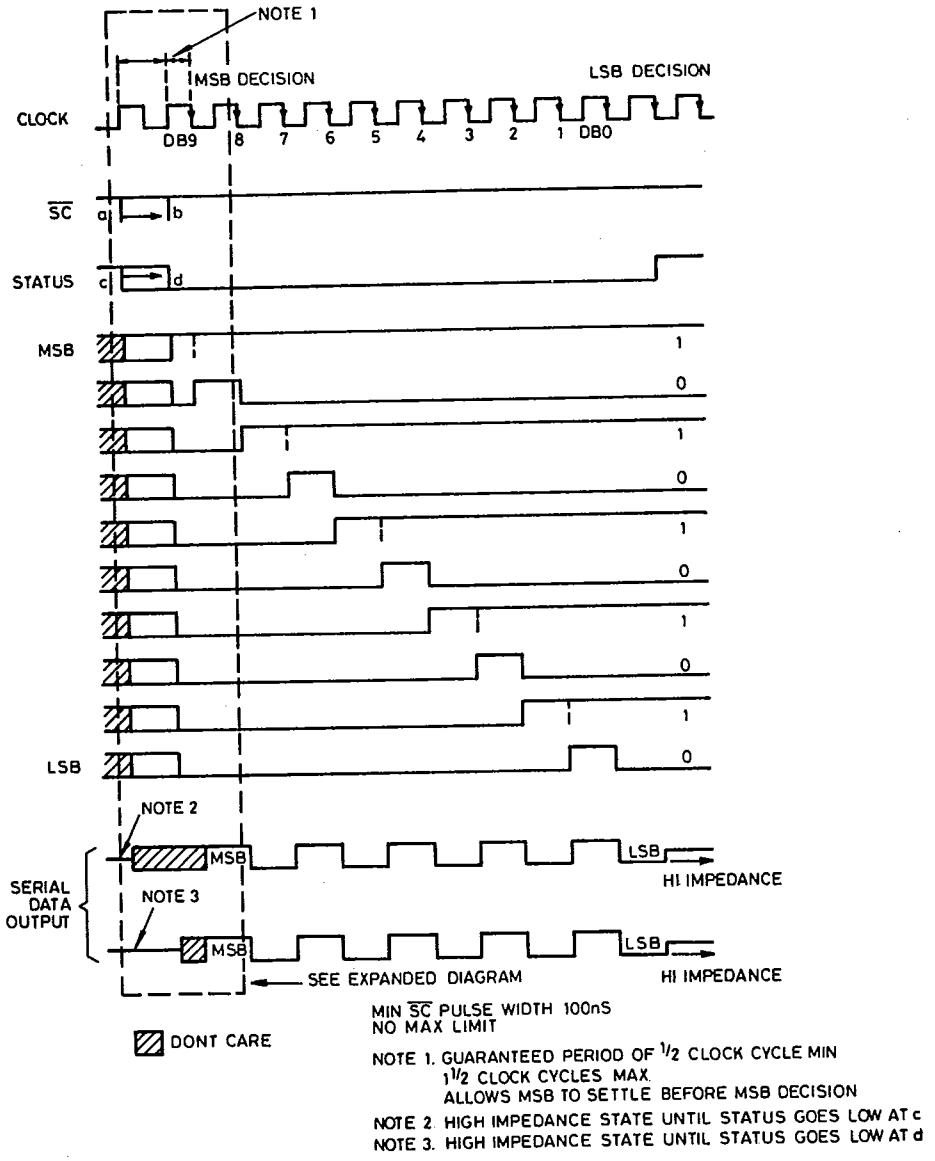


Fig. 4 Timing diagram

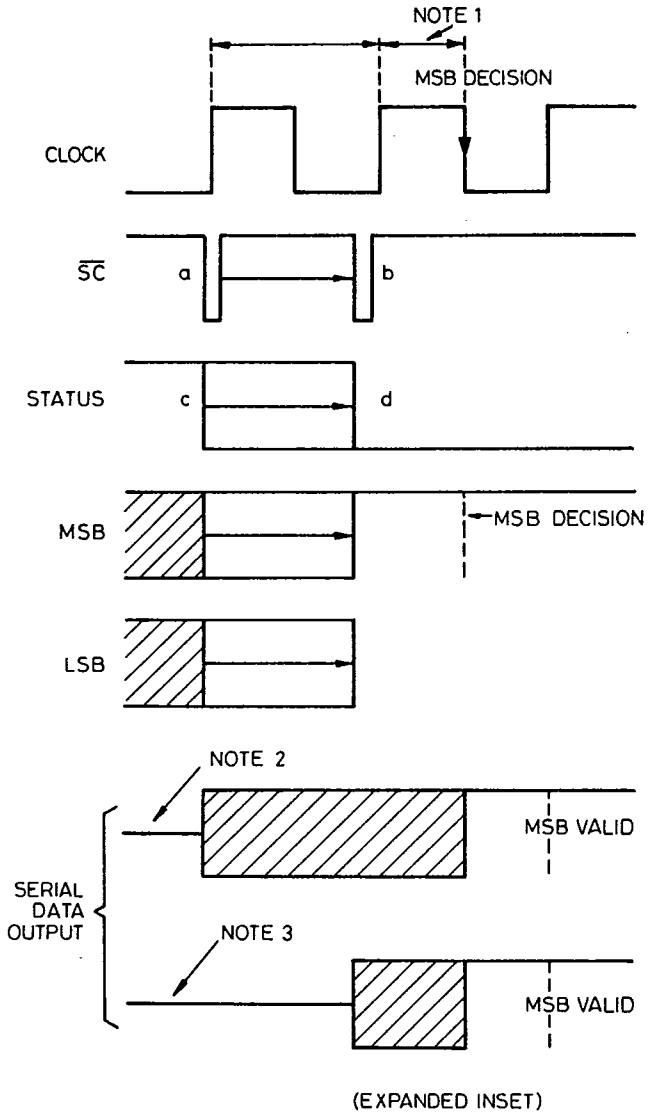


Fig. 5 Expanded timing diagram

CONTINUOUS CONVERSION

The converter can be made to cycle by inverting the STATUS output and feeding it back into the $\overline{SC}$ input. To ensure that the converter starts reliably after power up an initial start pulse is required. This can be ensured by using a NOR gate rather than of an inverter and feeding it with a positive going pulse which can be derived from a simple RC network that gives a single pulse when power is applied.

The propagation delay of the NOR gate determines the period over which STATUS remains high, during which time the data can be stored into latches. The time available for storing the data can be increased by inserting delays into the inverter path.

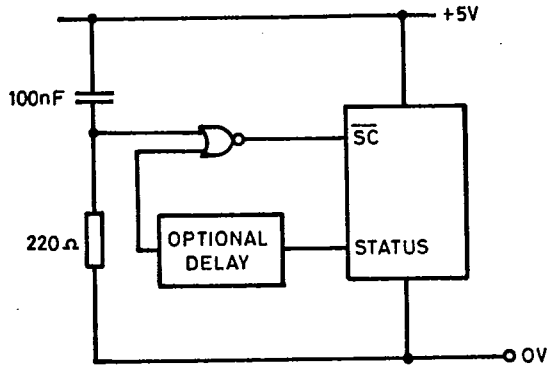


Fig. 6 Circuit for continuous conversion

PARALLEL DATA OUTPUTS

The ZN503/4 has true 3-state output buffers on-chip, hence eliminating the need for external buffers and latch circuitry.

The two byte select pins $\overline{BYTE}$ 1 and $\overline{BYTE}$ 2, control outputs DB9 to DB2, and outputs DB1 to DB0 respectively.

$\overline{BYTE}$ 1 and $\overline{BYTE}$ 2 will normally be held high during a conversion to keep the 3-state buffers in their high impedance state, and when data is ready, which will be signalled by a high going STATUS pulse, it can easily be read out by taking $\overline{BYTE}$ 1 and $\overline{BYTE}$ 2 low.

(A test circuit and timing diagram for the output enable/disable delays are given).

The STATUS output shown utilises a 5K internal pullup resistor for CMOS/TTL compatibility.

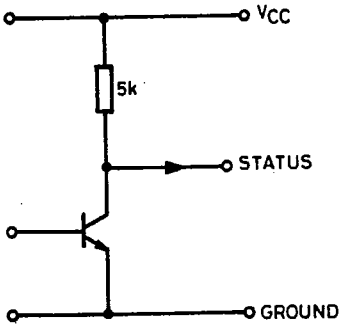


Fig. 7 Status output

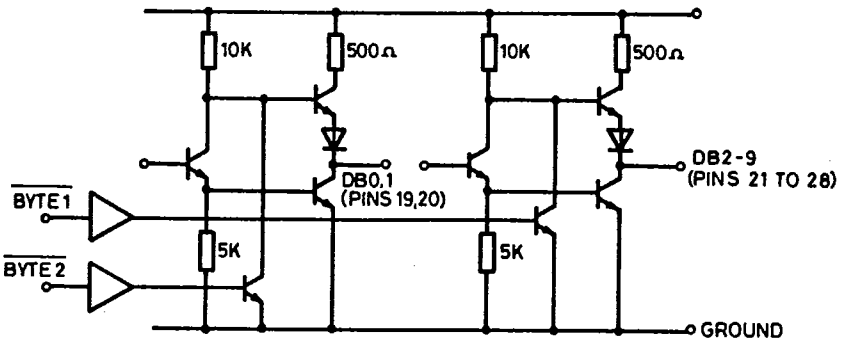
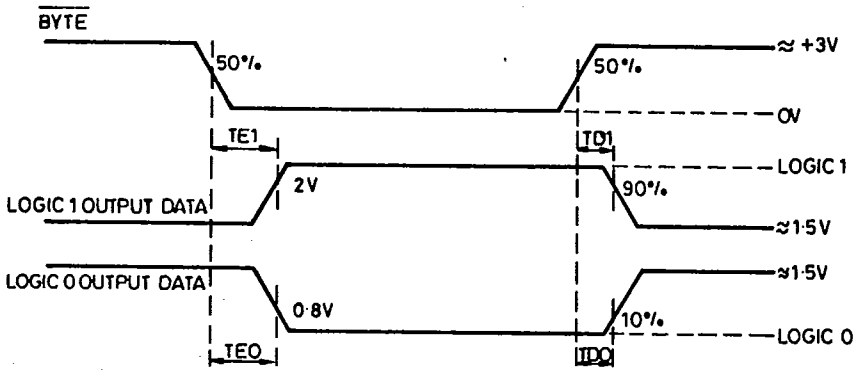


Fig. 8 Data outputs



TE = BYTE ENABLE DELAY TIME (CL = 50pF)
TD = BYTE DISABLE DELAY TIME (CL = 10pF)

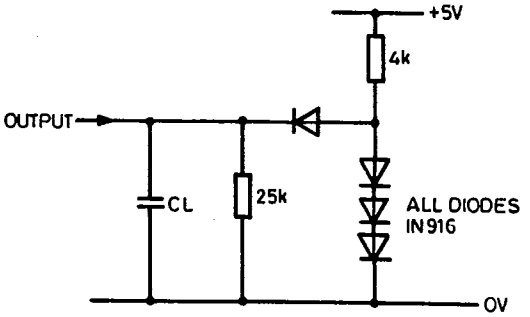


Fig. 9 Output enable/disable delays

DATA BUS CONNECTIONS

The ZN503/4 can be connected directly to an 8-bit microprocessor bus, where the two LSB's would normally be hardwired to the desired upper bits, usually the 2 MSB's. Hence the data would be transferred in two words with control of them, from $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2.

For use with a 16-bit microprocessor, $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2 would be tied together and all 10 bits would be enabled simultaneously. The 10-bit word could then be placed at either the higher or lower end of the 16-bit bus.

e.g.

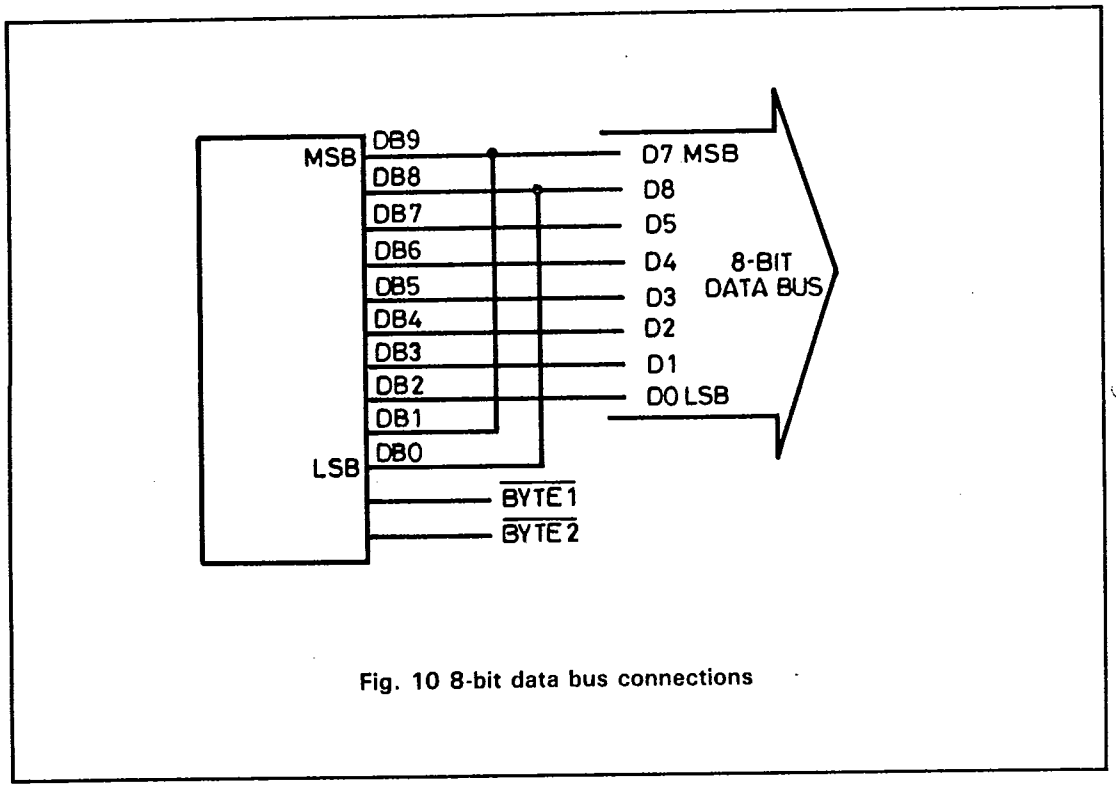


Fig. 10 8-bit data bus connections

$\overline{\text{BYTE}}$ 1	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2
	D7	D6	D5	D4	D3	D2	D1	D0
$\overline{\text{BYTE}}$ 2	DB1	DB0	X	X	X	X	X	X

DATA TRANSFERRED IN TWO WORDS

UNIPOLAR INPUT RANGES

V_{in} = 0 to +2.5V. R_{SET} (Pin9) connected to A_{in} (Pin10)

V_{in} = 0 to +5V. R_{SET} (Pin9) connected to A_{GND} (Pin7)

UNIPOLAR LOGIC CODING

Analogue input (Nominal code centre value)	Digital output code MSB LSB
FS - 1LSB	1111111111
FS - 2LSB	1111111110
¾.FS	1100000000
½.FS + LSB	1000000001
½.FS	1000000000
½.FS - 1LSB	0111111111
¼.FS	0100000000
1LSB	0000000001
0	0000000000

BIPOLAR INPUT RANGE

V_{in} = −2.5 to +2.5V. R_{SET} (Pin9) connected to $V_{REF\ OUT}$ (Pin6)

BIPOLAR LOGIC CODING

Analogue input (Nominal code centre value)	Digital output code MSB LSB
+(FS - 1LSB)	1111111111
+(FS - 2LSB)	1111111110
+(½.FS)	1100000000
+(1LSB)	1000000001
0	1000000000
−(1LSB)	0111111111
−(½.FS)	0100000000
−(FS - 1LSB)	0000000001
−FS	0000000000