Rev 0; 10/06

4-Channel Cold-Cathode Fluorescent Lamp Controller

DS3994

General Description

The DS3994 is a 4-channel controller for cold-cathode fluorescent lamps (CCFLs) that backlight liquid crystal displays (LCDs) in TV and PC monitor applications. The DS3994's features make it suitable for use in even the largest LCDs, while its low BOM cost makes it ideal for the entire range of LCD TVs and monitors.

The DS3994 can stagger the lamp bursts from each of the four channels. This feature allows scanning backlight schemes for video quality improvement to be implemented using a single CCFL controller IC, making it very simple and inexpensive to provide this enhancement. In addition, staggering the bursts from each channel can be used to minimize current ripple on the display power supply, which is especially important for larger LCDs. The relative stagger between each of the channels is programmable, so this feature can be tailored to the specific application.

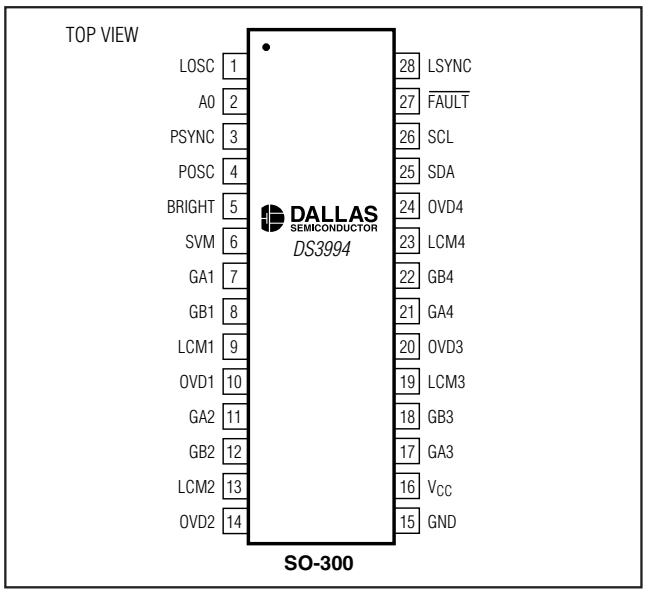
The DS3994 uses a push-pull drive architecture but it can also support full and half bridge drive schemes. Contact the factory for more details.

Applications

LCD Televisions

LCD PC Monitors

Pin Configurations



SO-300

Features

- **High-Density CCFL Controller for LCD TV and PC Monitor Backlights**
- **Programmable Staggered Start for Burst Dimming on Each Channel**
- **Strike Frequency Boost Option**
- **Programmable Strike Time**
- **Can Be Easily Cascaded**
- **Minimal External Components**
- **Analog Brightness Control**
- **Gate Driver Phasing Minimizes DC Supply Current Surges**
- **Per-Channel Lamp Fault Monitoring for Lamp Open, Lamp Overcurrent, Failure to Strike, and Overvoltage Conditions**
- **Accurate (±2%) On-Board Oscillator Lamp Frequency (20kHz to 80kHz)**
- **Wide Range On-Board DPWM Burst-Dimming Oscillator (22.5Hz to 440Hz)**
- **Can Be Synchronized to External Sources for the Lamp and DPWM Frequencies**
- **< 10% to 100% Dimming Range**
- **Soft-Start Minimizes Audible Transformer Noise**
- **I²C-Compatible Serial Port and On-Board Nonvolatile (NV) Memory Allow Device Customization**
- **3-Byte NV User Memory for Storage of Serial Numbers and Date Codes**
- **4.5V to 5.5V Single-Supply Operation**
- **-40°C to +85°C Temperature Range**
- **28-Pin SO (300 mils) Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS3994Z+	-40°C to +85°C	28 SO-300

+Denotes lead-free package.

Typical Operating Circuits appear at end of data sheet.

4-Channel Cold-Cathode Fluorescent Lamp Controller

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC}, SDA, and SCL Relative to Ground.....-0.5V to +6.0V
Voltage Range on Leads Other than V_{CC}, SDA, and SCL.....-0.5V to (V_{CC} + 0.5V), not to exceed +6.0V
Operating Temperature Range .....-40°C to +85°C
EEPROM Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....See J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	4.5		5.5	V
Input Logic 1	V_{IH}		2.2		V_{CC} + 0.3	V
Input Logic 0	V_{IL}		-0.3		0.8	V
SVM Voltage Range	V_{SVM}		-0.3		V_{CC} + 0.3	V
BRIGHT Voltage Range	V_{BRIGHT}		-0.3		V_{CC} + 0.3	V
LCM Voltage Range	V_{LCM}	(Note 2)	-0.3		V_{CC} + 0.3	V
OVD Voltage Range	V_{OVD}	(Note 2)	-0.3		V_{CC} + 0.3	V
Gate-Driver Output Charge Loading	Q_G				20	nC

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	G_A, G_B loaded with 600pF, 4 channels active		9	16	mA
Input Leakage (Digital Pins)	I_L		-1.0		+1.0	µA
Output Leakage (SDA, $\overline{FAULT}$)	I_{LO}	High impedance	-1.0		+1.0	µA
Low-Level Output Voltage (SDA, $\overline{FAULT}$)	V_{OL1}	I_{OL1} = 3mA			0.4	V
	V_{OL2}	I_{OL2} = 6mA			0.6	
Low-Level Output Voltage (PSYNC, LSYNC)	V_{OL3}	I_{OL3} = 4mA			0.4	V
Low-Level Output Voltage (GA, GB)	V_{OL4}	I_{OL4} = 4mA			0.4	V
High-Level Output Voltage (PSYNC, LSYNC)	V_{OH1}	I_{OH1} = -1mA	V_{CC} - 0.4			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.5V to +5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High-Level Output Voltage (GA, GB)	V_{OH2}	I_{OH2} = -1mA	V_{CC} - 0.4			V
UVLO Threshold—V_{CC} Rising	V_{UVLOR}				4.3	V
UVLO Threshold—V_{CC} Falling	V_{UVLOF}		3.7			V
UVLO Hysteresis	V_{UVLOH}			100		mV
SVM Falling Edge Threshold	V_{SVMT}		1.95	2.0	2.05	V
SVM Hysteresis	V_{SVMH}			150		mV
LCM and OVD Source Current				4		µA
LCM and OVD Sink Current				4		µA
LCM and OVD DC Bias Voltage	V_{DCB}			1.35		V
LCM and OVD Input Resistance	R_{DCB}			50		kΩ
Lamp Off Threshold	V_{LOT}	(Note 3)	1.65	1.75	1.85	V
Lamp Overcurrent Threshold	V_{LOC}	(Note 3)	3.15	3.35	3.55	V
Lamp Regulation Threshold	V_{LRT}	(Note 3)	2.29	2.35	2.41	V
OVD Threshold	V_{OVDT}	(Note 3)	2.25	2.35	2.45	V
Lamp Frequency Range	$f_{LF:OSC}$		20		80	kHz
Lamp Frequency Source Frequency Tolerance	$f_{LFS:TOL}$	LOSC resistor ±0.1% over temperature	-2		+2	%
Lamp Frequency Receiver Duty Cycle	$f_{LFR:DUTY}$		40		60	%
DPWM Frequency Range	$f_{D:OSC}$		22.5		440.0	Hz
DPWM Source Frequency Tolerance	$f_{DSR:TOL}$	POSC resistor ±0.1% over temperature	-2		+2	%
DPWM Receiver Duty Cycle	$f_{DFE:DUTY}$		40		60	%
DPWM Receiver Frequency Range	$f_{DR:OSC}$		22.5		440.0	Hz
DPWM Receiver Minimum Pulse Width	$t_{DR:MIN}$	(Note 4)	25			µs
BRIGHT Voltage—Minimum Brightness	V_{BMIN}	Positive slope (CR2.7 = 0)			0.5	V
BRIGHT Voltage—Maximum Brightness	V_{BMAX}	Positive slope (CR2.7 = 0)	2.0			V
BRIGHT Voltage—Minimum Brightness	V_{BMIN}	Positive slope (CR2.7 = 1)			0	V
BRIGHT Voltage—Maximum Brightness	V_{BMAX}	Positive slope (CR2.7 = 1)	3.3			V
Gate-Driver Output Rise/Fall Time	t_R/t_F	C_L = 600pF		50	100	ns
GAn and GBn Duty Cycle		(Note 5)			44	%

4-Channel Cold-Cathode Fluorescent Lamp Controller

I²C AC ELECTRICAL CHARACTERISTICS (See Figure 10)

(V_{CC} = +4.5V to +5.5V, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 6)	0		400	kHz
Bus Free Time Between Stop and Start Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) Start Condition	$t_{HD:STA}$	(Note 7)	0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Start Setup Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 8)	$20 + 0.1C_B$		300	ns
SDA and SCL Fall Time	t_F	(Note 8)	$20 + 0.1C_B$		300	ns
Stop Setup Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 8)			400	pF
EEPROM Write Time	t_W	(Note 9)		20	30	ms

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycles		+70°C (Note 10)	50,000			Cycles

Note 1: All voltages are referenced to ground, unless otherwise noted. Currents into the IC are positive, out of the IC negative.

Note 2: During fault conditions, the AC-coupled feedback values are allowed to be outside the Absolute Maximum Rating of the LCM or OVD pin for up to 1 second.

Note 3: Voltage including the DC offset, V_{DCB}.

Note 4: This is the minimum pulse width guaranteed to generate an output burst, which will generate the DS3994's minimum burst duty cycle. This duty cycle may be greater than the duty cycle of the PSYNC input. Once the duty cycle of the PSYNC input is greater than the DS3994's minimum duty cycle, the output's duty cycle will track the PSYNC's duty cycle. Leaving PSYNC low (0% duty cycle) disables the GAn and GBn outputs in DPWM Slave mode.

Note 5: This is the maximum lamp frequency duty cycle that will be generated at any of the GAn or GBn outputs.

Note 6: I²C interface timing shown is for fast-mode (400kHz) operation. This device is also backward compatible with I²C standard-mode timing.

Note 7: After this period, the first clock pulse can be generated.

Note 8: C_B—total capacitance allowed on one bus line in picofarads.

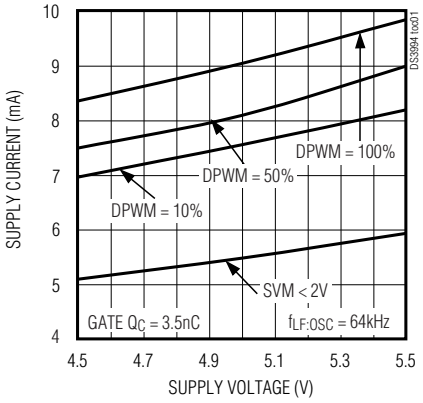
Note 9: EEPROM write begins after a stop condition occurs.

Note 10: Guaranteed by design.

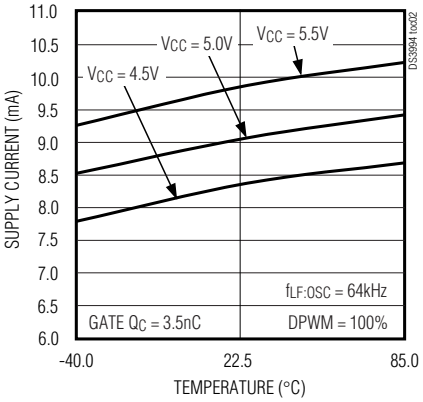
Typical Operating Characteristics

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.)

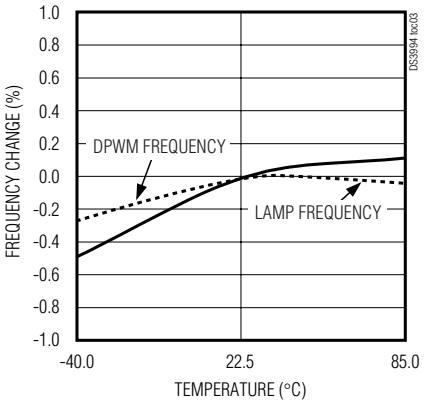
ACTIVE SUPPLY CURRENT vs. SUPPLY VOLTAGE



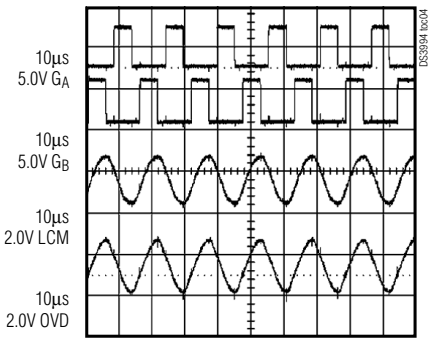
ACTIVE SUPPLY CURRENT vs. TEMPERATURE



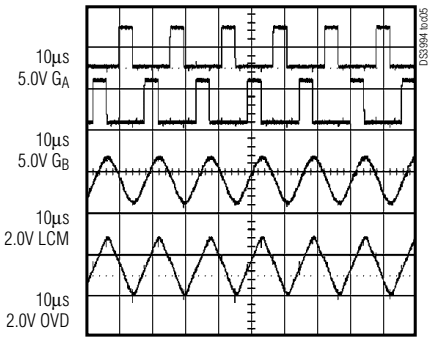
INTERNAL FREQUENCY CHANGE vs. TEMPERATURE



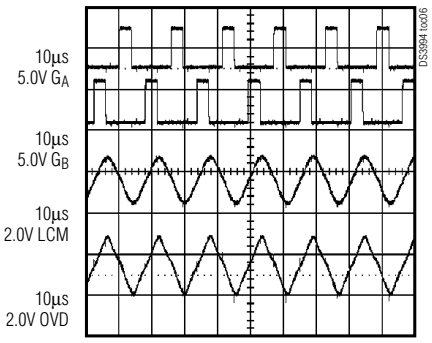
TYPICAL OPERATION AT 12V



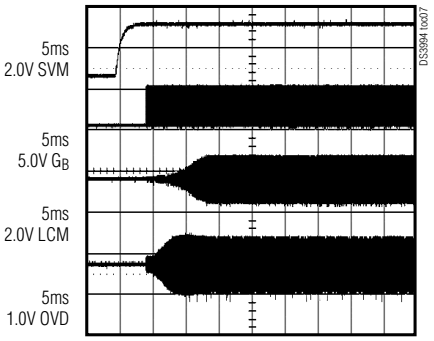
TYPICAL OPERATION AT 15V



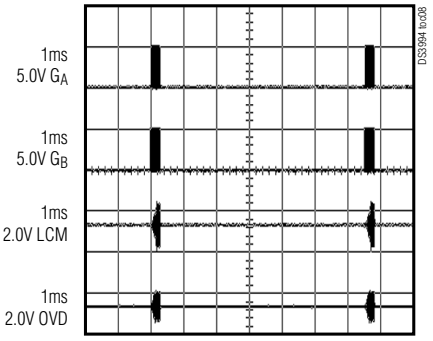
TYPICAL OPERATION AT 18V



TYPICAL STARTUP WITH SVM



BURST DIMMING AT 150Hz AND 10%

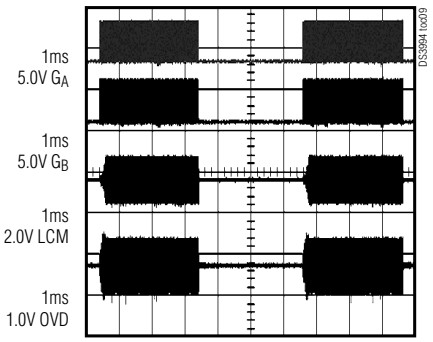


4-Channel Cold-Cathode Fluorescent Lamp Controller

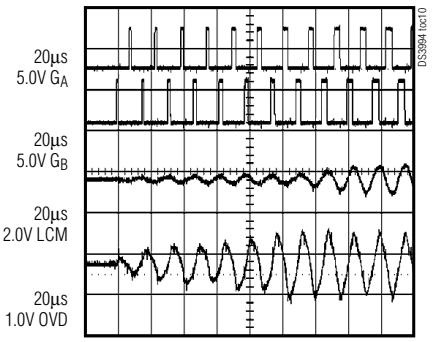
Typical Operating Characteristics (continued)

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.)

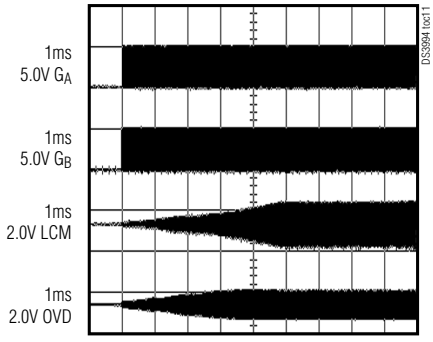
BURST DIMMING AT 150Hz AND 50%



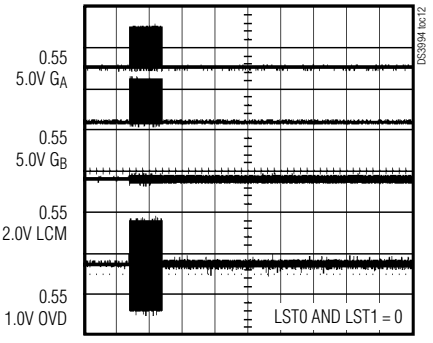
SOFT-START AT V_{INV} = 18V



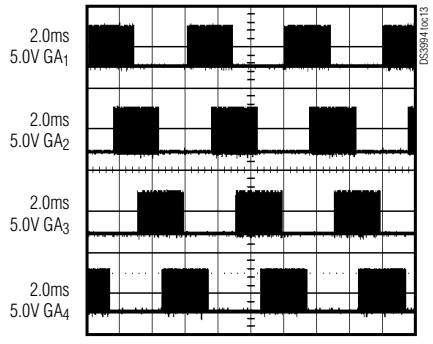
LAMP STRIKE—EXPANDED VIEW



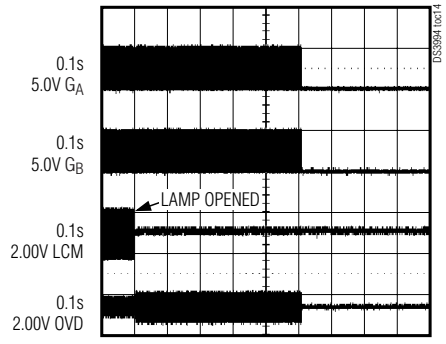
LAMP STRIKE WITH OPEN LAMP AUTORETRY DISABLED



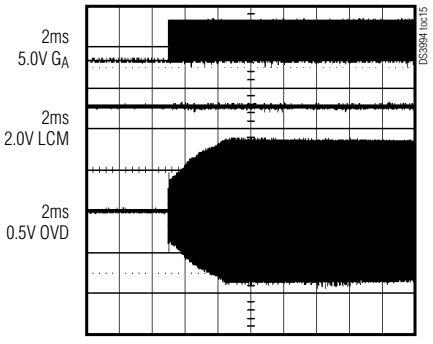
BURST DIMMING STAGGER



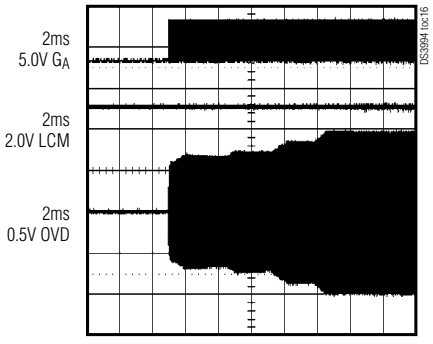
LAMP OUT (LAMP OPENED), AUTORETRY DISABLED



LAMP STRIKE WITH 0% FREQUENCY BOOST



LAMP STRIKE WITH 33% FREQUENCY BOOST



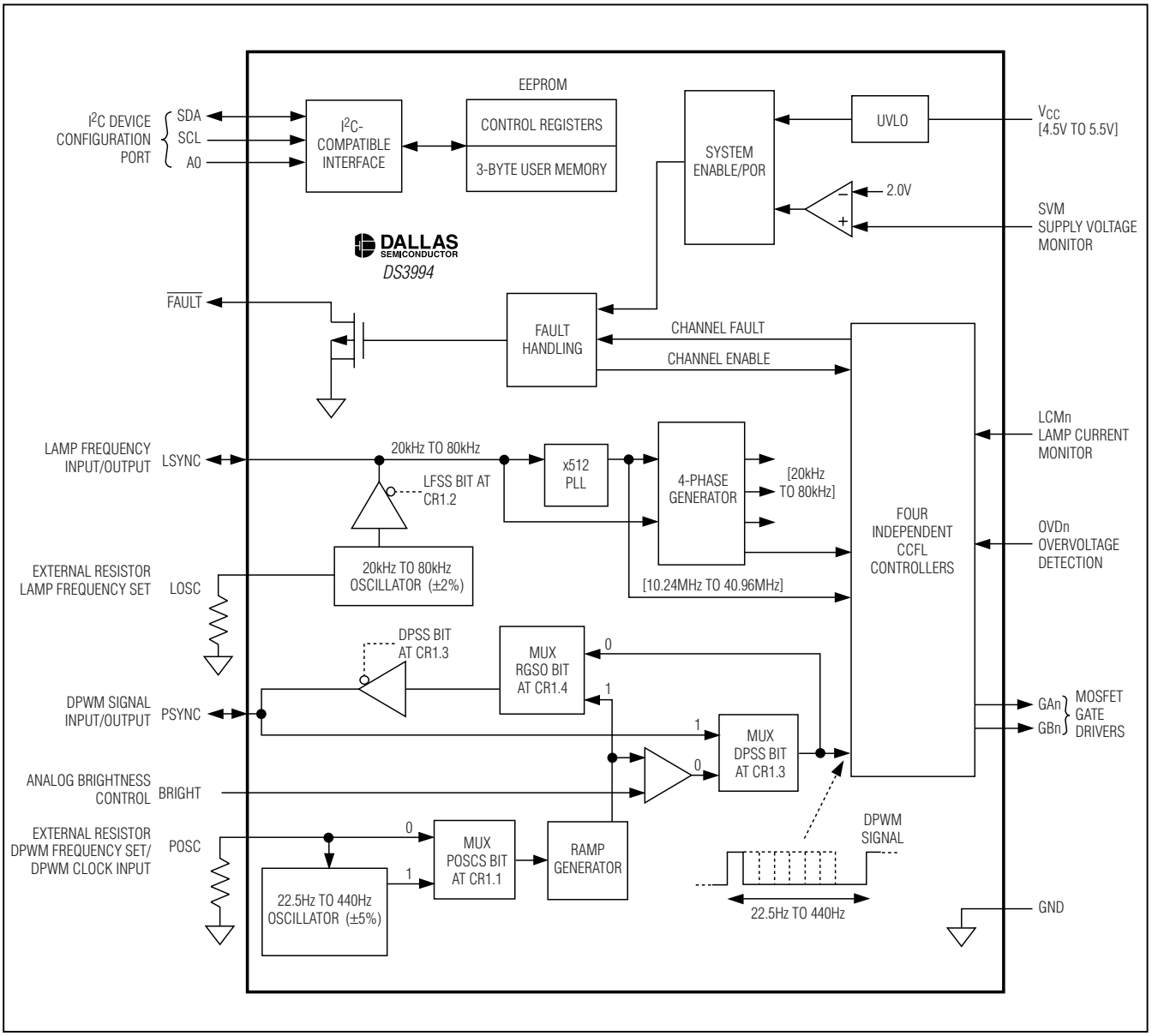
Pin Description

NAME	PINS BY CHANNEL (n = 1–4)				FUNCTION
	CH 1	CH 2	CH 3	CH 4	
GAn	7	11	17	21	MOSFET A Gate Drive. Connect directly to logic-level mode n-channel MOSFET. Leave open if channel is unused.
GBn	8	12	18	22	MOSFET B Gate Drive. Connect directly to logic-level mode n-channel MOSFET. Leave open if channel is unused.
LCMn	9	13	19	23	Lamp Current Monitor Input. Lamp current is monitored by measuring a voltage across a resistor placed in series with the low-voltage side of the lamp. Leave open if channel is unused.
OVDn	10	14	20	24	Overvoltage Detection. Lamp voltage is monitored through a capacitor-divider placed on the high-voltage side of the transformer. Leave open if channel is unused.

NAME	PIN	FUNCTION
GND	15	**Ground Connection**
V_{CC}	16	**Power-Supply Connection**
BRIGHT	5	**Analog Brightness Control Input.** Used to control DPWM dimming. Ground when using a PWM signal at PSYNC to control brightness.
SVM	6	**Supply Voltage Monitor Input.** Used to monitor the inverter voltage for undervoltage conditions.
SDA	25	**Serial Data Input/Output.** I^2C bidirectional data pin, which requires a pullup resistor to realize high logic levels.
SCL	26	**Serial Clock Input.** I^2C clock input.
$\overline{FAULT}$	27	**Fault Output.** This active-low, open-drain pin, requires an external pullup resistor to realize high logic levels.
LSYNC	28	**Lamp Frequency Input/Output.** This pin is the input for an externally sourced lamp frequency when the DS3994 is configured as a lamp frequency receiver. If the DS3994 is configured as a lamp frequency source (i.e., the lamp frequency is generated internally), the frequency is output on this pin for use by other lamp frequency receiver DS3994s.
LOSC	1	**Lamp Oscillator Resistor Adjust.** A resistor to ground on this pin sets the frequency of the lamp oscillator.
A0	2	**Address Select Input.** Determines the DS3994's I^2C slave address.
PSYNC	3	**DPWM Input/Output.** This pin is the input for an externally generated DPWM signal when the DS3994 is configured as a DPWM receiver. If the DS3994 is configured as a DPWM source (i.e., the DPWM signal is generated internally), the DPWM signal is output on this pin for use by other DPWM receiver DS3994s.
POSC	4	**DPWM Oscillator Resistor Adjust.** A resistor to ground on this lead sets the frequency of the DPWM oscillator (dimming clock). This lead can optionally accept a 22.5Hz to 440Hz clock as the source timing for the internal DPWM signal.

4-Channel Cold-Cathode Fluorescent Lamp Controller

Functional Diagram



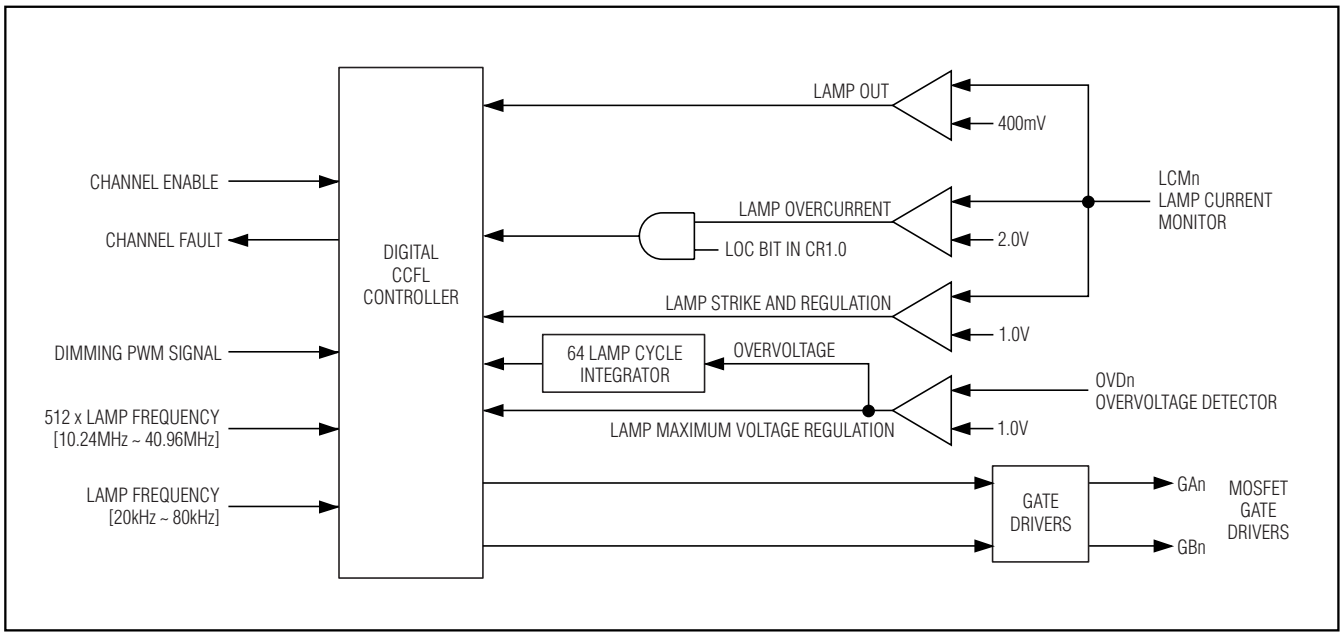


Figure 1. Per Channel Logic Diagram

Detailed Description

The DS3994 uses a push-pull drive scheme to convert a DC voltage (5V to 24V) to the high-voltage (600V_{RMS} to 1200V_{RMS}) AC waveform that is required to power the CCFLs. The push-pull drive scheme uses a minimal number of external components, which reduces assembly cost and makes the printed circuit board design easy to implement. The push-pull drive scheme also provides an efficient DC-to-AC conversion and produces near-sinusoidal waveforms.

Each DS3994 channel drives two logic-level n-channel MOSFETs that are connected between the ends of a step-up transformer and ground (see Figure 1 and the *Typical Operating Circuit*). The transformer has a center tap on the primary side that is connected to a DC voltage supply. The DS3994 alternately turns on the two MOSFETs to create the high-voltage AC waveform on the secondary side. By varying the duration of the MOSFET turn-on times, the controller is able to accurately control the amount of current flowing through the CCFL.

A resistor in series with the CCFL's ground connection enables current monitoring. The voltage across this resistor is fed to the lamp current monitor (LCM) input on the DS3994. The DS3994 compares the peak resistor voltage against an internal reference voltage to determine the duty cycle for the MOSFET gates. Each CCFL receives independent current monitoring and control, which results in equal brightness across all of the lamps and maximizes the lamp's brightness and lifetime.

The DS3994 can also drive more than one lamp per channel. See the *Typical Operating Circuit* section for implementation details when using multiple lamps per channel.

EEPROM Registers and I²C-Compatible Serial Interface

The DS3994 uses an I²C-compatible serial interface for communication with the on-board EEPROM configuration registers and user memory. The configuration registers, four Burst Dimming Stagger Registers (BDS1/2/3/4), and three Control Registers (CR1/2/3)—allow the user to customize many DS3994 parameters such as the time delay to stagger the burst dimming between channels, the lamp and dimming frequency sources, fault-monitoring options, and channel enabling/disabling. The three bytes of nonvolatile user memory can be used to store manufacturing data such as date codes, serial numbers, or product identification numbers.

The device is shipped from the factory with the configuration registers programmed to a set of default configuration parameters. To inquire about custom factory programming, please send an email to MixedSignal.Apps@dalsemi.com.

4-Channel Cold-Cathode Fluorescent Lamp Controller

Channel Phasing

The lamp-frequency MOSFET gate turn-on times are equally phased among the four channels during the burst period. This reduces the inrush current that would result from all lamps switching simultaneously, and hence eases the design requirements for the DC supply. Figure 2 details how the four channels are phased. Note that it is the lamp frequency signals that are phased, NOT the DPWM signals. See the *Burst Dimming Stagger Functionality* section for details or to adjust the DPWM signals of each channel.

Lamp Dimming Control (DPWM)

The DS3994 uses a digital pulse-width modulated (DPWM) signal (22.5Hz to 440Hz) to provide efficient and precise lamp dimming. During the high period of the DPWM cycle, the lamps are driven at the selected lamp frequency (20kHz to 80kHz) as shown in Figure 7. This part of the cycle is called the "burst" period because of the lamp frequency burst that occurs during this time. During the low period of the DPWM cycle, the controller disables the MOSFET gate drivers so the lamps are not driven. This causes the current to stop flowing in the lamps, but the time is short enough to keep the lamps from de-ionizing. Dimming is increased/decreased by adjusting (i.e., modulating) the duty cycle of the DPWM signal.

The DS3994 can generate its own DPWM signal internally (set DPSS = 0 in CR1), which can then be sourced to other DS3994s if required, or the DPWM signal can be supplied from an external source (set DPSS = 1 in CR1).

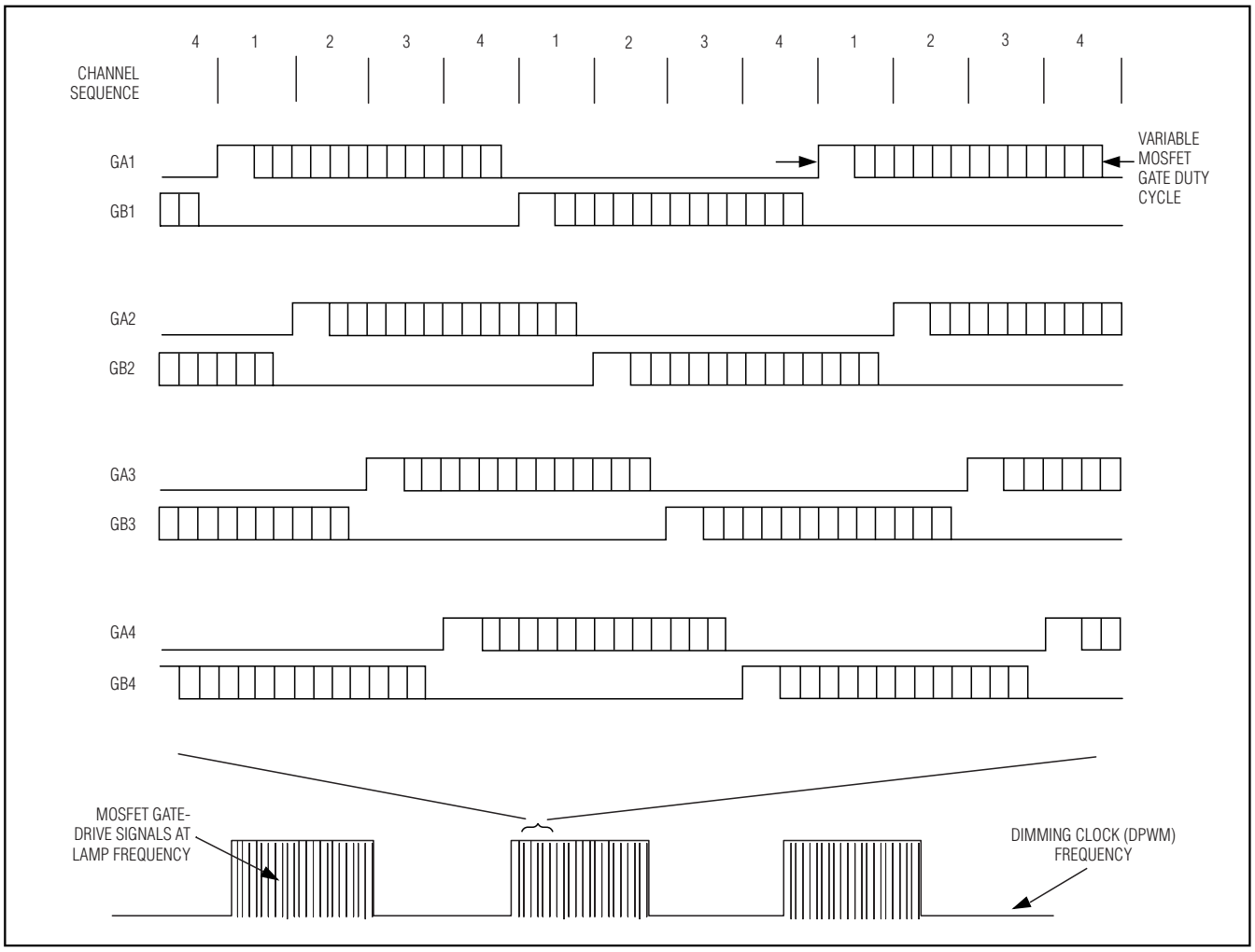


Figure 2. Channel Phasing Detail

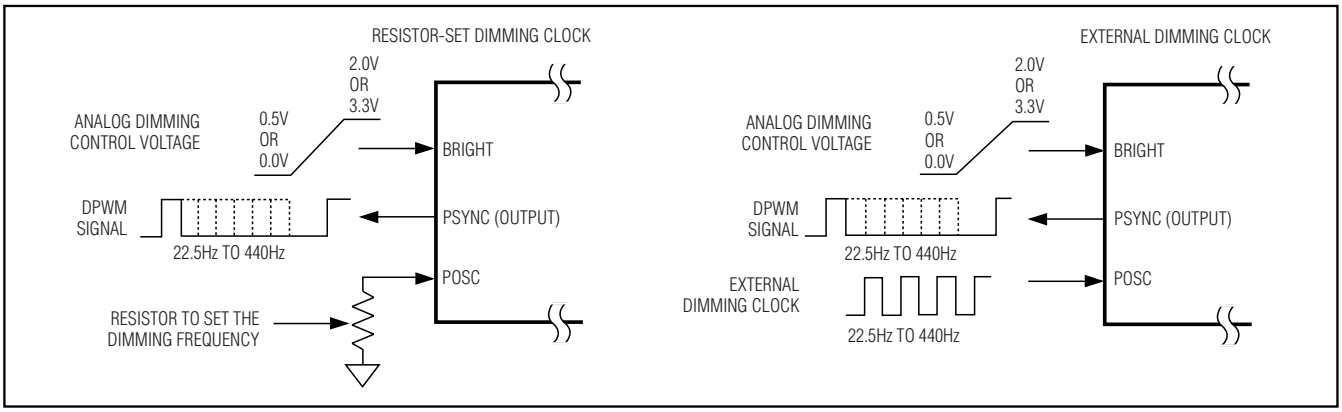


Figure 3. DPWM Source Configuration Options

Table 1. BRIGHT Analog Dimming Input Slope and Voltage Range Configuration

CR2.7	CR3.0	RANGE	SLOPE	MINIMUM BRIGHTNESS	MAXIMUM BRIGHTNESS
0	0	0.5 to 2V	Positive	0.5V	2.0V
0	1	0.5 to 2V	Negative	2.0V	0.5V
1	0	0 to 3.3V	Positive	0V	3.3V
1	1	0 to 3.3V	Negative	3.3V	0V

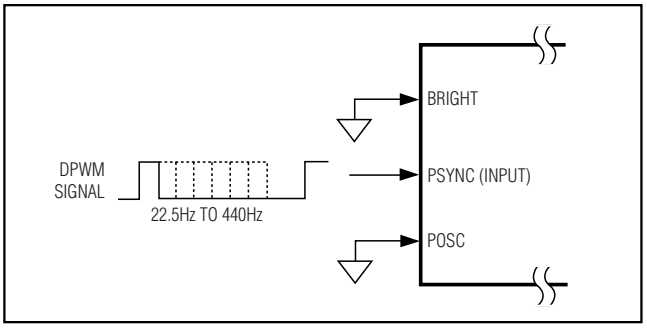


Figure 4. DPWM Receiver Configuration

To generate the DPWM signal internally, the DS3994 requires a clock (referred to as the dimming clock) to set the DPWM frequency. The user can supply the dimming clock by setting POSCS = 1 in CR1 and applying an external 22.5Hz to 440Hz signal at the POSC pin, or DS3994's clock can be generated by the DS3994's oscillator (set POSCS = 0 in CR1), in which case the frequency is set by an external resistor at the POSC pin. These two dimming clock options are shown in Figure 3. Regardless of whether the dimming clock is generated internally or sourced externally, the POSCR1 and POSCR2 bits in CR2 must be set to match the desired dimming clock frequency.

Lamp Dimming Control (DPWM)

When the DPWM signal is generated internally, its duty cycle (and, thus, the lamp brightness) is controlled by a user-applied analog voltage at the BRIGHT input. Users can select a positive or negative slope for the bright pin's dimming input as well as the voltage range. If SLOPE = 0 in CR3, then the slope is positive. This means that a BRIGHT voltage less than the minimum voltage causes the DS3994 to operate with the minimum burst duty cycle, providing the lowest brightness setting, while any voltage greater than the maximum voltage causes a 100% burst duty cycle (i.e., lamps always being driven), which provides the maximum brightness. For voltages between the minimum voltage and the maximum voltage, the duty cycle varies linearly between the minimum and 100%.

The internally generated DPWM signal is available at the PSYNC I/O pin (set RGSO = 0 in CR1) for sourcing to other DS3994s, if any, in the circuit. This allows all DS3994s in the system to be synchronized to the same DPWM signal. The DS3994 that is generating the DPWM signal for other DS3994s in the system is referred to as the DPWM source.

4-Channel Cold-Cathode Fluorescent Lamp Controller

When the DPWM signal is provided by an external source, either from the PSYNC pin of another DS3994 or from some other user-generated source, it is input into the PSYNC I/O pin of the DS3994. In this mode, the BRIGHT and POSC inputs are disabled and should be grounded (see Figure 4). When multiple DS3994s are used in a design, DS3994s configured to use externally generated DPWM signals are referred to as DPWM receivers.

Burst Dimming Stagger (BDS) Functionality

The DS3994 also features burst dimming stagger (BDS) functionality integrated into the burst dimming controller. BDS is useful to reduce the current ripple on the DC supply as well as improve the visual motion response of the LCD panel. This feature allows users to enter a digital code into each channel independent register (BDS1/2/3/4) that would delay the start of each burst period. The 8-bit BDS code can be calculated by using Table 2 and the following equations.

Table 2. Multiplication Factor M, Based on Lamp Frequency Oscillator and DPWM Frequency Oscillator

POSCR1 (CR2.2)	POSCR0 (CR2.1)	SELECTED PWM OSCILLATOR RANGE (Hz)	M, LAMP CYCLE PERIOD MULTIPLICATION FACTOR	
			LAMP OSCILLATOR = 40 TO 80kHz (LOFS = 0)	LAMP OSCILLATOR = 20 TO 40kHz (LOFS = 1)
0	0	22.5 to 55	8	8
0	1	45 to 110	4	4
1	0	90 to 220	2	2
1	1	180 to 440	1	1

$$BDS\_Resolution = \frac{M}{f_{LF:OSC}}$$

$$BDS\_Delay = BDS\_Resolution \times BDS\_8\text{-}Bit\_Value$$

If a BDS_Delay is used that is longer than the burst period, then the gate drivers, GA and GB, have no output.

For example, assume a lamp frequency of 50kHz and a burst frequency of 167Hz. The step resolution of the burst-dimming stagger would be 40µs (2/50,000). To achieve equal stagger, as shown in Figure 5, the BDS1/2/3/4 registers would be programmed as described in Table 3.

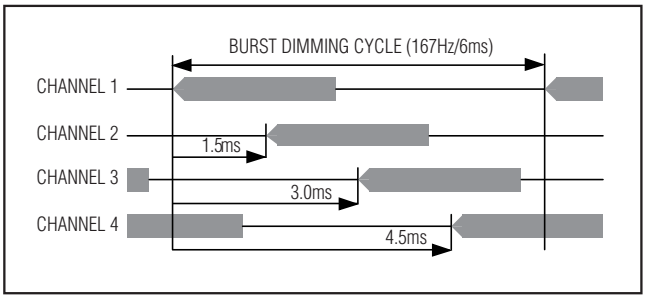


Figure 5. Example Burst Dimming Stagger Cycle

Table 3. Example BDS1/2/3/4 Programmed Values

CHANNEL	REGISTER	DESIRED STAGGER (ms)	STEP RESOLUTION (µs)	COUNT	PROGRAMMED VALUE
1	BDS1	0	40	0	00h
2	BDS2	1.5	40	38	26h
3	BDS3	3.0	40	75	48h
4	BDS4	4.5	40	113	71h

Lamp Strike Frequency Boost

The DS3994 also features a programmable lamp strike frequency boost option. During the strike period, the transformer secondary is essentially unloaded. The lamp frequency be can be easily increased causing a higher strike voltage. The SB0/1/2 bits in CR3 control how the frequency is increased during lamp strike. A setting of 000b results in no frequency increase, while the maximum setting (111b) causes a 100% increase. Once the DS3994 detects that the lamp has struck, the lamp frequency is automatically reset to the nominal run level.

Lamp Frequency Configuration

The DS3994 can generate its own lamp frequency clock internally (set LFSS = 0 in CR1), which can then be sourced to other DS3994s if required, or the lamp clock can be supplied from an external source (set LFSS = 1 in CR1). When the lamp clock is internally generated, the frequency (20kHz to 80kHz) is set by an external resistor at the LOSC. In this case, the DS3994 can act as a lamp frequency source because the lamp clock is output at the LSYNC I/O pin for synchronizing any other DS3994s configured as lamp frequency receivers.

The DS3994 acts as a lamp frequency receiver when the lamp clock is supplied externally. In this case, a 20kHz to 80kHz clock must be supplied at the LSYNC I/O. The external clock can originate from the LSYNC I/O of a DS3994 configured as a lamp frequency source or from some other source.

The LOFS bit in CR3 must be set to match the appropriate lamp frequency range. If a 20kHz to 40kHz frequency is used, then LOFS must be set to 1; if a 40kHz to 80kHz frequency is used, then LOFS must be set to 0.

Configuring Systems with Multiple DS3994s

The source and receiver options for the lamp frequency clock and DPWM signal allow multiple DS3994s to be synchronized in systems requiring more than four lamps. The lamp and dimming clocks can either be generated on board the DS3994 using external resistors to set the frequency, or they can be sourced by the host system to synchronize the DS3994 to other system resources. Figure 6 shows various multiple DS3994 configurations that allow both lamp and/or DPWM synchronization for all DS3994s in the system.

DPWM Soft-Start

At the beginning of each lamp burst, the DS3994 provides a soft-start that slowly increases the MOSFET gate-driver duty cycle (see Figure 7). This minimizes the possibility of audible transformer noise that could result from current surges in the transformer primary. The soft-start length is fixed at 16 lamp cycles.

4-Channel Cold-Cathode Fluorescent Lamp Controller

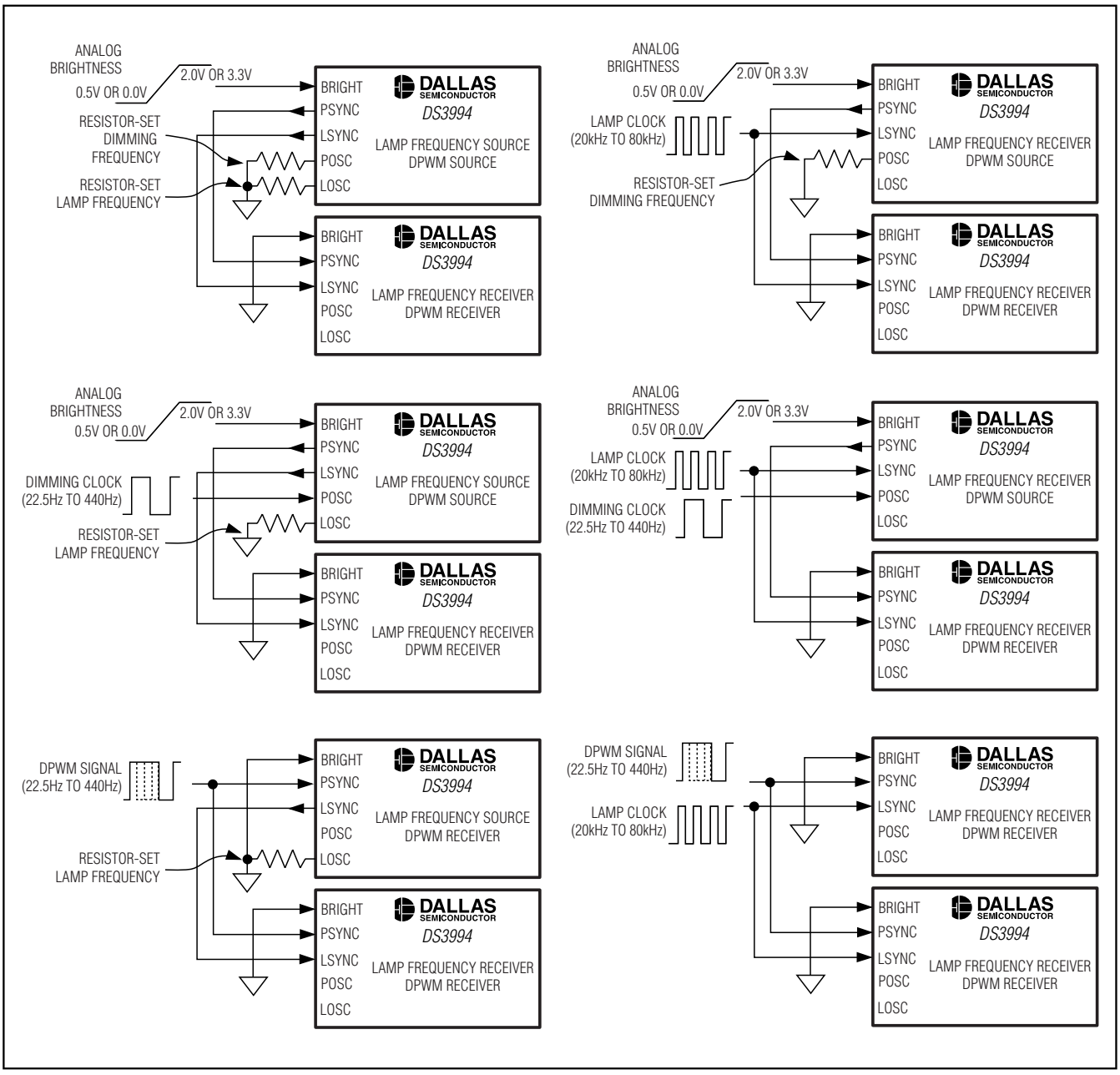


Figure 6. Frequency Configuration Options for Designs Using Multiple DS3994s

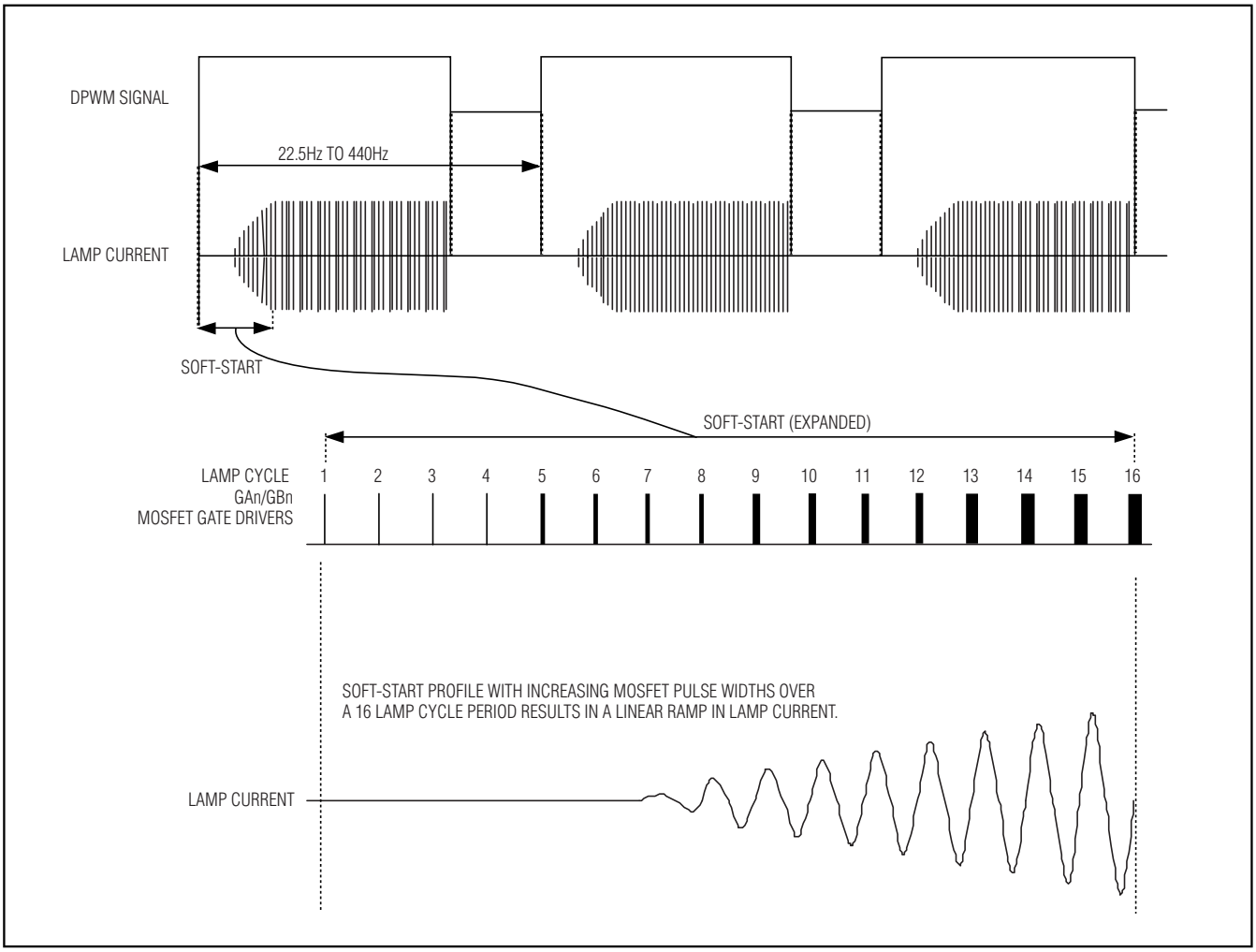


Figure 7. Digital PWM Dimming and Soft-Start

4-Channel Cold-Cathode Fluorescent Lamp Controller

Setting the Lamp and Dimming Clock (DPWM) Frequencies Using External Resistors

Both the lamp and dimming clock frequencies can be set using external resistors. The resistance required for either frequency can be determined using the following formula:

$$R_{OSC} = \frac{K}{f_{OSC}}$$

where K = 1600kΩ•kHz for lamp frequency calculations. When calculating the resistor value for the dimming clock frequency, K will be one of four values as determined by the desired frequency and the POSCR0 and POSCR1 bit settings as shown in the Control Register 2 (CR2) in the *Detailed Register Descriptions* section.

Example: Selecting the resistor values to configure a DS3994 to have a 50kHz lamp frequency and a 160Hz dimming clock frequency:

For this configuration, POSCR0 and POSCR1 must be programmed to 1 and 0, respectively, to select 90Hz to 220Hz as the dimming clock frequency range. This sets K for the dimming clock resistor (R_{POSC}) calculation to 4kΩ•kHz. For the lamp frequency resistor (R_{LOSC}) calculation, K = 1600kΩ•kHz, which allows the lamp frequency K value regardless of the frequency. The formula above can now be used to calculate the resistor values for R_{LOSC} and R_{POSC} as follows:

$$R_{LOSC} = \frac{1600k\Omega \bullet kHz}{50kHz} = 32k\Omega,$$

$$R_{POSC} = \frac{4k\Omega \bullet kHz}{0.160kHz} = 25.0k\Omega$$

Supply Monitoring

The DS3994 monitors both the transformer's DC supply and its own V_{CC} supply to ensure that both voltage levels are adequate for proper operation.

The inverter's transformer supply (V_{INV}) is monitored using an external resistor-divider that is the input into a comparator (see Figure 8) with a 2V threshold. Using the equation below to determine the resistor values, the supply voltage monitor (SVM) trip point (V_{TRIP}) can be customized to shut off the inverter when the transformer's input voltage drops below any specified value. Operating with the transformer's supply at too low of a level can prevent the inverter from reaching the strike voltage and could potentially cause numerous other problems. Proper use of the SVM can prevent these problems. If desired, the SVM can be disabled by connecting the SVM pin to V_{CC}.

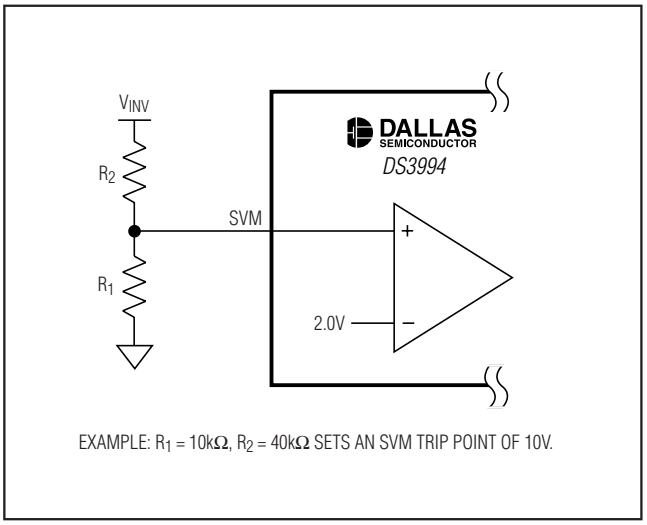


Figure 8. Setting the SVM Threshold Voltage

$$V_{TRIP} = 2.0\left(\frac{R_1 + R_2}{R_1}\right)$$

The V_{CC} monitor is used as a 5V supply undervoltage lockout (UVLO) that prevents operation when the DS3994 does not have adequate voltage for its analog circuitry to operate or to drive the external MOSFETs. The V_{CC} monitor features hysteresis to prevent V_{CC} noise from causing spurious operation when V_{CC} is near the trip point. This monitor cannot be disabled by any means.

Fault Monitoring

The DS3994 provides extensive fault monitoring for each channel. It can detect open-lamp, lamp overcurrent, failure to strike, and overvoltage conditions. The DS3994 can be configured to disable all channels if one or more channels enter a Fault State, or it can be configured to disable only the channel where the fault occurred. Once a Fault State has been entered, the $\overline{FAULT}$ output is asserted and the channel(s) remain disabled until either the DS3994 is power-cycled or the inverter's DC supply is power-cycled. The DS3994 can also be configured to automatically attempt to clear a detected fault (except lamp overcurrent) by restriking the lamp, as explained in Step 4. Configuration bits for the fault monitoring options are located in the control registers.

Figure 9 shows a flowchart of how the DS3994 controls and monitors each lamp. The steps are as follows:

1) Supply Check—The lamps will not turn on unless the DS3994 supply voltage is ≥ 4.5V and the voltage at the supply voltage monitor (SVM) input is ≥ 2V.
2) Strike Lamp—When both the DS3994 and the DC inverter supplies are above these minimum values, the DS3994 attempts to strike each enabled channel. The DS3994 slowly ramps up the MOSFET gate duty cycle until the lamp strikes. The controller detects that the lamp has struck by detecting current flow in the lamp. If during the strike ramp the maximum allowable voltage is reached, the controller stops increasing the MOSFET gate duty cycle to keep from overstressing the system. The DS3994 goes into a fault handling state (step 4) if the lamp has not struck after the timeout period as defined by the LST0 and LST1 control bits in the CR3 register. If an overvoltage event is detected during the strike attempt, the DS3994 disables the MOSFET gate drivers and goes into the fault handling state.
3) Run Lamp—Once the lamp is struck, the DS3994 moves to the Run Lamp stage. In the Run Lamp stage, the DS3994 adjusts the MOSFET gate duty cycle to optimize the lamp current. The gate duty cycle is always constrained to keep the system from exceeding the maximum allowable lamp voltage. If lamp current ever drops below the Lamp Out reference point for the period as defined by the LST0 and LST1 control bits in the CR3 register, then the lamp is considered extinguished. In this case the MOSFET gate drivers are disabled and the device moves to the fault handling stage.
4) Fault Handling—During fault handling, the DS3994 performs an optional (user-selectable) automatic retry to attempt to clear all faults except a lamp overcurrent. The automatic retry makes 14 additional attempts to rectify the fault before declaring the channel in a Fault State and permanently disabling the channel. Between each of the 14 attempts, the controller waits 1024 lamp cycles. In the case of a lamp overcurrent, the DS3994 instantaneously declares the channel to be in a Fault State and permanently disables the channel. The DS3994 can be configured to disable all channels if one or more channels enters a Fault State or it can be configured to disable only the channel where the fault occurred. Once a Fault State is entered, the channel remains in that state until one of the following occurs:
   - V_{CC} drops below the UVLO threshold.
   - The SVM threshold is crossed.
   - The channel is disabled.

4-Channel Cold-Cathode Fluorescent Lamp Controller

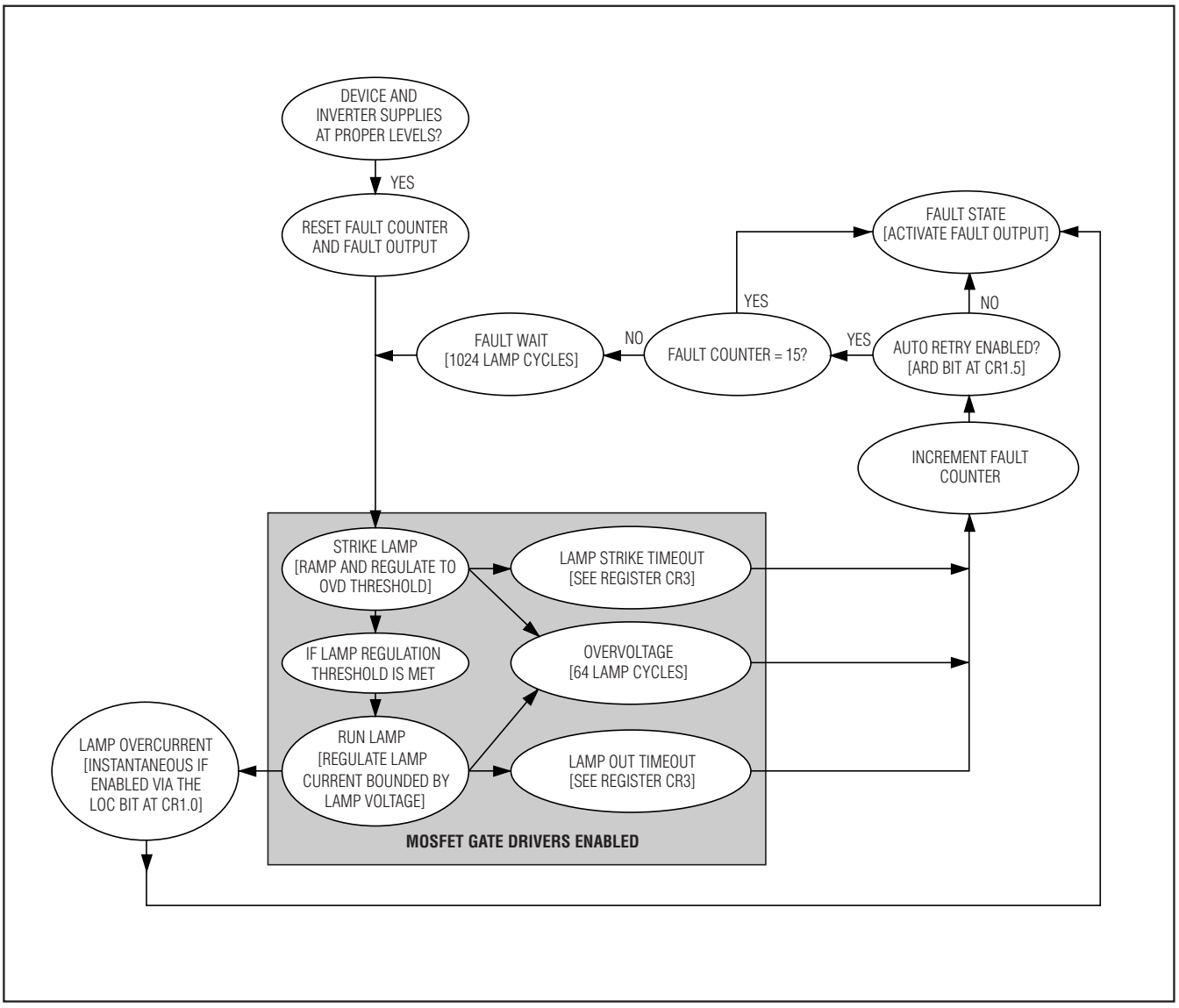


Figure 9. Fault-Handling Flow Chart

Detailed Register Descriptions

The DS3994's register map is shown in Table 4. Detailed register and bit descriptions follow in the subsequent tables.

Table 4. Register Map

BYTE ADDRESS	BYTE NAME	FACTORY DEFAULT*	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F0h	Reserved	21h	—				—			
F1h	Reserved	43h	—				—			
F2h	Reserved	65h	—				—			
F3h	Reserved	77h	—				—			
F4h	CR1	20h	DPD	FRS	ARD	RGSO	DPSS	LFSS	POSCS	LOC
F5h	CR2	08h	BVRS	LD1	LD0	0	1	POSCR1	POSCR0	UMWP
F6h	Reserved	00h	—	—	—	—	—	—	—	—
F7h	Reserved	00h	—	—	—	—	—	—	—	—
F8h	BDS1	00h	Burst dimming stagger for channel 1.							
F9h	BDS2	00h	Burst dimming stagger for channel 2.							
FAh	BDS3	00h	Burst dimming stagger for channel 3.							
FBh	BDS4	00h	Burst dimming stagger for channel 4.							
FCh	CR3	00h	LOFS	IGO	SB2	SB1	SB0	LST1	LST0	SLOPE
FD-FFh	User Memory	00h	EE	EE	EE	EE	EE	EE	EE	EE

**This is the factory-programmed default stored in EEPROM.*

4-Channel Cold-Cathode Fluorescent Lamp Controller

F4h: Control Register 1 (CR1)

BIT	NAME	FUNCTION
0	LOC	Lamp Overcurrent 0 = Lamp overcurrent detection disabled. 1 = Lamp overcurrent detection enabled.
1	POSCS	POSC Select. See POSCR0 and POSCR1 bits in Control Register 2 to select the oscillator range. 0 = Connect POSC to ground with a resistor to set the dimming frequency. 1 = Connect POSC to an external 22.5Hz to 440Hz dimming clock to set the dimming frequency.
2	LFSS	Lamp Frequency Source Select 0 = Lamp frequency source mode. The lamp frequency is generated internally and sourced at the LSYNC output for use by lamp frequency receivers. 1 = Lamp frequency receiver mode. The lamp frequency must be provided at the LSYNC input.
3	DPSS	DPWM Signal Source Select 0 = DPWM source mode. DPWM signal is generated internally, and can be output at PSYNC pin (see RGSO bit). 1 = DPWM receiver mode. DPWM signal is generated externally and supplied at the PSYNC input.
4	RGSO	Ramp Generator Source Option 0 = Sources DPWM at the PSYNC output. 1 = Sources the internal ramp generator at PSYNC output.
5	ARD	Autoretry Disable 0 = Autoretry function enabled. 1 = Autoretry function disabled.
6	FRS	Fault Response Select 0 = Disable only the malfunctioning channel. 1 = Disable all channels upon fault detection at any channel.
7	DPD	DPWM Disable 0 = DPWM function enabled. 1 = DPWM function disabled. DPWM set to 100% duty cycle.

F5h: Control Register 2 (CR2)

BIT	NAME	FUNCTION
0	UMWP	User Memory Write Protect 0 = User Memory Write Access Blocked 1 = User Memory Write Access Permitted
1	POSCR0	DPWM Oscillator Range Select. When using an external source for the dimming clock, these bits must be set to match the external oscillator's frequency. When using a resistor to set the dimming frequency, these bits plus the external resistor control the frequency.
2	POSCR1	See table below

POSCR1	POSCR0	DIMMING CLOCK (DPWM) FREQUENCY RANGE (Hz)	K (kΩ-kHz)
0	0	22.5 to 55.0	1
0	1	45 to 110	2
1	0	90 to 220	4
1	1	180 to 440	8

3	Reserved	Reserved. Should be set to one.
4	Reserved	Reserved. Should be set to zero.
5	LD0	Lamp Disable. Used to disable channels if all 4 are not required for an application.
6	LD1	See table below
7	BVRS	Bright Voltage Range Select. 0 = 0.5V to 2.0V 1 = 0.0V to 3.3V

LD1	LD0	CHANNELS DISABLED	NUMBER OF ACTIVE LAMP CHANNELS
0	0	All Channels Enabled	4
0	1	4	3
1	0	2/4	2
1	1	1/2/4	1

F8–FBh: Burst Dimming Stagger (BDS1/2/3/4)

BIT	NAME	FUNCTION
0	BDSC0	8-Bit Programmable Counter That Staggers the Start of Burst Dimming. 00h = 0ms stagger. Setting the stagger longer than the burst dimming cycle results in the channel never turning on. See Table 2.
1	BDSC1	
2	BDSC2	
3	BDSC3	
4	BDSC4	
5	BDSC5	
6	BDSC6	
7	BDSC7	

4-Channel Cold-Cathode Fluorescent Lamp Controller

FCh: Control Register 3 (CR3)

BIT	NAME	FUNCTION				
0	SLOPE	BRIGHT Analog Dimming Slope Select 0 = Positive Slope 1 = Negative Slope				
1	LST0	LST1	LST0	STRIKE AND LAMP OUT TIMEOUT IN LAMP FREQUENCY CYCLES		EXAMPLE TIME OUT IF LAMP FREQUENCY IS 25kHz OR 50kHz
				LAMP OSCILLATOR = 40kHz TO 80kHz (LOFS = 0)	LAMP OSCILLATOR = 20kHz TO 40kHz (LOFS = 1)	
		0	0	32,768	16,384	0.66 seconds
		0	1	65,536	32,768	1.31 seconds
2	LST1	1	0	98,304	49,152	1.97 seconds
		1	1	131,072	65,536	2.62 seconds
Note: The strike frequency boost does not affect this timeout.						
3	SB0	LAMP STRIKE FREQUENCY BOOST SELECT				
		SB2	SB1	SB0	LAMP STRIKE FREQUENCY BOOST	EXAMPLE STRIKE FREQUENCY IF LAMP FREQUENCY IS 50kHz
		0	0	0	0%	50kHz
4	SB1	0	0	1	14%	57kHz
		0	1	0	23%	61.5kHz
		0	1	1	33%	66.7kHz
		1	0	0	46%	73kHz
5	SB2	1	0	1	60%	80kHz
		1	1	0	78%	89kHz
		1	1	1	100%	100kHz
6	IGO	Invert MOSFET Gate A and Gate B Driver Outputs 0 = Do not invert GA and GB outputs. 1 = Invert GA and GB outputs.				
7	LOFS	Lamp Oscillator Frequency Select 0 = 40kHz to 80kHz 1 = 20kHz to 40kHz				

I²C Definitions

The following terminology is commonly used to describe I²C data transfers.

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses, start, and stop conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between stop and start conditions when both SDA and SCL are inactive and in their logic-high states.

Start Condition: A start condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a start condition. See the timing diagram for applicable timing.

Stop Condition: A stop condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a stop condition. See the timing diagram for applicable timing.

Repeated Start Condition: The master can use a repeated start condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated starts are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated start condition is issued identically to a normal start condition. See the timing diagram for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements (see Figure 10). Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time (see Figure 10) before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An acknowledgement (ACK) or not acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing (Figure 10) for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

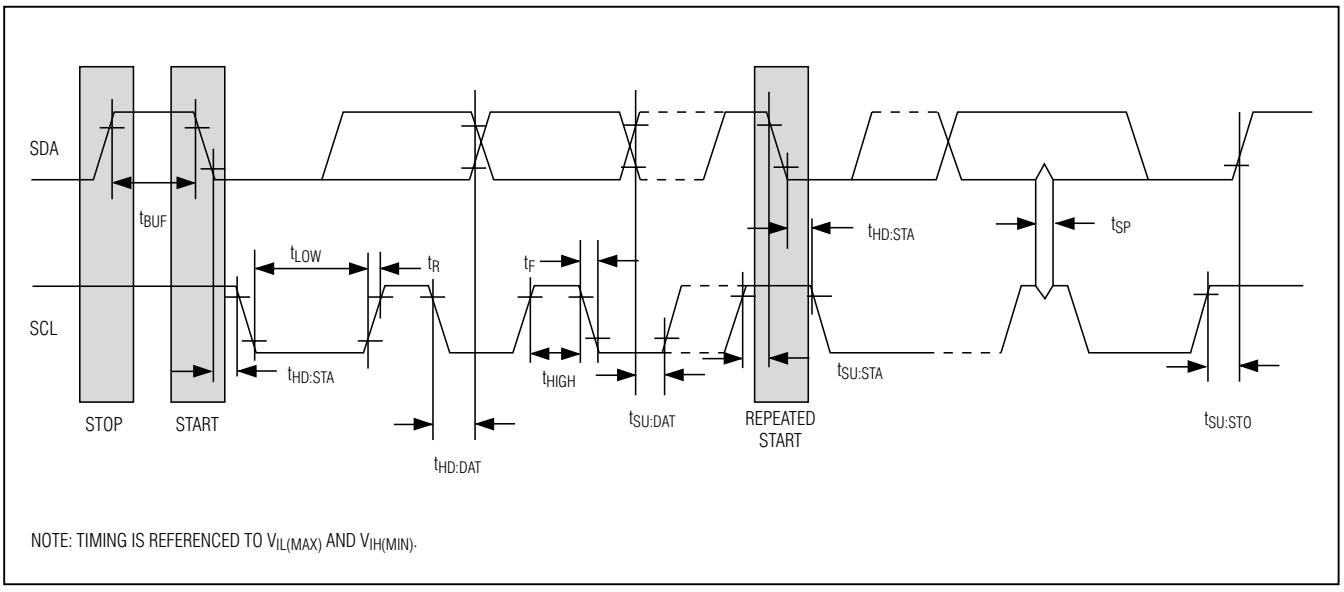


Figure 10. I²C Timing Diagram

4-Channel Cold-Cathode Fluorescent Lamp Controller

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit-write definition and the acknowledgement is read using the bit-read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave will return control of SDA to the master.

Slave Address Byte: Each slave on the I²C bus responds to a slave addressing byte sent immediately following a start condition. The slave address byte (Figure 11) contains the slave address in the most significant seven bits and the R/$\overline{W}$ bit in the least significant bit.

The DS3994's slave address is 101000A_0 (binary), where A_0 is the value of the address pin (A_0). The address pin allows the device to respond to one of two possible slave addresses. By writing the correct slave address with R/$\overline{W}$ = 0, the master writes data to the slave. If R/$\overline{W}$ = 1, the master reads data from the slave. If an incorrect slave address is written, the DS3994 will assume the master is communicating with another I²C device and ignore the communications until the next start condition is sent.

Memory Address: During an I²C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

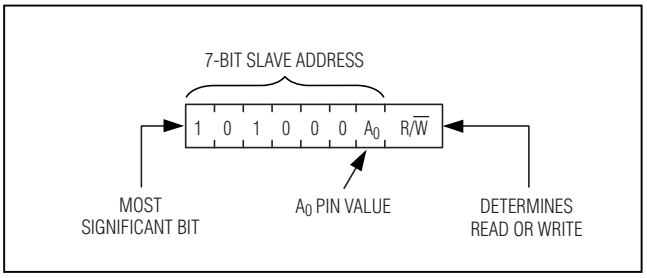


Figure 11. DS3994's Slave Address Byte

I²C Communication

Writing a Data Byte to a Slave: The master must generate a start condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a stop condition. Remember the master must read the slave's acknowledgement during all byte write operations. See Figure 12 for more detail.

Acknowledge Polling: Any time EEPROM is written, the DS3994 requires the EEPROM write time (t_W) after the stop condition to write the contents to EEPROM. During the EEPROM write time, the DS3994 will not acknowledge its slave address because it is busy. It is possible to take advantage of that phenomenon by repeatedly addressing the DS3994, which allows the next byte of data to be written as soon as the DS3994 is ready to receive the data. The alternative to acknowledge polling is to wait for a maximum period of t_W to elapse before attempting to write again to the DS3994.

EEPROM Write Cycles: The number of times the DS3994's EEPROM can be written before it fails is specified in the *Nonvolatile Memory Characteristics* table. This specification is shown at the worst-case write temperature. The DS3994 is typically capable of handling many additional write cycles when the writes are performed at room temperature.

Reading a Data Byte from a Slave: To read a single byte from the slave the master generates a start condition, writes the slave address byte with R/$\overline{W}$ = 0, writes the memory address, generates a repeated start condition, writes the slave address with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a stop condition. See Figure 12 for more detail.

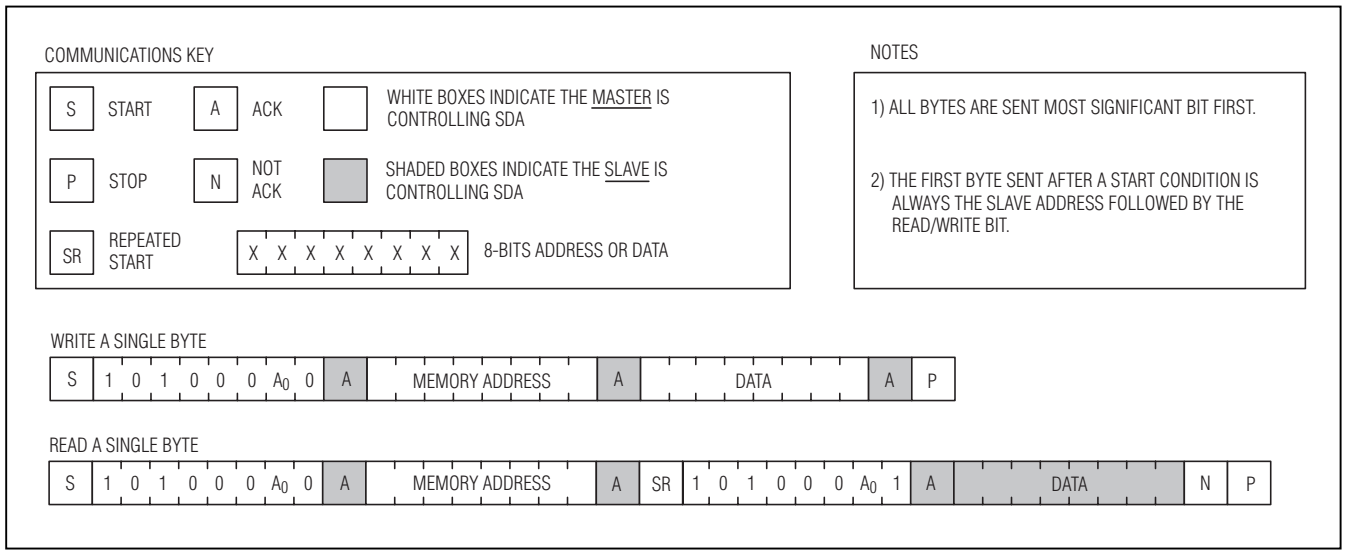


Figure 12. I²C Communications Examples

Applications Information

Addressing Multiple DS3994s On a Common I²C Bus

Each DS3994 responds to one of two possible slave addresses based on the state of the address input (A_0). For information about device addressing see the *I²C Communications* section.

Power-Supply Decoupling

To achieve best results, it is recommended that each V_{CC} pin is decoupled with a 0.01µF or a 0.1µF capacitor to GND. Use high-quality, ceramic, surface-mount capacitors, and mount the capacitors as close as possible to the V_{CC} and GND pins to minimize trace inductance.

Setting the RMS Lamp Current

Resistor R8 in the typical operating circuit (Figure 13) sets the lamp current. R8 = 140Ω corresponds to a $5mA_{RMS}$ lamp current as long as the current waveform is approximately sinusoidal. The formula to determine the resistor value for a given sinusoidal lamp current is:

$$R8 = \frac{1}{\sqrt{2} \times I_{LAMP(RMS)}}$$

Component Selection

External component selection has a large impact on the overall system performance and cost. The two most important external components are the transformers and n-channel MOSFETs.

The transformer should be able to operate in the 20kHz to 80kHz frequency range of the DS3994, and the turns ratio should be selected so the MOSFET drivers run at 28% to 35% duty cycle during steady state operation. The transformer must be able to withstand the high open-circuit voltage that will be used to strike the lamp. Additionally, its primary/secondary resistance and inductance characteristics must be considered because they contribute significantly to determining the efficiency and transient response of the system. Table 5 shows a transformer specification that has been utilized for a 12V inverter supply, 438mm x 2.2mm lamp design.

The n-channel MOSFET must have a threshold voltage that is low enough to work with logic-level signals, a low on-resistance to maximize efficiency and limit the n-channel MOSFET's power dissipation, and a breakdown voltage high enough to handle the transient. The breakdown voltage should be a minimum of 3x the inverter voltage supply. Additionally, the total gate charge must be less than Q_G, which is specified in the *Recommended DC Operating Conditions* table. These specifications are easily met by many of the dual n-channel MOSFETs now available in SO-8 packages.

Table 6 lists suggested values for the external resistors and capacitors used in the typical operating circuit.

4-Channel Cold-Cathode Fluorescent Lamp Controller

Table 5. Transformer Specifications

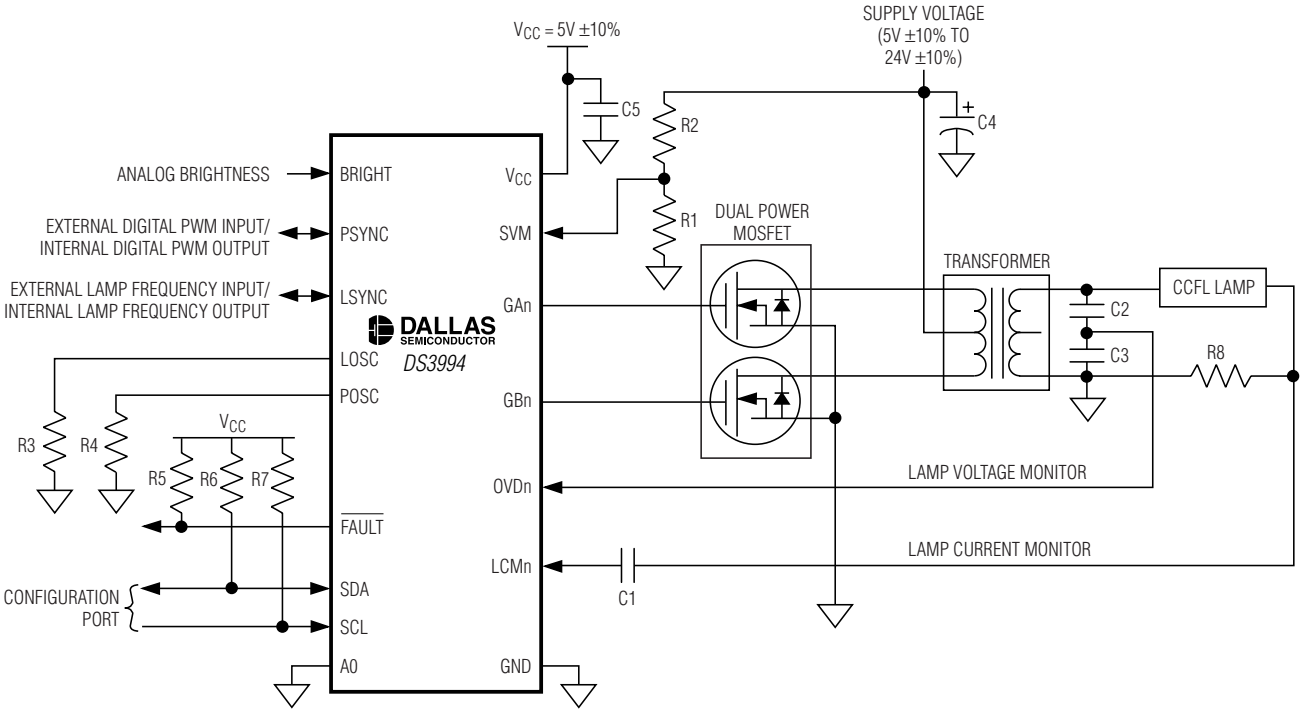
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Turns Ratio (Secondary/Primary)	(Notes 1, 2, 3)		40		
Frequency		40		80	kHz
Output Power				6	W
Output Current			5	8	mA
Primary DCR	Center tap to one end		200		mΩ
Secondary DCR			500		Ω
Primary Leakage			12		µH
Secondary Leakage			185		mH
Primary Inductance			70		µH
Secondary Inductance			500		mH
Center Tap Voltage		10.8	12	13.2	V
Secondary Output Voltage	100ms minimum	2000			V_{RMS}
	Continuous	1000			

Note 1: Primary should be Bifilar wound with center tap connection.
Note 2: Turns ratio is defined as secondary winding divided by the sum of both primary windings.
Note 3: 40:1 is the nominal turns ratio for driving a 438mm x 2.2mm lamp with a 12V supply. Refer to Application Note 3375 for more information.

Table 6. Resistor and Capacitor Selection Guide

DESIGNATOR	QTY	VALUE	TOLERANCE (%) AT 25°C	TEMPERATURE COEFFICIENT	NOTES
R1	1	10kΩ	1	—	—
R2	1	12.5kΩ to 105kΩ	1	—	See the *Setting the SVM Threshold Voltage* section.
R3	1	20kΩ to 40kΩ	1	≤153ppm/°C	2% or less total tolerance. See the *Lamp Frequency Configuration* section to determine value.
R4	1	18kΩ to 45kΩ	1	≤153ppm/°C	2% or less total tolerance. See the *Lamp Frequency Configuration* section to determine value.
R5	1	4.7kΩ	5	Any grade	—
R6	1	4.7kΩ	5	Any grade	—
R7	1	4.7kΩ	5	Any grade	—
R8	1/Ch	140Ω	1	—	See the *Setting the RMS Lamp Current* section.
C1	1/Ch	100nF	10	X7R	Capacitor value will also affect LCM bias voltage during power-up. A larger capacitor may cause a longer time for V_{DCB} to reach its normal operating level.
C2	1/Ch	10pF	5	±1000ppm/°C	2kV to 4kV breakdown voltage required.
C3	1/Ch	27nF	5	X7R	Capacitor value will also affect LCM bias voltage during power-up. A larger capacitor may cause a longer time for V_{DCB} to reach its normal operating level.
C4	1/Ch	33µF	20	Any grade	—
C5	1	0.1µF	10	X7R	Place close to V_{CC} and GND on DS3994.

Typical Operating Circuits



NOTE 1: ONLY ONE CHANNEL SHOWN TO SIMPLIFY DRAWING.
NOTE 2: SEE THE *COMPONENT SELECTION* SECTION FOR RECOMMENDED EXTERNAL COMPONENTS.

Figure 13. Typical Operating Circuit

4-Channel Cold-Cathode Fluorescent Lamp Controller

Typical Operating Circuits (continued)

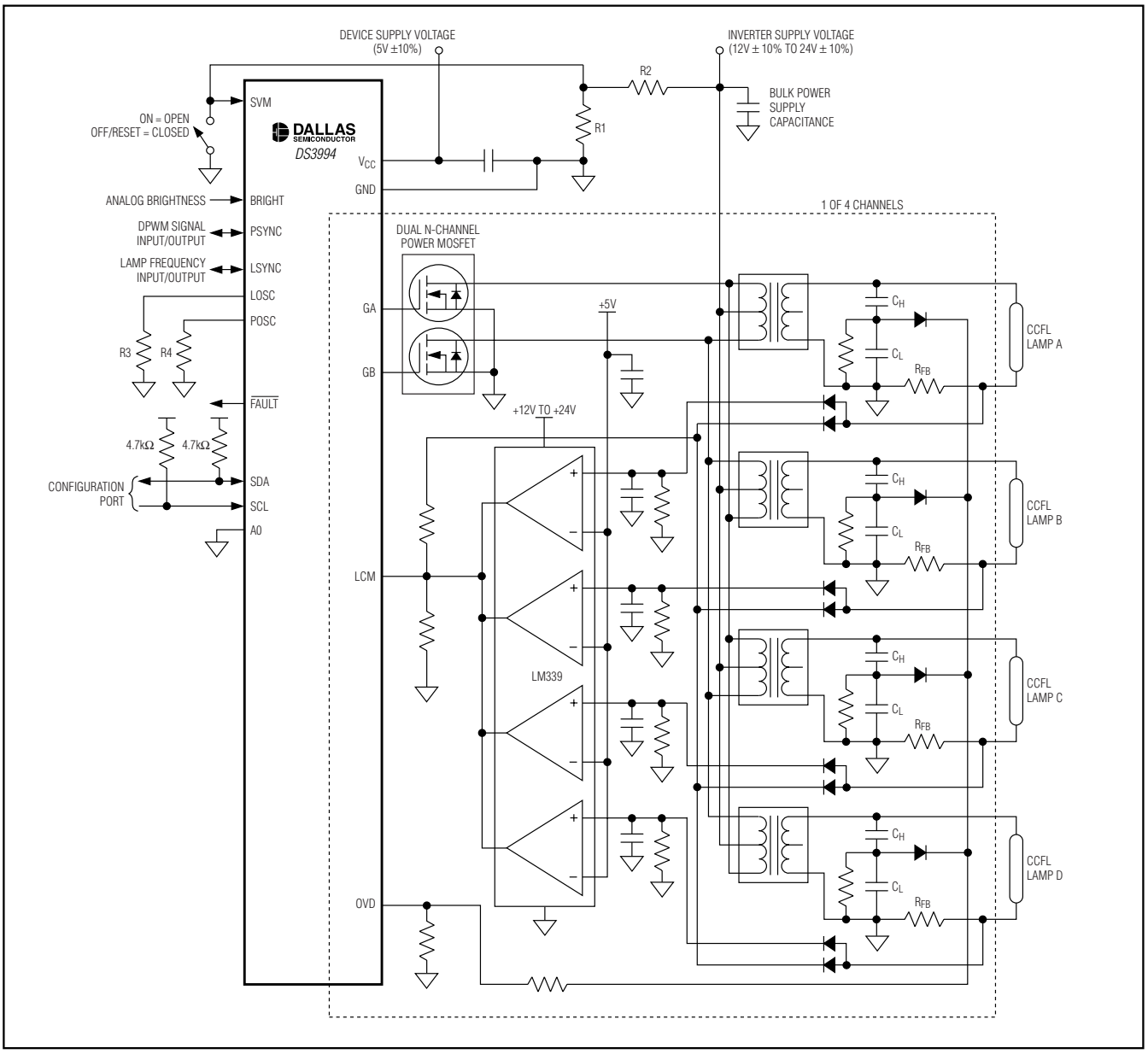


Figure 14. Typical Operating Circuit with Multiple Lamps per Channel

Chip Information

TRANSISTOR COUNT: 53,000

SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.