MC14517B

Dual 64-Bit Static Shift Register

The MC14517B dual 64–bit static shift register consists of two identical, independent, 64–bit registers. Each register has separate clock and write enable inputs, as well as outputs at bits 16, 32, 48, and 64. Data at the data input is entered by clocking, regardless of the state of the write enable input. An output is disabled (open circuited) when the write enable input is high. During this time, data appearing at the data input as well as the 16–bit, 32–bit, and 48–bit taps may be entered into the device by application of a clock pulse. This feature permits the register to be loaded with 64 bits in 16 clock periods, and also permits bus logic to be used. This device is useful in time delay circuits, temporary memory storage circuits, and other serial shift register applications.

- Diode Protection on All Inputs
- Fully Static Operation
- Output Transitions Occur on the Rising Edge of the Clock Pulse
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input
- 3–State Output at 64th–Bit Allows Use in Bus Logic Applications
- Shift Registers of any Length may be Fully Loaded with 16 Clock Pulses
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	–0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	–0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 2.)	500	mW
T_A	Operating Temperature Range	–55 to +125	°C
T_{stg}	Storage Temperature Range	–65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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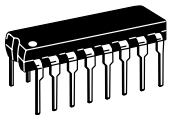
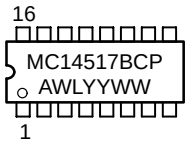
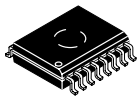
MARKING DIAGRAMS

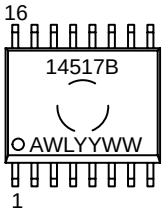


PDIP–16
P SUFFIX
CASE 648





SOIC–16
DW SUFFIX
CASE 751G

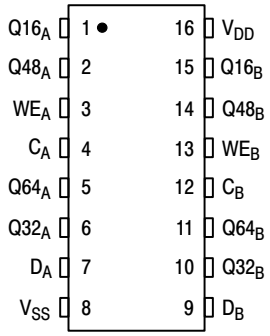


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14517BCP	PDIP–16	2000/Box
MC14517BDW	SOIC–16	47/Rail
MC14517BDWR2	SOIC–16	1000/Tape & Reel

PIN ASSIGNMENT



FUNCTIONAL TRUTH TABLE (X = Don't Care)

Clock	Write Enable	Data	16–Bit Tap	32–Bit Tap	48–Bit Tap	64–Bit Tap
0	0	X	Content of 16–Bit Displayed	Content of 32–Bit Displayed	Content of 48–Bit Displayed	Content of 64–Bit Displayed
0	1	X	High Impedance	High Impedance	High Impedance	High Impedance
1	0	X	Content of 16–Bit Displayed	Content of 32–Bit Displayed	Content of 48–Bit Displayed	Content of 64–Bit Displayed
1	1	X	High Impedance	High Impedance	High Impedance	High Impedance
⎍	0	Data entered into 1st Bit	Content of 16–Bit Displayed	Content of 32–Bit Displayed	Content of 48–Bit Displayed	Content of 64–Bit Displayed
⎍	1	Data entered into 1st Bit	Data at tap entered into 17–Bit	Data at tap entered into 33–Bit	Data at tap entered into 49–Bit	High Impedance
⎎	0	X	Content of 16–Bit Displayed	Content of 32–Bit Displayed	Content of 48–Bit Displayed	Content of 64–Bit Displayed
⎎	1	X	High Impedance	High Impedance	High Impedance	High Impedance

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (3.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
V_{in} = V_{DD} or 0		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
“1” Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
V_{in} = 0 or V_{DD}		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage “0” Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
“1” Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	
(V_{OH} = 4.6 Vdc)		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
(V_{OH} = 9.5 Vdc)		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc)		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current (4.) (5.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (4.2 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (8.8 µA/kHz) f + I_{DD}							
		15	I_T = (13.7 µA/kHz) f + I_{DD}							
Three–State Leakage Current	I_{TL}	15	—	± 0.1	—	± 0.0001	± 0.1	—	± 3.0	µAdc

3. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
4. The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

SWITCHING CHARACTERISTICS [6.] (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ [7.]	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.65 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 390 ns		5.0	—	475	770	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 177 ns		10	—	210	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 115 ns		15	—	140	215	
Clock Pulse Width	t_{WH}	5.0	330	170	—	ns
		10	125	75	—	
		15	100	60	—	
Clock Pulse Frequency	f_{cl}	5.0	—	3.0	1.5	MHz
		10	—	6.7	4.0	
		15	—	8.3	5.3	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	See Note [8.]			—
		10				
		15				
Data to Clock Setup Time	t_{su}	5.0	0	– 40	—	ns
		10	10	– 15	—	
		15	15	0	—	
Data to Clock Hold Time	t_h	5.0	150	75	—	ns
		10	75	25	—	
		15	35	10	—	
Write Enable to Clock Setup Time	t_{su}	5.0	400	170	—	ns
		10	200	65	—	
		15	110	50	—	
Write Enable to Clock Release Time	t_{rel}	5.0	380	160	—	ns
		10	180	55	—	
		15	100	40	—	

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
8. When shift register sections are cascaded, the maximum rise and fall time of the clock input should be equal to or less than the rise and fall time of the data outputs, driving data inputs, plus the propagation delay of the output driving stage.

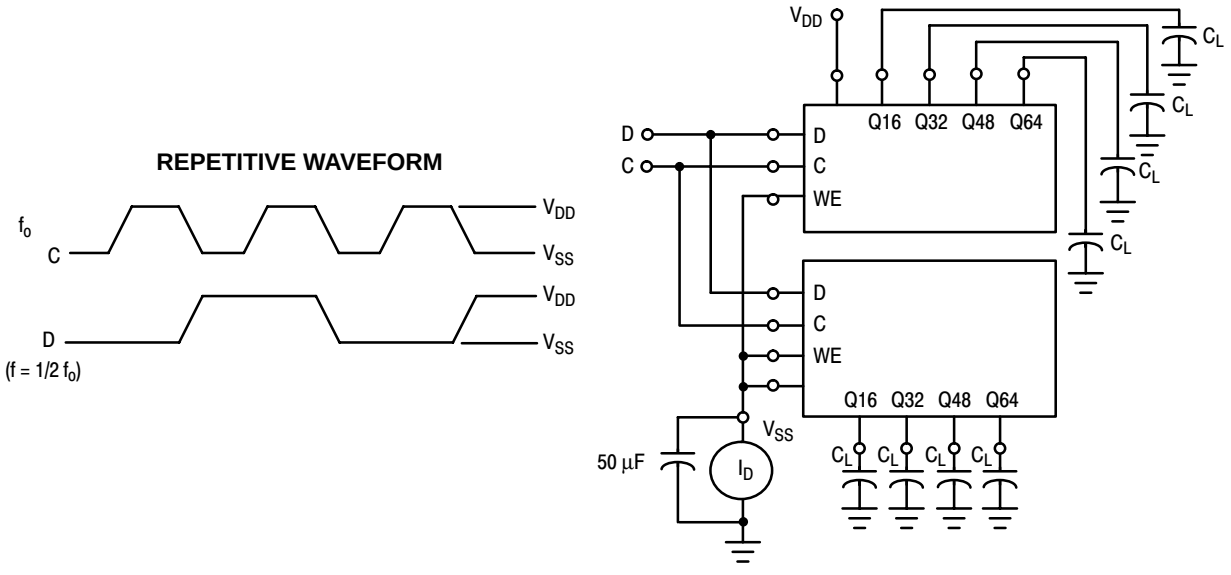
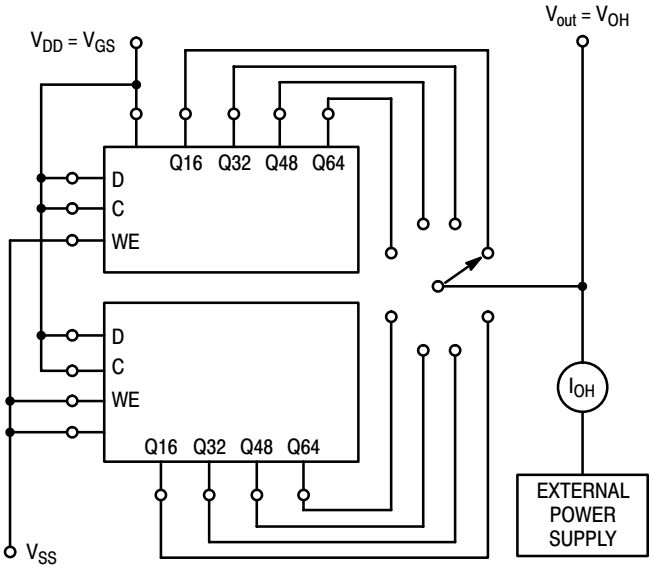
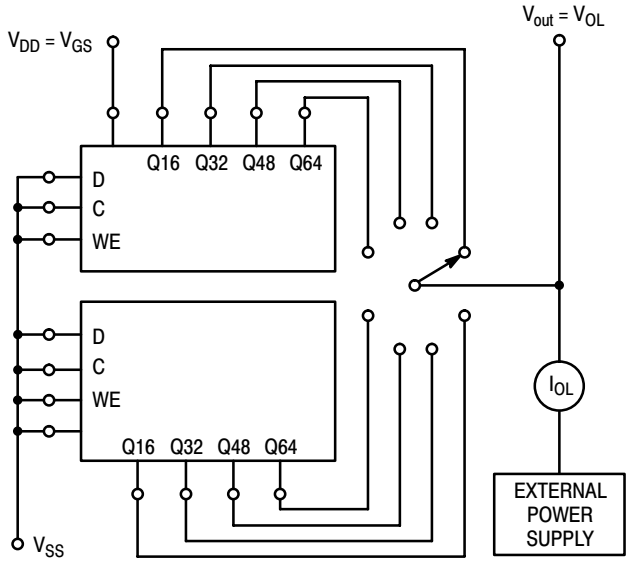


Figure 1. Power Dissipation Test Circuit and Waveform



(Output being tested should be in the high–logic state)

Figure 2. Typical Output Source Current Characteristics Test Circuit



(Output being tested should be in the low–logic state)

Figure 3. Typical Output Sink Current Characteristics Test Circuit

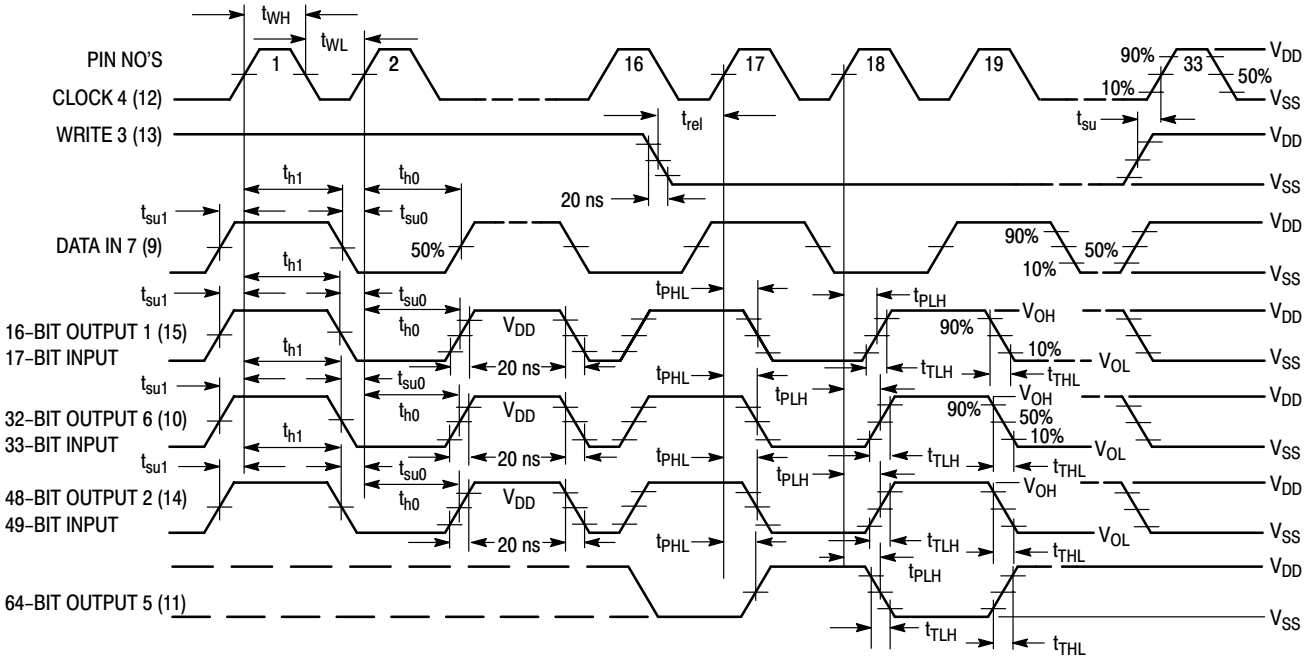
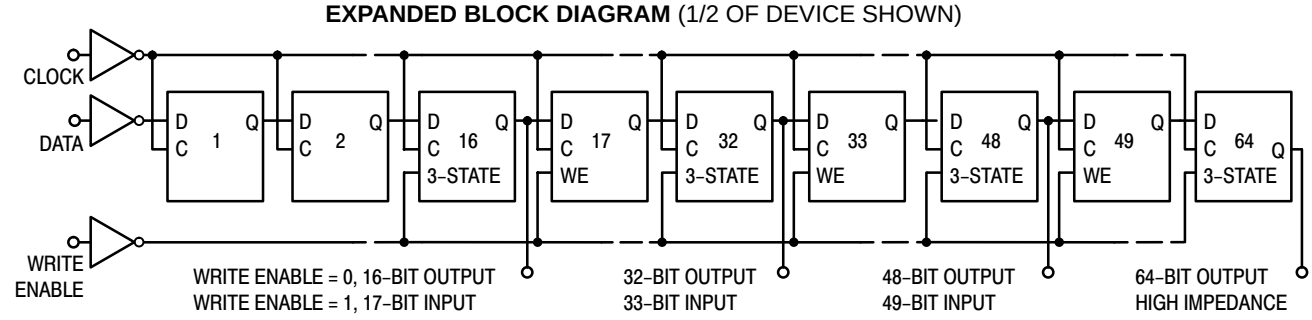


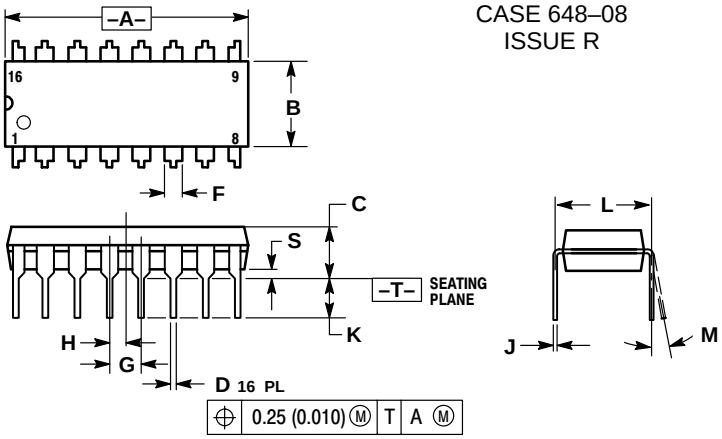
Figure 4. AC Test Waveforms

EXPANDED BLOCK DIAGRAM (1/2 OF DEVICE SHOWN)



PACKAGE DIMENSIONS

PDIP–16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

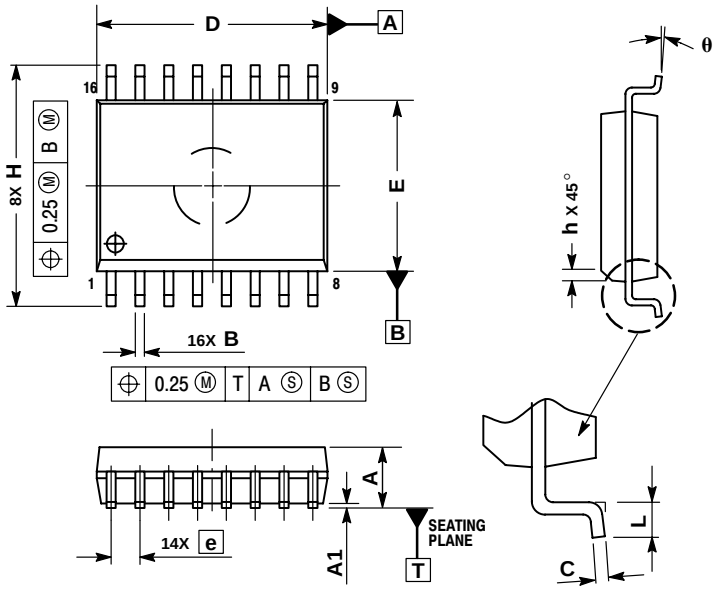


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

PACKAGE DIMENSIONS

SOIC–16
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751G–03
ISSUE B



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

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