



128Kx8 SRAM

PRELIMINARY *

PLASTIC PLUS™ FEATURES

- Access Times 55, 70, 85nS
- Standard Commercial Off-The-Shelf (COTS) Memory Devices for Extended Temperature Range
- JEDEC Standard Packages:
 - 32 Pin 600mil Plastic DIP
 - 32 Lead 525mil Plastic SOP
 - 32 Lead TSOP(I) Forward and Reverse
- Electrical and Speed Characteristics for:
 - Military Temperature (-55°C to +125°C)
 - Industrial Temperature (-40°C to +85°C)
- Burn-in and Temperature Cycle Available
- Organized as 128K x 8

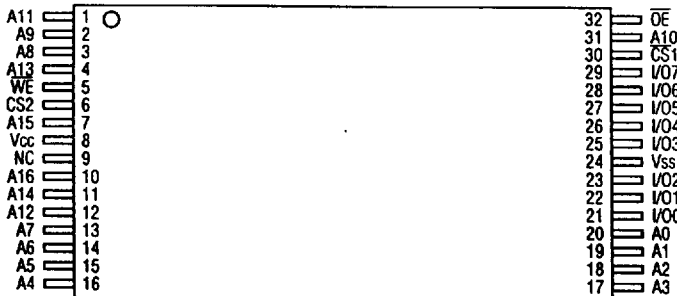
- 5 Volt Power Supply
- Low Power CMOS, 35mW typ.
- Battery Back-Up Operation
- Reliability Test Data Available:
 - High Temperature Operating Life
 - High Temperature Storage
 - Pressure Cooker Test
 - Wet High Temperature Operating Life
 - Thermal Shock
 - Temperature Cycling

* This data sheet describes a product under development and is subject to change without notice.

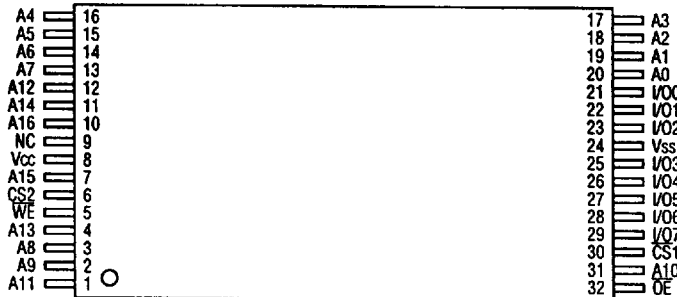
Plastic SRAM

PIN CONFIGURATIONS

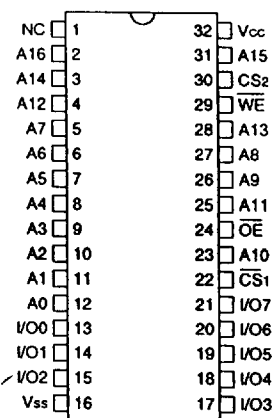
TSOP(I) FORWARD TOP VIEW



TSOP(I) REVERSE TOP VIEW



DIP SOP TOP VIEW



PIN DESCRIPTION

| | |
|------------------------|-------------------|
| A0-16 | Address Inputs |
| I/O0-7 | Data Input/Output |
| $\overline{CS1}$ - CS2 | Chip Selects |
| \overline{OE} | Output Enable |
| \overline{WE} | Write Enable |
| Vcc | +5.0V Power |
| Vss | Ground |



ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min | Max | Unit |
|--------------------------------|------------------|------|-----------------------|------|
| Operating Temperature (Mil.) | T _A | -55 | +125 | °C |
| Operating Temperature (Ind.) | T _A | -40 | +85 | °C |
| Storage Temperature | T _{STG} | -65 | +150 | °C |
| Signal Voltage Relative to GND | V _S | -0.5 | V _{CC} + 0.5 | V |
| Supply Voltage | V _{CC} | -0.5 | 7.0 | V |

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|------------------------------|-----------------|------|-----------------------|------|
| Supply Voltage | V _{CC} | 4.5 | 5.5 | V |
| Input High Voltage | V _{IH} | 2.2 | V _{CC} + 0.5 | V |
| Input Low Voltage | V _{IL} | -0.3 | +0.8 | V |
| Operating Temperature (Mil.) | T _A | -55 | +125 | °C |
| Operating Temperature (Ind.) | T _A | -40 | +85 | °C |

TRUTH TABLE

| CS ₁ | CS ₂ | WE | OE | Mode | I/O Pin | V _{CC} Current |
|-----------------|-----------------|----|----|-------------|---------|------------------------------------|
| H | X | X | X | Power Down | High-Z | I _{SB} , I _{SBL} |
| X | L | X | X | Power Down | High-Z | I _{SB} , I _{SBL} |
| L | H | H | H | Out Disable | High-Z | I _{CC} |
| L | H | H | L | Read | Dout | I _{CC} |
| L | H | L | X | Write | Din | I _{CC} |

CAPACITANCE

(T_A = +25°C)

| Parameter | Symbol | Condition | Max | Unit |
|--------------------|------------------|-----------------------------------|-----|------|
| Input capacitance | C _{IN} | V _{IN} = 0V, f = 1.0MHz | 6 | pF |
| Output capacitance | C _{OUT} | V _{OUT} = 0V, f = 1.0MHz | 8 | pF |

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C to +125°C)

| Parameter | Symbol | Conditions | Units | | |
|--------------------------|-----------------|--|-------|------|----|
| | | | Min | Max | |
| Input Leakage Current | I _{LI} | V _{CC} = 5.5, V _{IN} = GND to V _{CC} | | 10 | μA |
| Output Leakage Current | I _{LO} | CS ₁ = V _{IH} , CS ₂ = V _{IL} , OE = V _{IH} , V _{OUT} = GND to V _{CC} | | 10 | μA |
| Operating Supply Current | I _{CC} | CS ₁ = V _{IL} , CS ₂ = V _{IH} , OE = V _{IH} , f = 5MHz, V _{CC} = 5.5 | | 30 | mA |
| Standby Current | I _{SB} | CS ₁ = V _{IH} , CS ₂ = OE = V _{IH} , f = 5MHz, V _{CC} = 5.5 | | 0.25 | mA |
| Output Low Voltage | V _{OL} | I _{OL} = 2.1mA, V _{CC} = 4.5 | | 0.4 | V |
| Output High Voltage | V _{OH} | I _{OH} = -1.0mA, V _{CC} = 4.5 | 2.4 | | V |

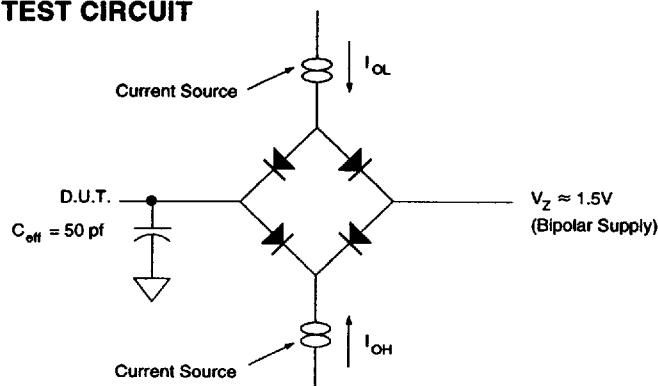
NOTE: DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

| Parameter | Symbol | Conditions | Units | | | |
|-------------------------------|-------------------|--|-------|-----|-----|----|
| | | | Min | Typ | Max | |
| Data Retention Supply Voltage | V _{DR} | CS ₁ Controlled: CS ₁ ≥ V _{CC} - 0.2V, CS ₂ ≥ V _{CC} - 0.2V CS ₂ Controlled: CS ₂ ≤ 0.2V | 2.0 | | 5.5 | V |
| Data Retention Current | I _{CCDR} | V _{CC} = 3V | | 3 | 180 | μA |

AC TEST CIRCUIT



AC TEST CONDITIONS

| Parameter | Typ | Unit |
|----------------------------------|--|------|
| Input Pulse Levels | V _{IL} = 0, V _{IH} = 3.0 | V |
| Input Rise and Fall | 5 | nS |
| Input and Output Reference Level | 1.5 | V |
| Output Timing Reference Level | 1.5 | V |

NOTES:

V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z₀ = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

**AC CHARACTERISTICS**(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

| Parameter | Symbol | -55 | | -70 | | -85 | | Units |
|------------------------------------|-------------------|-----|-----|-----|-----|-----|-----|-------|
| | | Min | Max | Min | Max | Min | Max | |
| Read Cycle | | | | | | | | |
| Read Cycle Time | t _{RC} | 55 | | 70 | | 85 | | nS |
| Address Access Time | t _{AA} | | 55 | | 70 | | 85 | nS |
| Output Hold from Address Change | t _{OH} | 5 | | 5 | | 5 | | nS |
| Chip Select Access Time | t _{ACS} | | 55 | | 70 | | 85 | nS |
| Output Enable to Output Valid | t _{OE} | | 25 | | 35 | | 45 | nS |
| Chip Select to Output in Low Z | t _{CLZ'} | 10 | | 10 | | 10 | | nS |
| Output Enable to Output in Low Z | t _{OLZ'} | 5 | | 5 | | 5 | | nS |
| Chip Disable to Output in High Z | t _{CHZ'} | | 20 | | 25 | | 30 | nS |
| Output Disable to Output in High Z | t _{OHZ'} | | 20 | | 25 | | 30 | nS |

1. This parameter is guaranteed by design but not tested.

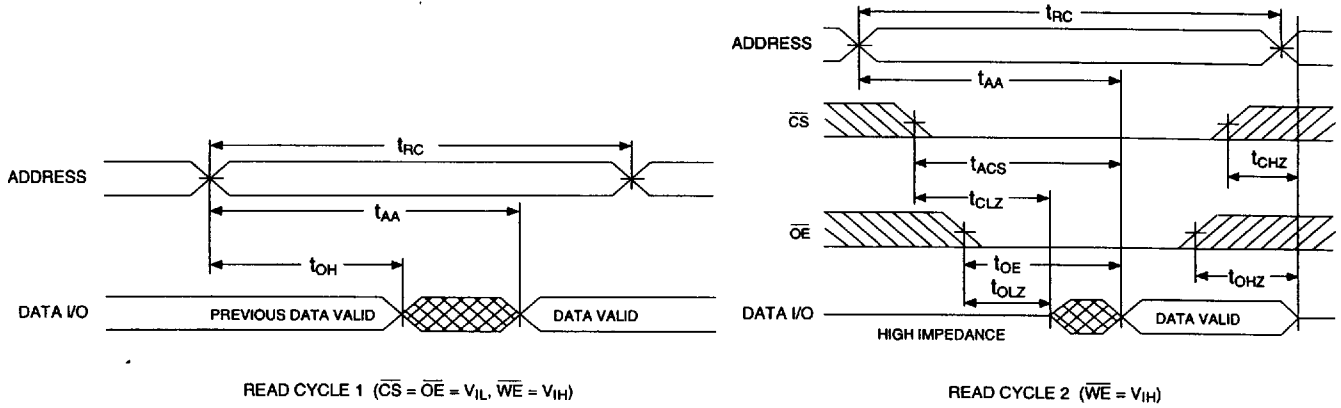
AC CHARACTERISTICS(V_{CC} = 5.0V, T_A = -55°C to +125°C)

| Parameter | Symbol | -55 | | -70 | | -85 | | Units |
|----------------------------------|-------------------|-----|-----|-----|-----|-----|-----|-------|
| | | Min | Max | Min | Max | Min | Max | |
| Write Cycle | | | | | | | | |
| Write Cycle Time | t _{WC} | 55 | | 70 | | 85 | | nS |
| Chip Select to End of Write | t _{CW} | 45 | | 60 | | 70 | | nS |
| Address Valid to End of Write | t _{AW} | 50 | | 60 | | 70 | | nS |
| Data Valid to End of Write | t _{DW} | 25 | | 30 | | 35 | | nS |
| Write Pulse Width | t _{WP} | 40 | | 50 | | 55 | | nS |
| Address Setup Time | t _{AS} | 0 | | 0 | | 0 | | nS |
| Address Hold Time | t _{AH} | 0 | | 0 | | 0 | | nS |
| Output Active from End of Write | t _{OW'} | 5 | | 5 | | 5 | | nS |
| Write Enable to Output in High Z | t _{WHZ'} | | 20 | | 25 | | 30 | nS |
| Data Hold Time | t _{DH} | 0 | | 0 | | 0 | | nS |

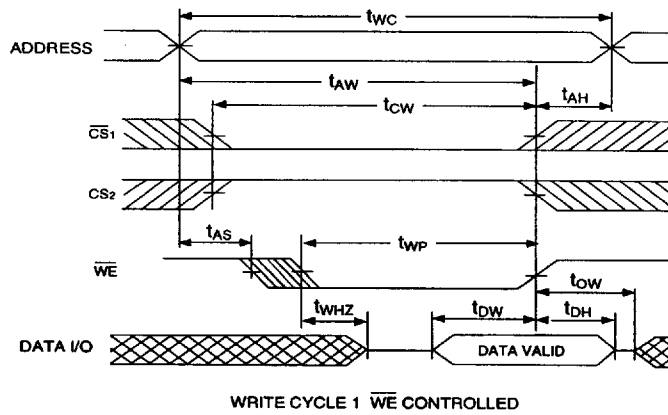
1. This parameter is guaranteed by design but not tested.



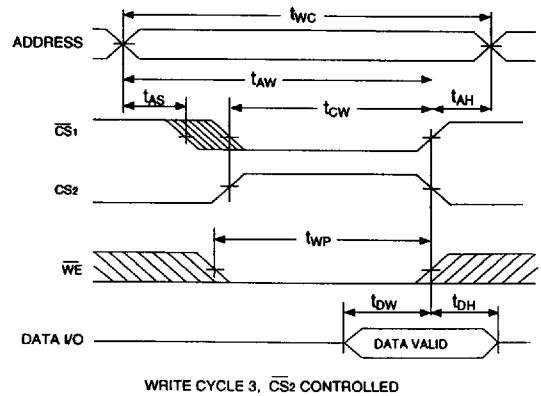
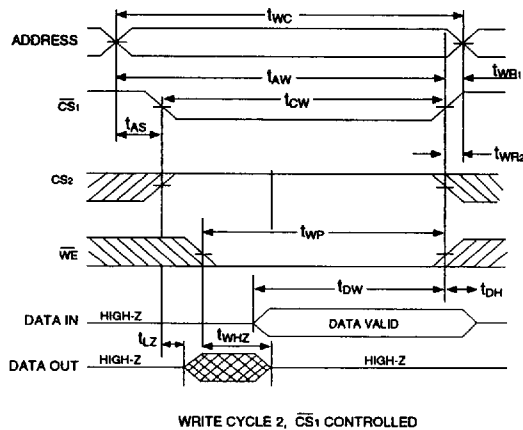
TIMING WAVEFORM - READ CYCLE



WRITE CYCLE 1

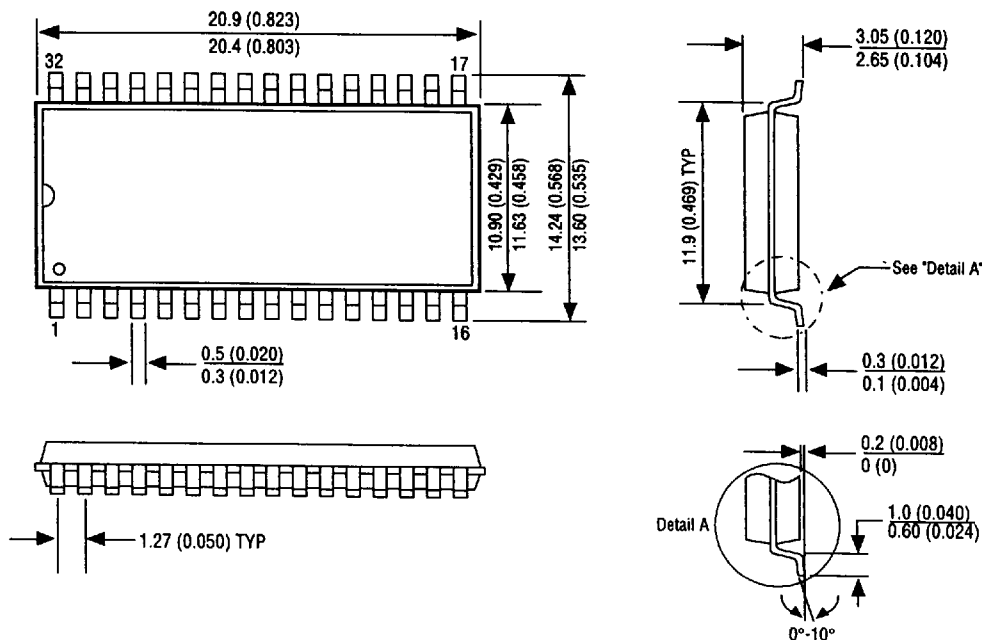


WRITE CYCLES 2 & 3



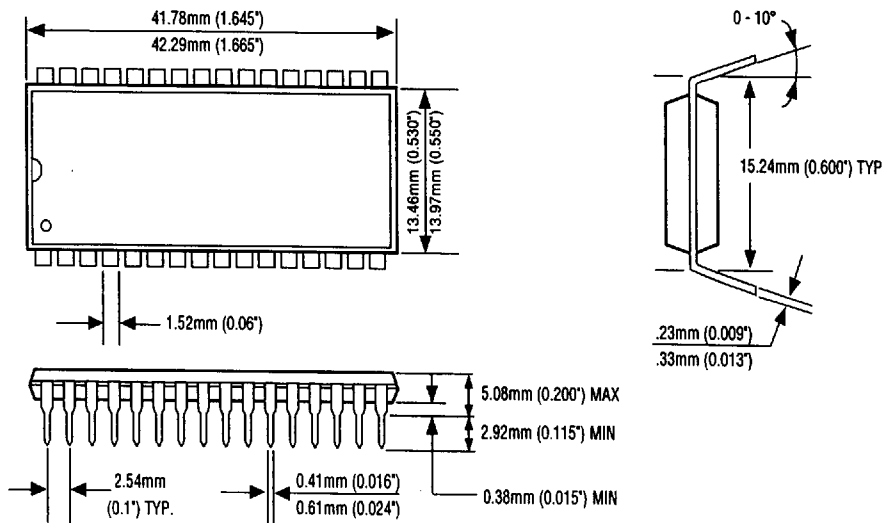


32 LEAD, PLASTIC SOP (525 mil) PACKAGE DIMENSION



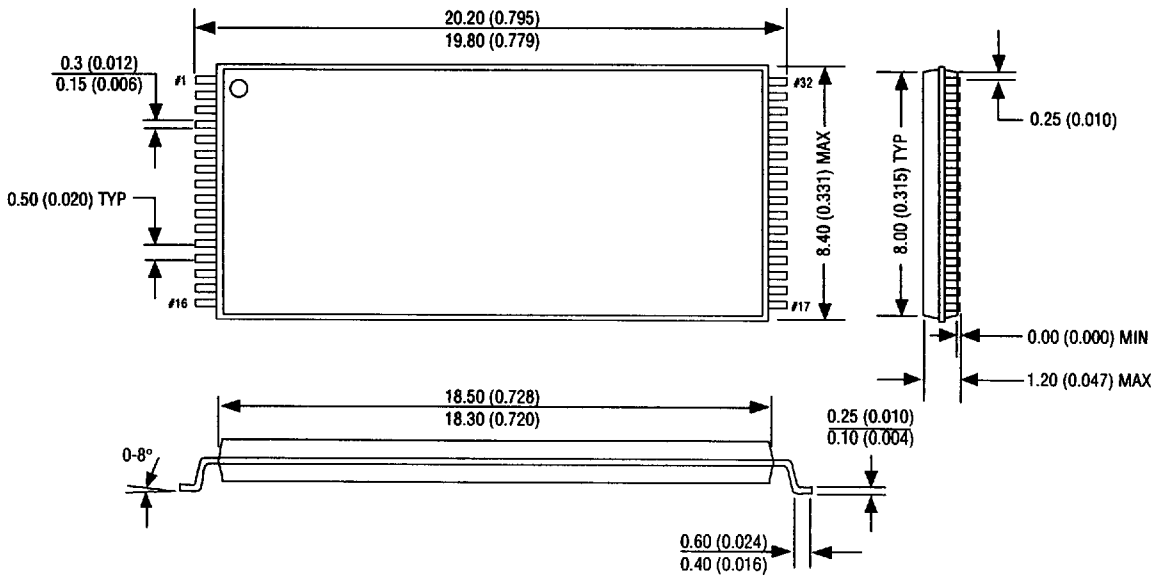
DIMENSIONS IN MILLIMETERS AND (INCHES)

32 PIN, PLASTIC DIP PACKAGE DIMENSION



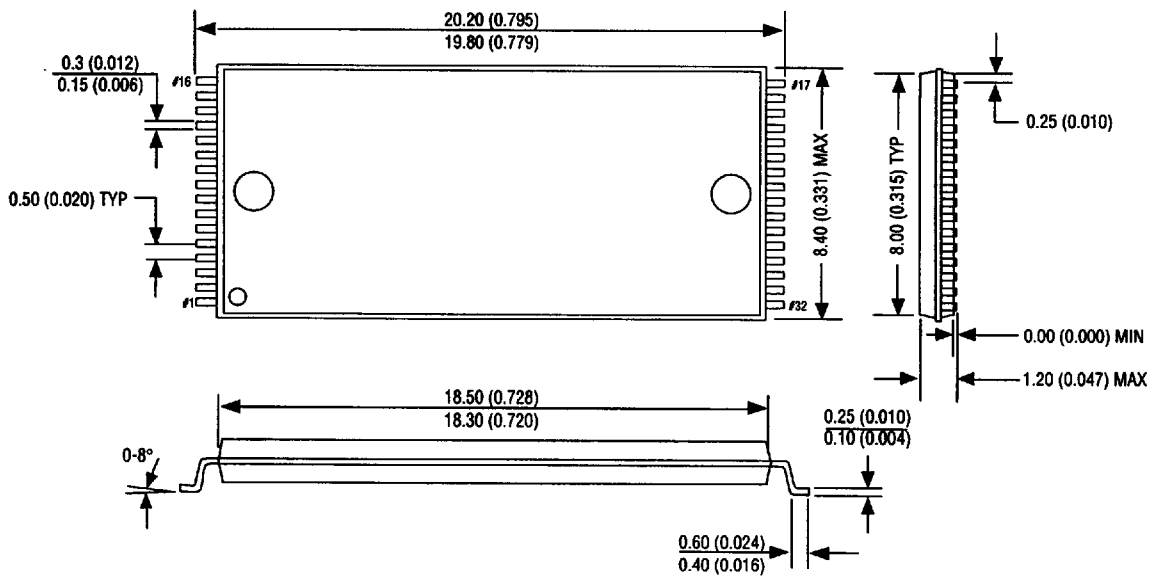


32 LEAD, PLASTIC TSOP I FORWARD PACKAGE DIMENSION



DIMENSIONS IN MILLIMETERS AND (INCHES)

32 LEAD, PLASTIC TSOP I REVERSE PACKAGE DIMENSION



DIMENSIONS IN MILLIMETERS AND (INCHES)



ORDERING INFORMATION

W P S 128K 8 X - XXX X X

DEVICE GRADE:

- M = Military Temperature -55°C to +125°C
- I = Industrial Temperature -40°C to +85°C

PACKAGE:

- W = 32 pin 600mil Plastic DIP
- G = 32 lead SOP (525 mil)
- TF = 32 TSOP(I) Forward
- TR = 32 TSOP(I) Reverse

ACCESS TIME in nS

IMPROVEMENT MARK

- B = Burn-in
- T = Temperature Cycle
- C = Burn-in and Temperature Cycle

ORGANIZATION, 128K x 8

SRAM

PLASTIC PLUS™

WHITE MICROELECTRONICS