



# STW24NK55Z

N-channel 550 V - 0.18  $\Omega$  - 23 A - TO-247  
Zener-protected SuperMESH™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STW24NK55Z	550 V	<0.22 $\Omega$	23 A	285 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability

## Application

- Switching applications

## Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs.

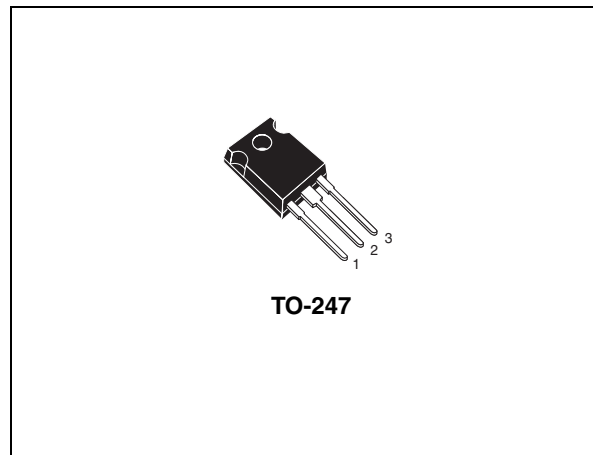


Figure 1. Internal schematic diagram

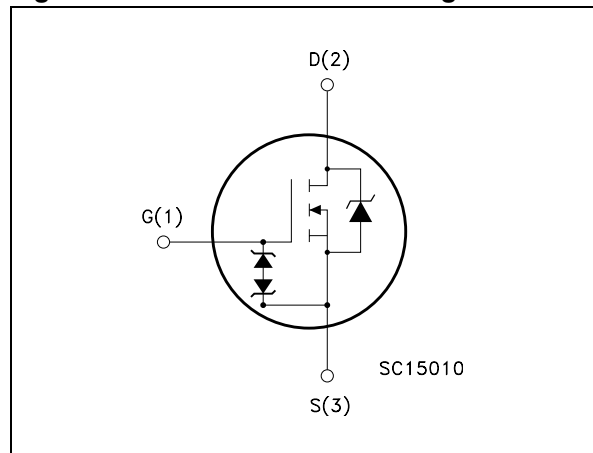


Table 1. Device summary

Order code	Marking	Package	Packaging
STW24NK55Z	24NK55Z	TO-247	Tube

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	550	V
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	23	A
$I_D$	Drain current (continuous) at $T_C=100\text{ }^\circ\text{C}$	10.35	A
$I_{DM}^{(1)}$	Drain current (pulsed)	92	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	285	W
	Derating factor	2.27	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$T_{stg}$	Storage temperature	-55 to $150\text{ }^\circ\text{C}$	$^\circ\text{C}$
$T_J$	Max. perating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2.  $I_{SD} \leq 23\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.44	$^\circ\text{C}/\text{W}$
$R_{thj-a}$	Thermal resistance junction-ambient max	50	$^\circ\text{C}/\text{W}$
$T_I$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ Max)	23	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J=25\text{ }^\circ\text{C}$ , $I_D=I_{AR}$ , $V_{DD}=50\text{ V}$ )	400	mJ

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}, V_{GS} = 0$	550			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating @ } 125\text{ °C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 11.5\text{ A}$		0.18	0.22	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}, I_D = 11.5\text{ A}$		20		S
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$		4397.5		pF
$C_{oss}$	Output capacitance			480.5		pF
$C_{rss}$	Reverse transfer capacitance			116		pF
$C_{oss\ eq}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0\text{ to } 480\text{ V}$		250		pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}, \text{ open drain}$		2.3		$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 440\text{ V}, I_D = 23\text{ A}$ $V_{GS} = 10\text{ V}$ <i>(see Figure 15)</i>		130		nC
$Q_{gs}$	Gate-source charge			25		nC
$Q_{gd}$	Gate-drain charge			76		nC
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 275\text{ V}, I_D = 11.5\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ <i>(see Figure 14)</i>		30		ns
$t_r$	Rise time			35		ns
$t_{d(off)}$	Turn-off delay time			136		ns
$t_f$	Fall time			88		ns

1. Pulsed: pulse duration=300  $\mu\text{s}$ , duty cycle 1.5%

2.  $C_{oss\ eq}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				23	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				92	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=23\text{ A}$ , $V_{GS}=0$			1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD}=23\text{ A}$ , $V_{DD}=50\text{ V}$		508		ns
$Q_{rr}$	Reverse recovery charge	$di/dt = 100\text{ A}/\mu\text{s}$ ,		7.4		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 18)		29		A
$t_{rr}$	Reverse recovery time	$I_{SD}=23\text{ A}$ ,		608		ns
$Q_{rr}$	Reverse recovery charge	$di/dt = 100\text{ A}/\mu\text{s}$ ,		9.7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	$V_{DD}=50\text{ V}$ , $T_J=150\text{ }^\circ\text{C}$		31.8		A
		(see Figure 18)				

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300  $\mu\text{s}$ , duty cycle 1.5%

**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{GS}=\pm 1\text{ mA}$ (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

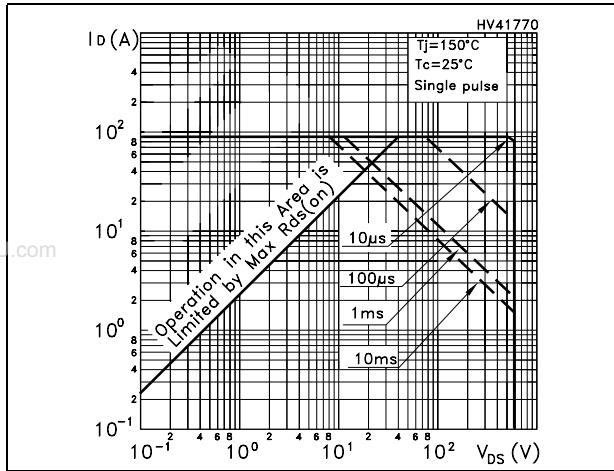


Figure 3. Thermal impedance

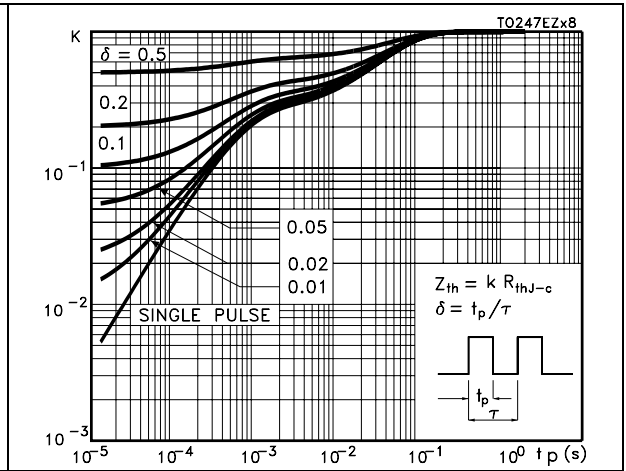


Figure 4. Output characteristics

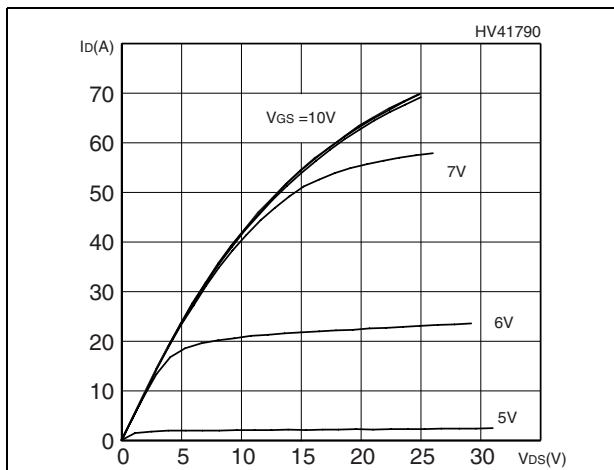


Figure 5. Transfer characteristics

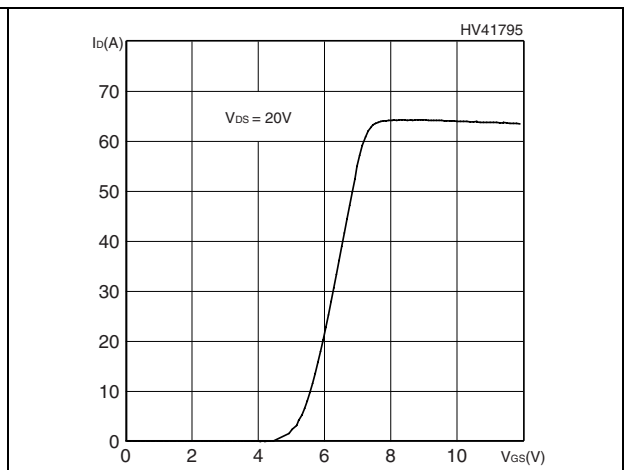


Figure 6. Normalized  $BV_{DSS}$  vs temperature

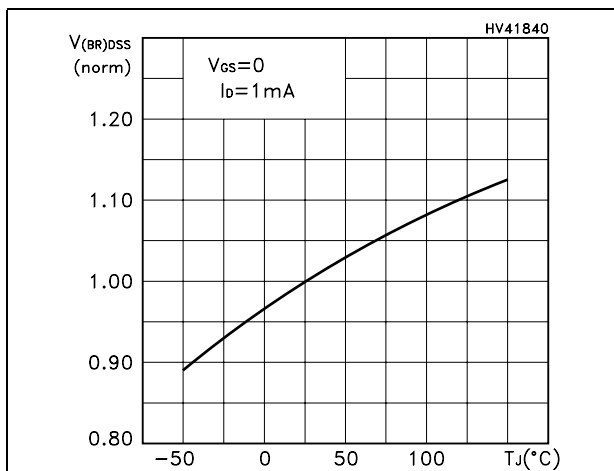


Figure 7. Static drain-source on resistance

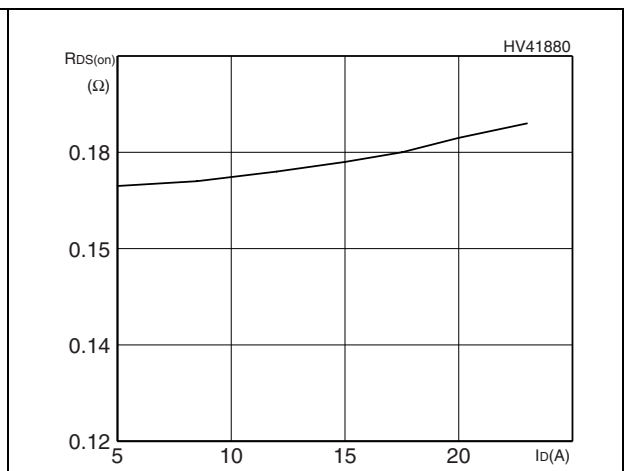


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

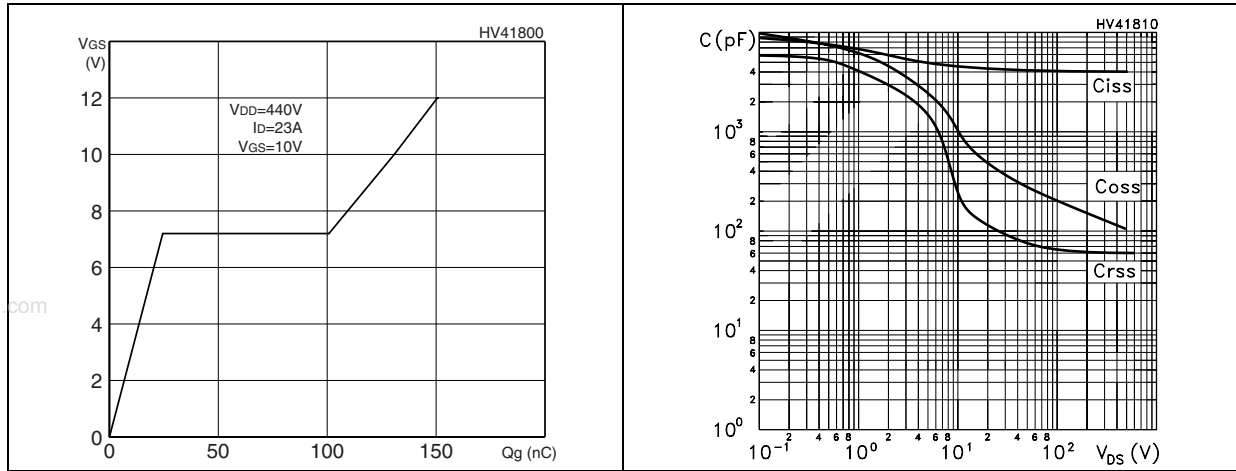


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

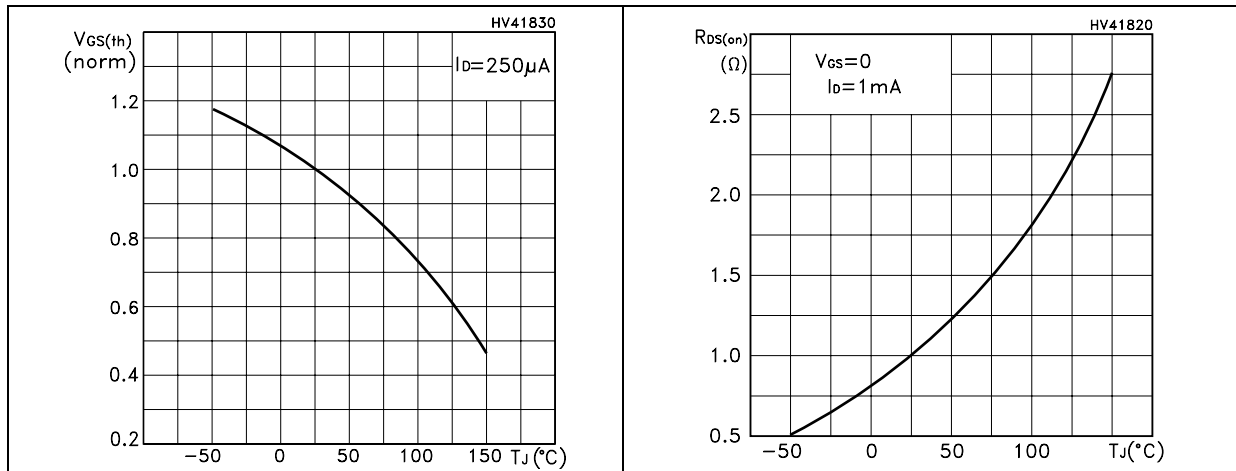
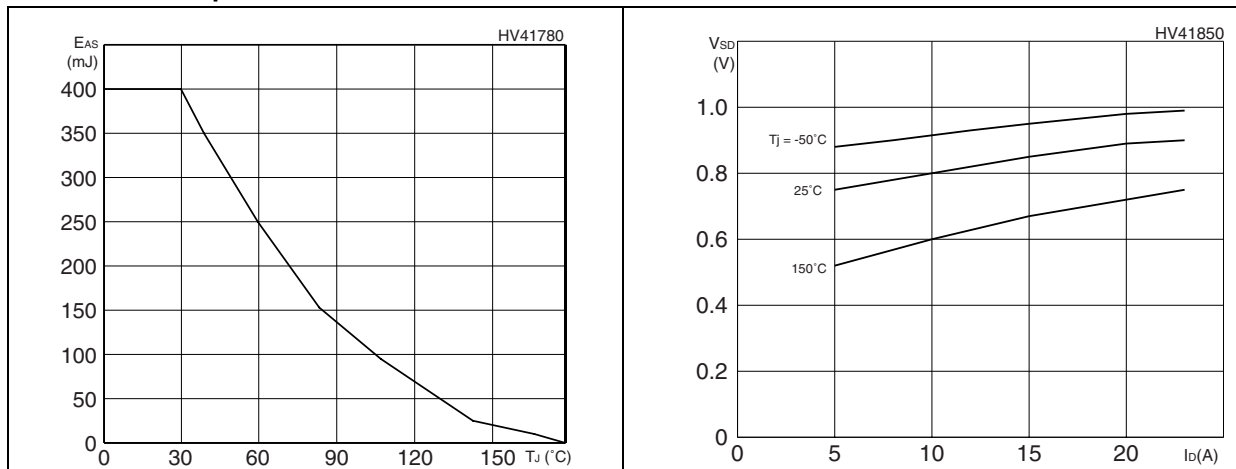


Figure 12. Maximum avalanche energy vs temperature Figure 13. Source-drain diode forward characteristics



### 3 Test circuits

Figure 14. Switching times test circuit for resistive load

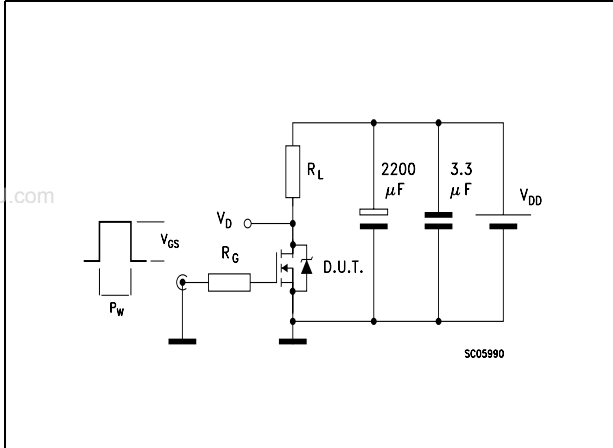


Figure 15. Gate charge test circuit

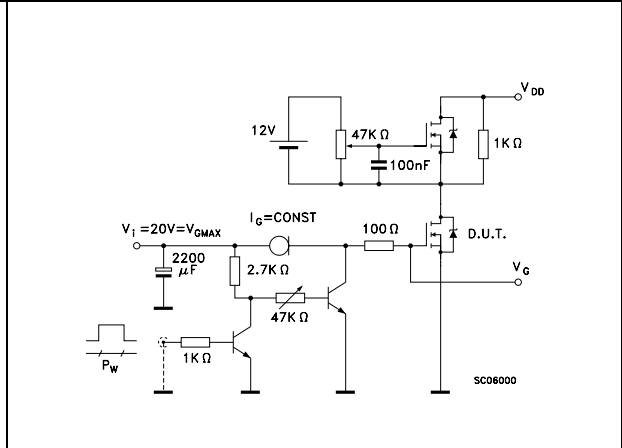


Figure 16. Test circuit for inductive load switching and diode recovery times



Figure 17. Unclamped Inductive load test circuit

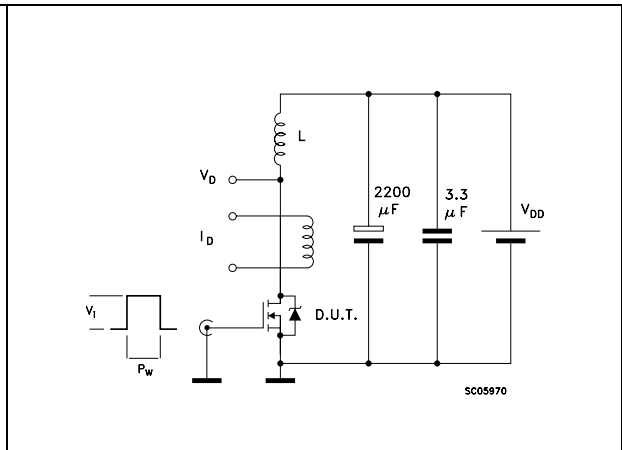


Figure 18. Unclamped inductive waveform

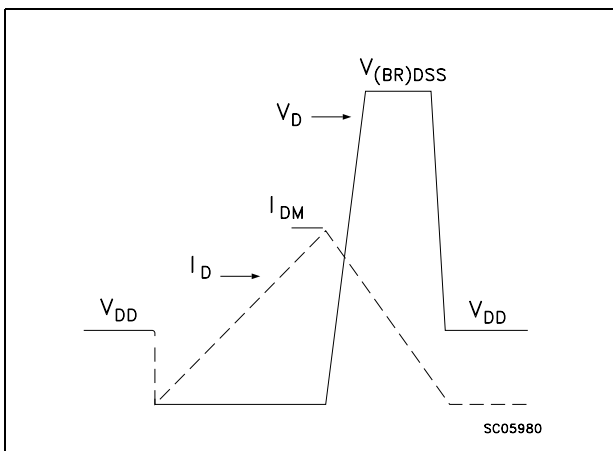
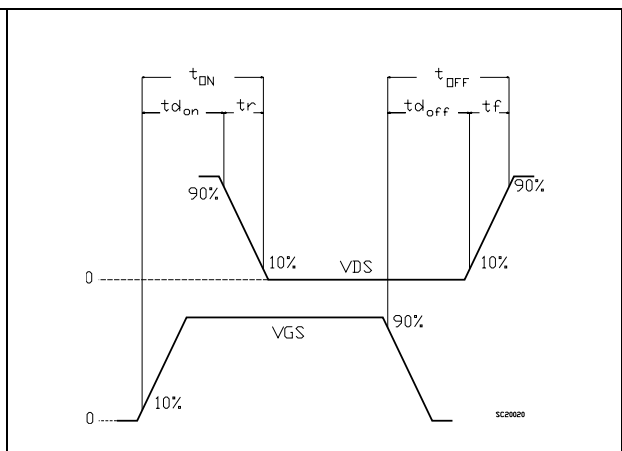


Figure 19. Switching time waveform



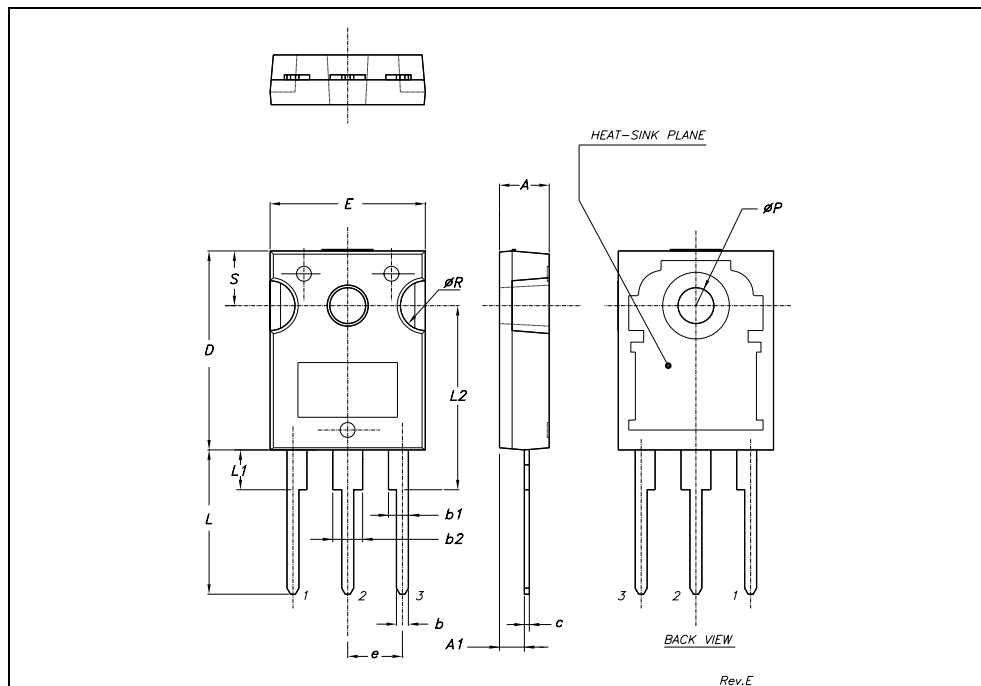


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
04-Jan-2008	1	First release

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