

# MAS9128A

## LDO Voltage Regulator IC

- Three low dropout voltage regulators
- Regulator enable/disable control
- Power saving sleep mode
- Thermal protection

### DESCRIPTION

The MAS9128A is voltage regulator IC with three 2.85V LDO regulators providing voltage regulation for the handset terminal. The output voltages of the three regulators can be modified through a mask option. Two enable/disable pins control the state of

the regulators. In order to save power the device goes into sleep mode when all regulators are disabled. An internal thermal protection circuit prevents the device from overheating. The maximum output current is limited internally.

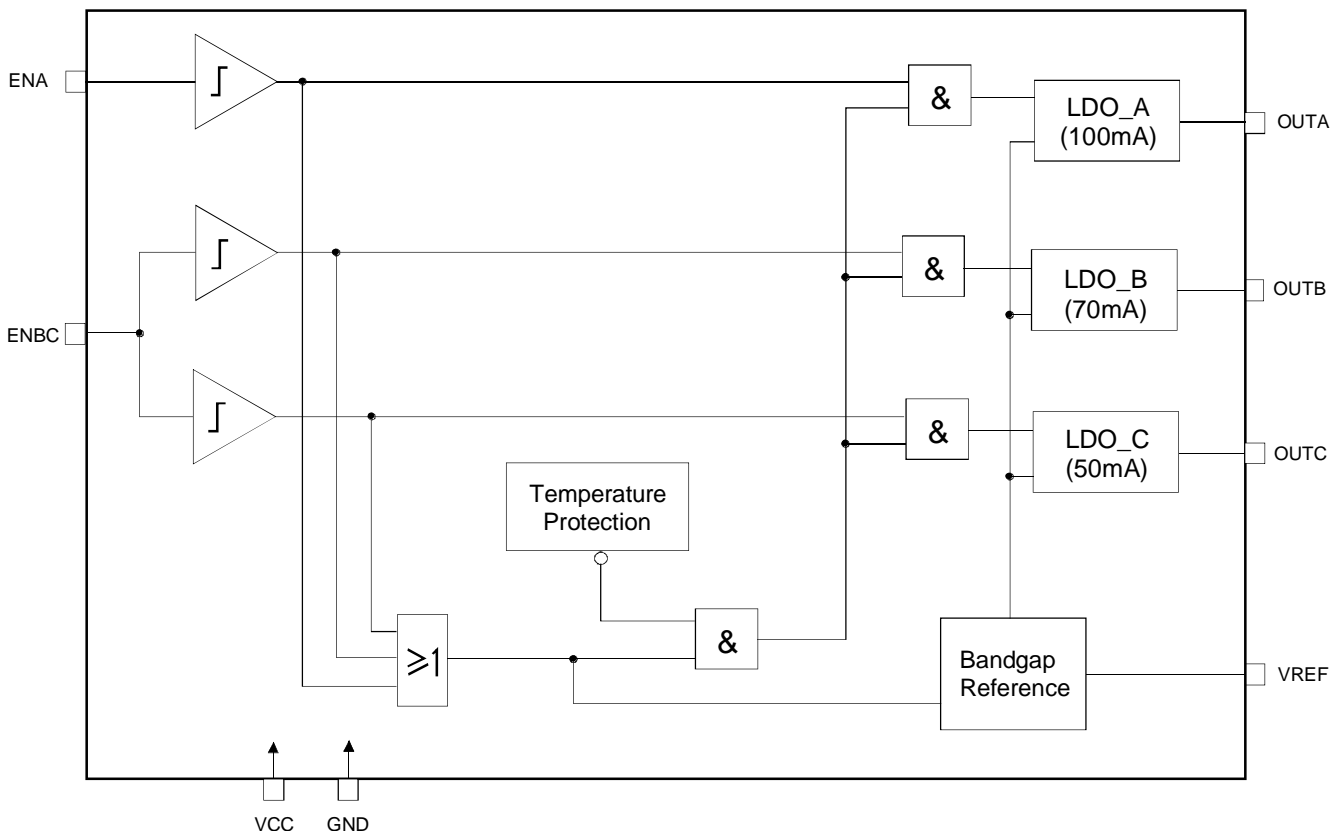
### FEATURES

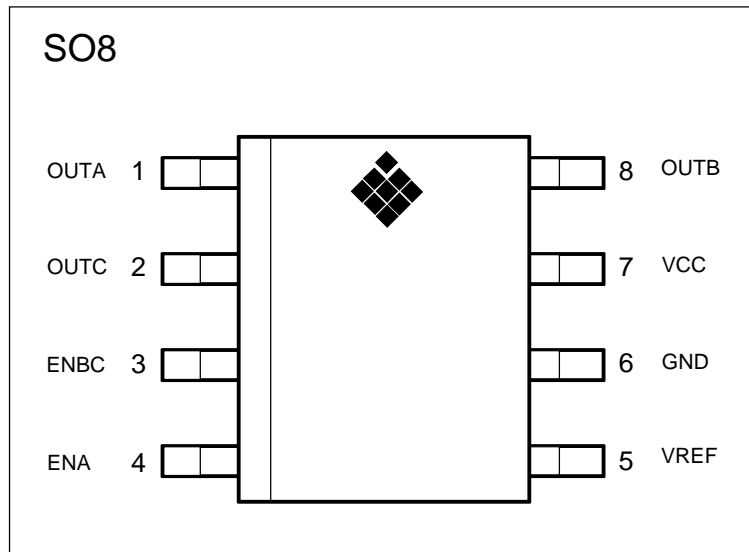
- 2.85V regulators at 100mA, 70mA and 50mA
- Output accuracy  $<\pm 3\%$
- Fast dynamic response
- Low output noise
- Low supply current: 150 $\mu$ A per regulator
- SO8 package

### APPLICATION

- Mobile phones
- Cordless phones
- Battery powered systems

### BLOCK DIAGRAM



**PIN CONFIGURATION**

**PIN DESCRIPTION**

| Pin Name | Pin | Type | Function                      |
|----------|-----|------|-------------------------------|
| OUTA     | 1   | O    | 2.85V/100mA regulator output  |
| OUTC     | 2   | O    | 2.85V/50mA regulator output   |
| ENBC     | 3   | I    | Enable for regulators B and C |
| ENA      | 4   | I    | Enable for regulator A        |
| VREF     | 5   | O    | Reference voltage             |
| GND      | 6   | P    | Ground                        |
| VCC      | 7   | P    | Positive supply voltage       |
| OUTA     | 8   | O    | 2.85V/70mA regulator output   |

## ABSOLUTE MAXIMUM RATINGS

(All voltages with respect to ground.)

| Parameter                 | Symbol   | Conditions     | Min  | Max          | Unit                        |
|---------------------------|----------|----------------|------|--------------|-----------------------------|
| Supply Voltage            | $V_{CC}$ |                | -0.3 | 13.0         | V                           |
| Logic input voltage       | $V_{EN}$ |                | -0.3 | $V_{CC}+0.3$ |                             |
| Max. Junction Temperature | $T_J$    |                |      | 150          | $^{\circ}\text{C}$          |
| Thermal resistance        | $R_{JA}$ |                |      | 163          | $^{\circ}\text{C}/\text{W}$ |
| Lead temperature          |          | for 10 seconds |      | 230          | $^{\circ}\text{C}$          |
| Storage Temperature       | $T_S$    |                | -55  | +150         | $^{\circ}\text{C}$          |
| ESD Rating                |          |                |      |              |                             |

Note 1: Stresses beyond those listed may cause permanent damage to the device. The device may not operate under these conditions, but will not be destroyed.

## RECOMMENDED OPERATION CONDITIONS

| Parameter             | Symbol    | Conditions | Min | Typ | Max | Unit               |
|-----------------------|-----------|------------|-----|-----|-----|--------------------|
| Supply Voltage        | $V_{CC}$  |            | 3.1 |     | 6.5 | V                  |
| Operating Temperature | $T_{AMB}$ |            | -20 |     | +70 | $^{\circ}\text{C}$ |

## ELECTRICAL CHARACTERISTICS

### ◆ Thermal protection

| Parameter                                 | Symbol | Conditions                     | Min | Typ | Max | Unit               |
|---|--------|--------------------------------|-----|-----|-----|--------------------|
| Threshold high                            | $T_H$  |                                | 130 | 150 | 170 | $^{\circ}\text{C}$ |
| Threshold low                             | $T_L$  |                                | 120 | 140 | 160 | $^{\circ}\text{C}$ |
| Continuous power dissipation in operation |        | $T_{AMB} = 25^{\circ}\text{C}$ |     |     | 644 | mW                 |
|   |        | $T_{AMB} = 70^{\circ}\text{C}$ |     |     | 368 | mW                 |

NOTE 2: A hysteresis of  $10^{\circ}\text{C}$  avoids oscillation in case of thermal shutdown. After the regulator temperature has dropped by this value, it will turn on again automatically.

### ◆ Digital Inputs (ENA, ENBC)

( $T_{AMB} = -20^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ , unless otherwise noted. Typical value for  $T_J$  is  $27^{\circ}\text{C}$ .)

| Parameter          | Symbol   | Conditions | Min | Typ | Max  | Unit |
|--------------------|----------|------------|-----|-----|------|------|
| Input high voltage | $V_{IH}$ |            | 2.2 |     |      | V    |
| Input low voltage  | $V_{IL}$ |            |     |     | 0.40 | V    |

**ELECTRICAL CHARACTERISTICS**
**◆ Regulator Outputs (LDO\_A, LDO\_B, LDO\_C)**

 (T<sub>AMB</sub> = -20°C to +70°C, unless otherwise noted. Typical value for J is 27°C Cin=1μF Cout= 1μF,ceramic)

| Parameter                       | Symbol            | Conditions  | Min  | Typ  | Max | Unit  |
|---------------------------------|-------------------|---|------|------|-----|-------|
| Output voltage                  | V <sub>OUT</sub>  | 3.1V < V <sub>CC</sub> < 6.5V,<br>0mA < I <sub>OUT</sub> < I <sub>MAX</sub> | 2.7  | 2.85 | 3.0 | V     |
| Short circuit current           |                   |   |      |      |     |       |
| LDO_A                           | I <sub>MAXA</sub> |   |      | 310  |     | mA    |
| LDO_B                           | I <sub>MAXB</sub> |   |      | 220  |     | mA    |
| LDO_C                           | I <sub>MAXC</sub> |   |      | 170  |     | mA    |
| Load Current                    |                   |   |      |      |     |       |
| LDO_A                           | I <sub>OUTA</sub> |   | 0    |      | 100 | mA    |
| LDO_B                           | I <sub>OUTB</sub> |   | 0    |      | 70  | mA    |
| LDO_C                           | I <sub>OUTC</sub> |   | 0    |      | 50  | mA    |
| Line regulation                 |                   | 1Vpp at V <sub>CC</sub> , max. load   |      | 1.1  | 10  | mV    |
| Load regulation                 |                   | 0mA < I <sub>OUT</sub> < I <sub>MAX</sub>                                   |      |      |     |       |
| LDO_A                           |                   |   |      | 9    | 45  | mV    |
| LDO_B                           |                   |   |      | 6    | 31  | mV    |
| LDO_C                           |                   |   |      | 5    | 22  | mV    |
| Load transient                  |                   | T <sub>AMB</sub> = 25°C   |      |      |     |       |
|                                 |                   | 10uA to ½ load in 1us (4)   |      | -60  |     | mV    |
|                                 |                   | 100uA to max. Load in 1us (4)   |      | -70  |     | mV    |
|                                 |                   | 10uA to max. Load in 1us (5)  |      | -85  |     | mV    |
| PSRR                            |                   | f ≤ 10kHz, 1Vpp at V <sub>CC</sub> = 4.5V<br>C <sub>REF</sub> = 10nF        | 50   | 60   |     | dB    |
| Quiescent current per regulator |                   | (3)   |      |      |     |       |
|                                 | I <sub>QR</sub>   | ON, max. load   |      | 170  |     | uA    |
|                                 | I <sub>QR</sub>   | ON, I <sub>OUT</sub> = 100uA  |      | 150  |     | uA    |
|                                 | I <sub>QR</sub>   | OFF   |      | <1   |     | uA    |
| Total quiescent current         | I <sub>Q</sub>    | ENA = ENBC = 0V<br>I <sub>OUT</sub> = 0 V <sub>CC</sub> = 6.5V              |      | <1   | 30  | μA    |
| Noise                           |                   |   |      |      |     |       |
|                                 |                   | 10Hz < f < 100kHz<br>typical load, no capacitor at VREF                     |      | 190  |     | uVrms |
|                                 |                   | 10Hz < f < 100kHz<br>typical load, 10nF cap. at VREF                        |      | 50   |     | uVrms |
| Settling time                   |                   | Enables OFF to ON<br>2.7V < V <sub>OUT</sub> < 3.0V<br>10nF cap. at VREF    |      | 0.5  | 1.0 | ms    |
| Output capacitor                |                   |   |      |      |     |       |
|                                 | C <sub>OUT</sub>  |   | 0.8  | 1.0  | 2.6 | uF    |
|                                 | ESR               |   | 0.01 | 0.1  | 1   | Ohm   |

NOTE 3: To get the real quiescent current of the device, the quiescent current of the reference voltage generator (140uA typ.) has to be added together once for all regulators.

 NOTE 4: V<sub>OUT</sub> does not drop below 2.7V for more than 1us.

 NOTE 5: V<sub>OUT</sub> does not drop below 2.5V for more than 1us or below 2.7V for more than 50us.

## FUNCTIONS

### ◆ Supply Voltage, Voltage Regulators

The device is supplied with 3.1V to 6.5V battery voltage under normal conditions. An internal band gap voltage reference is used to generate the reference voltage for all three voltage regulators. The reference voltage is routed via an internal 20kOhm Resistor to an external pin where a filter capacitor can be connected in order to reduce the noise level of all three regulators. The startup time of the reference voltage is then determined by the value of the bypass capacitor at pin VREF.

### ◆ Enable Pins

Each regulator can be enabled/disabled by the two enable pins ENA and ENBC. Pin ENA controls regulator LDO\_A and pin ENBC controls both regulators LDO\_B and LDO\_C. If both enable pins are forced low, the internal voltage reference and

internal bias source are turned off in order to save power. A common enable for all three regulator outputs is designed, but connected to VDD internally for the SOIC8 version of MAS9128A.

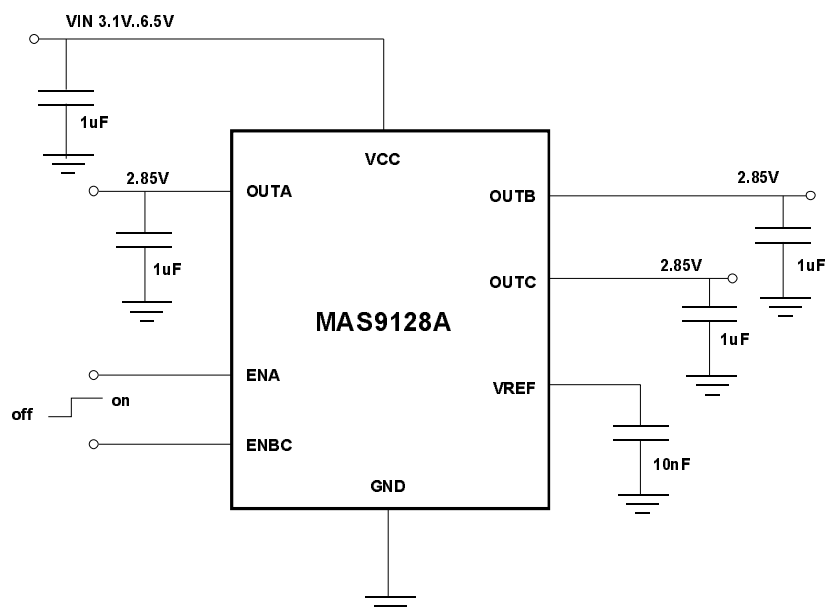
### ◆ Regulators

The device contains three 2.85V low dropout CMOS regulators with maximum output currents of 100mA, 70mA and 50mA. There is a mask option to modify the output voltage to 2.55V, 2.70V, 2.85V, 3.00V or 3.15V. The IC has thermal protection in order to prevent thermal destruction especially at high ambient temperatures. Maximum output current of each regulator is limited by an internal circuitry. The regulation loop of the regulators is optimized to work with low ESR ceramic buffer capacitors at the output.

Logic table for Enable inputs

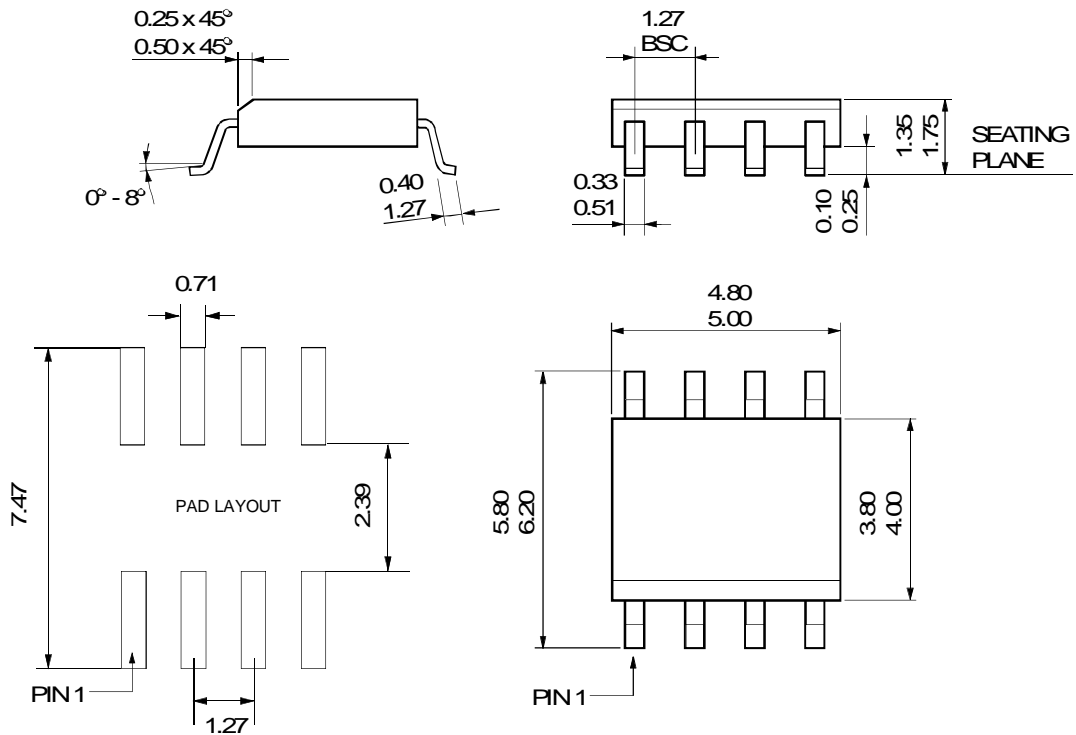
| ENA | ENBC | LDO_A | LDO_B | LDO_C | VREF |
|-----|------|-------|-------|-------|------|
| 1   | 1    | ON    | ON    | ON    | ON   |
| 1   | 0    | ON    | OFF   | OFF   | ON   |
| 0   | 1    | OFF   | ON    | ON    | ON   |
| 0   | 0    | OFF   | OFF   | OFF   | OFF  |

## APPLICATION INFORMATION

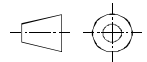


**PACKAGE OUTLINES AND RECOMMENDED LAND PATTERN**

**8 LEAD SO OUTLINE**



ALL MEASUREMENTS IN mm



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**ORDERING INFORMATION**


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|-------------|--------------------------|----------|---------------|
|             |                          | <b>k</b> |               |
| MAS9128AS   | LDO Voltage Regulator IC | SO8      |               |
| MAS9128AS-T | LDO Voltage Regulator IC | SO8      | Tape and Reel |

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**MICRONAS CONTACTS**


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|   |  |
|---|--|
| Micronas Semiconductor GmbH<br>Lohweg 29<br>D-85375 NEUFAHRN, GERMANY | Tel. (08165) 9521 0<br>Tel. Int. + 49 8165 9521 0<br>Telefax + 49 8165 9521 99 |
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|  |   |
|--|---|
| Micronas Semiconductor SA<br>Ch. Chapons-des-Prés<br>CH-2022 BEVAIX, SWITZERLAND | tel. (032) 847 0111<br>Tel. Int. +41 32 847 0111<br>Telefax +41 32 846 1930 |
|--|---|

|   |   |
|---|---|
| Micronas Oy<br>Kamreerintie 2, P.O.Box 51<br>FIN-02771 ESPOO, FINLAND | Tel. (09) 80521<br>Tel. Int. +358 9 80521<br>Telefax +358 9 8053213 |
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**End of Data Sheet**