NEC

MOS INTEGRATED CIRCUIT

μPD16337

64-BIT AC-PDP DRIVER

The μPD16337 is a high-voltage CMOS driver designed for flat display panels such as PDPs, VFDs and ELs. It consists of a 64-bit bi-directional shift register (16 bit × 4 circuits), 64-bit latch and high-voltage CMOS driver. The logic block is designed to operate at 5-V power supply, enabling direct connection to a microcontroller. In addition, the μPD16337 achieves low power dissipation by employing CMOS structure while having a high withstand voltage output (150 V, 40 mA MAX.)

FEATURES

- Built in four 16-bit bi-directional shift register circuits
- Data control with transfer clock (external) and latch
- High-speed data transfer ($f_{max.}$ = 20 MHz MIN. at cascade connection)
- Wide operating temperature range (T_A = –40 to +85°C)
- High withstand output voltage (150 V, 40 mA MAX.)
- 5-V CMOS input interface
- High withstand voltage CMOS structure
- Capable of reversing all driver outputs by PC pin

ORDERING INFORMATION

Part Number	Package
μPD16337GF-3BA	100-pin plastic QFP

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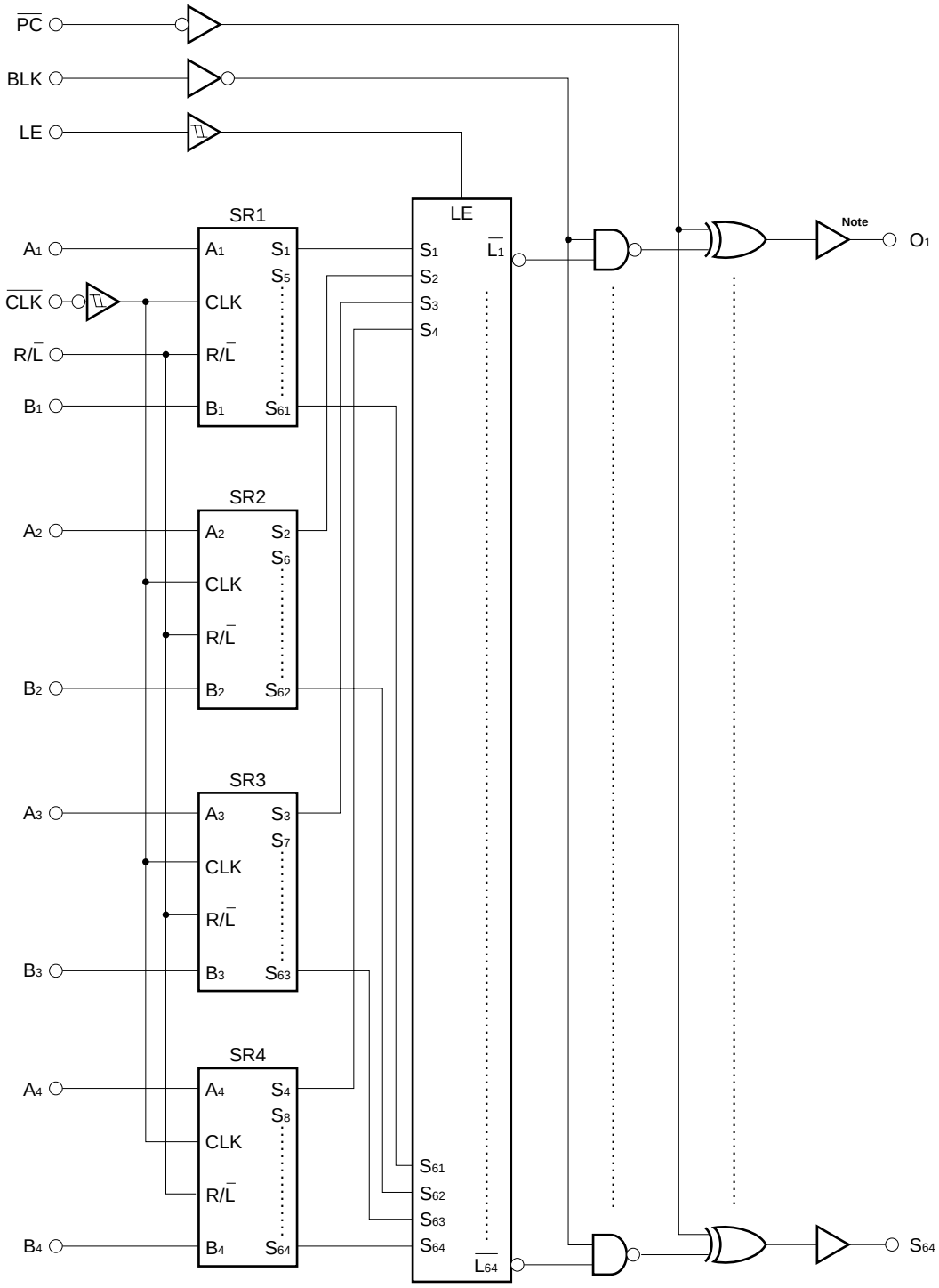
Printed in Japan

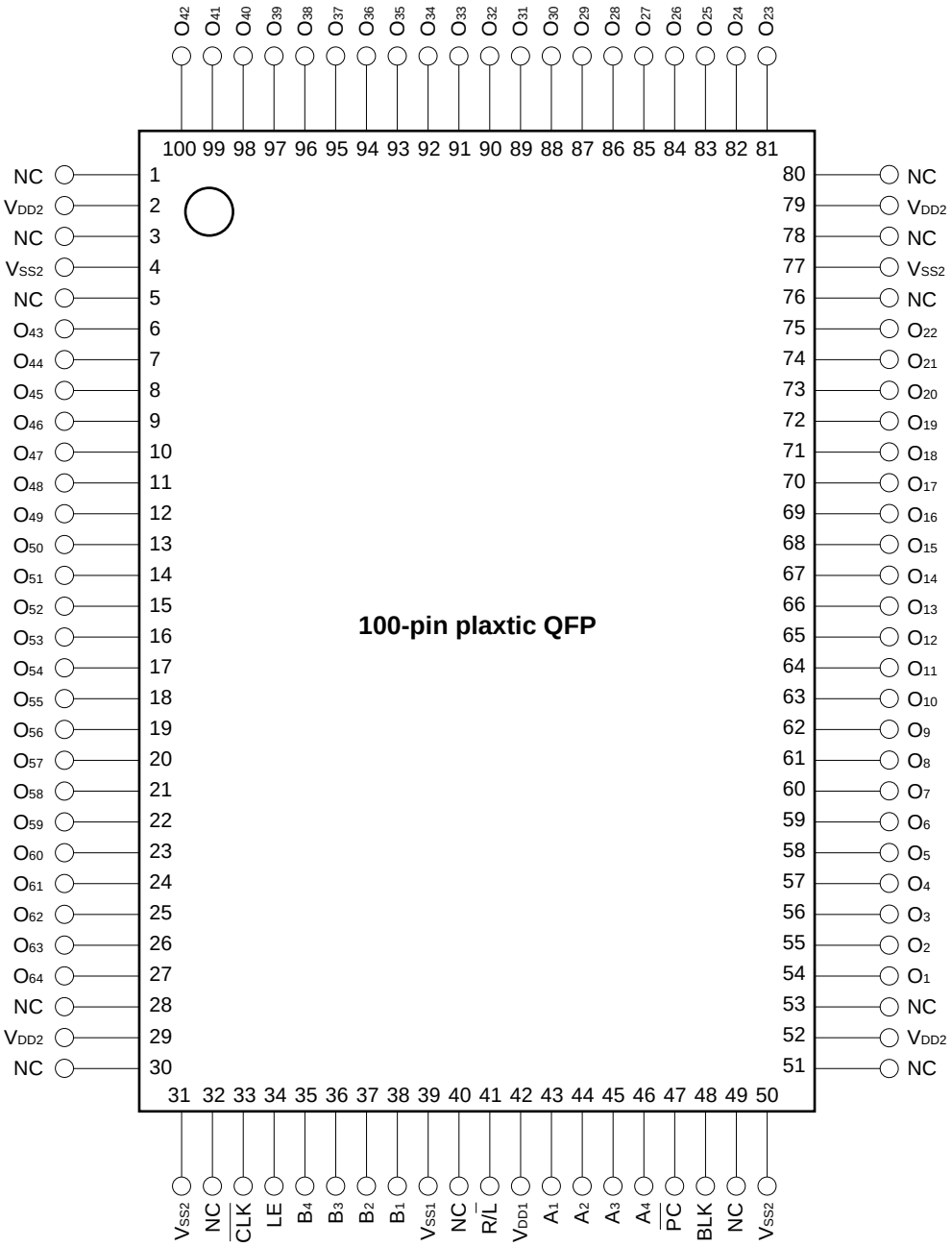
BLOCK DIAGRAM



SRn: 16-bit shift register

Note High withstand voltage CMOS driver, 150 V, ±40 mA (MAX.)

PIN CONFIGURATION (Top View)



Cautions

1. **Pin 40 is connected to the lead frame, and therefore must be left open.**
2. **Ensure that the V_{DD1}, V_{DD2}, V_{SS1} and V_{SS2} pins are all used, and that V_{SS1} and V_{SS2} are used at the same potential.**
3. **To prevent latch up breakdown, the power should be turned on in the order V_{DD1}, logic signal, V_{DD2}. It should be turned off in the opposite order.**

PIN DESCRIPTION

Symbol	Pin Name	Pin Number	Description
$\overline{PC}$	Polarity change input	47	$\overline{PC}$ = L: All driver output invert
BLK	Blank input	48	BLK = H: All output = H or L
LE	Latch enable input	34	Automatically executes latch by setting High at rising edge of the clock
A_1 to A_4	RIGHT data input/output	43 to 46	When R/$\overline{L}$ = H, A_1 to A_4: Input B_1 to B_4: Output
B_1 to B_4	LEFT data input/output	38 to 35	When R/$\overline{L}$ = L, A_1 to A_4: Output B_1 to B_4: Input
$\overline{CLK}$	Clock input	33	Shift executed on fall
R/$\overline{L}$	Shift control input	41	Right shift mode when R/L = H SR_1: $A_1 \rightarrow S_1 \cdots S_{61} \rightarrow B_1$ (Same direction for $SR_2 \cdot SR_4$) Left shift mode when R/L = L SR_1: $B_1 \rightarrow S_{61} \cdots S_1 \rightarrow A_1$ (Same direction for $SR_2 \cdot SR_4$)
O_1 to O_{64}	High withstand voltage output	54 to 75, 81 to 100, 6 to 27	130 V, 40 mA MAX.
V_{DD1}	Power supply for logic block	42	5 V ±10%
V_{DD2}	Power supply for driver block	2, 29, 52, 79	30 to 130 V
V_{SS1}	Logic GND	39	Connect to system GND
V_{SS2}	Driver GND	4, 31, 50, 77	Connect to system GND
NC	Non-connection	1, 3, 5, 28, 30, 32, 40, 49, 51, 53, 76, 78, 80	Non-connection Ensure that pin 40 is left open.

TRUTH TABLE 1 (Shift Register Block)

Input		Output		Shift Register
R/$\overline{L}$	$\overline{CLK}$	A	B	
H	↓	Input	Output[Note 1]	Right shift execution
H	H or L		Output	Hold
L	↓	Output[Note 2]	Input	Left shift execution
L	H or L	Output		Hold

Notes 1. The data of S_{57}, S_{58}, S_{59}, S_{60} shifts to S_{61}, S_{62}, S_{63}, S_{64} and is output from B_1, B_2, B_3, B_4 at the falling edge of the clock, respectively.

2. The data of S_5, S_6, S_7, S_8 shifts to S_1, S_2, S_3, S_4 and is output from A_1, A_2, A_3, A_4 at the falling edge of the clock, respectively.

TRUTH TABLE 2 (Latch Block)

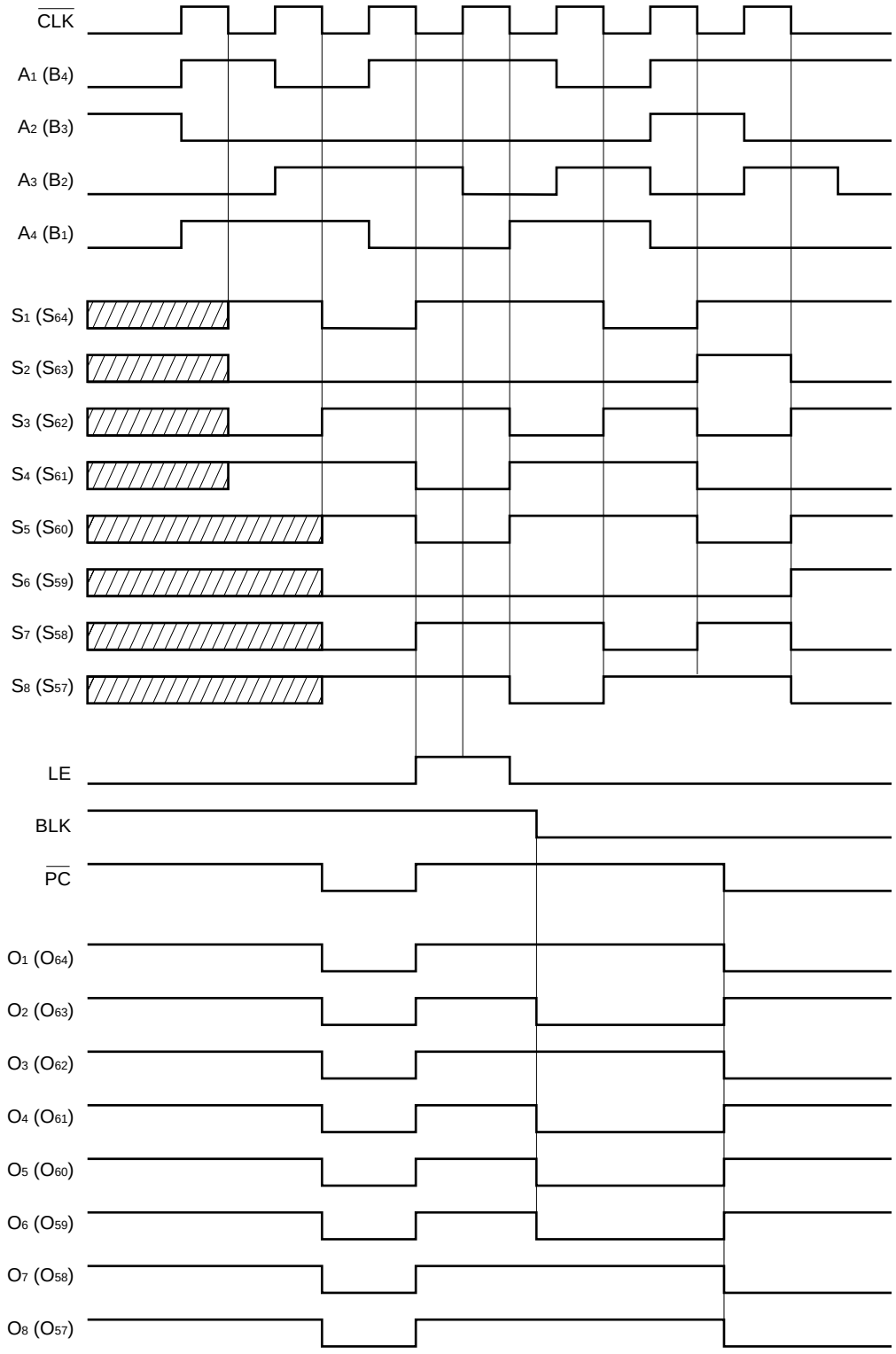
LE	$\overline{CLK}$	Output State of Latch Block ($\overline{L_n}$)
H	↑	Latch S_n data and hold output data
	↓	Hold latch data
L	×	Hold latch data

TRUTH TABLE 3 (Driver Block)

$\overline{L_n}$	BLK	$\overline{PC}$	Output State of Driver Block
×	H	H	H (All driver outputs: H)
×	H	L	L (All driver outputs: L)
×	L	H	Output latch data ($\overline{L_n}$)
×	L	L	Output reversed latch data ($\overline{L_n}$)

×: H or L, H: High level, L: Low level

TIMING CHART (Right shift)



Remark Values in parentheses in the above chart are when R/$\overline{L}$ = L.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic Block Supply Voltage	V_{DD1}	–0.5 to +7.0	V
Driver Block Supply Voltage	V_{DD2}	–0.5 to +150	V
Logic Block Input Voltage	V_I	–0.5 to V_{DD1} + 0.5	V
Driver Block Output Current	I_{O2}	40	mA
Input Current	I_I	±25	mA
Power Dissipation	P_D	1300**Note**	mW
Operating Ambient Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–65 to +150	°C

Note Derate at –13 mW/°C at T_A = 25°C or higher

RECOMMENDED OPERATING CONDITIONS (T_A = –40 to +85°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Block Supply Voltage	V_{DD1}	4.5	5.0	5.5	V
Driver Block Supply Voltage	V_{DD2}	30		130	V
High-Level Input Voltage	V_{IH}	0.7 V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}	0		0.2 V_{DD1}	V
Driver Output Current	I_{OH2}			–30	mA
	I_{OL2}			+30	mA

ELECTRICAL SPECIFICATIONS (T_A = 25°C, V_{DD1} = 5.0 V, V_{DD2} = 130 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-Level Output Voltage	V_{OH1}	Logic, I_{OH1} = –1.0 mA	0.9 V_{DD1}		V_{DD1}	V
Low-Level Output Voltage	V_{OL1}	Logic, I_{OL1} = 1.0 mA	0		0.1 V_{DD1}	V
High-Level Output Voltage	V_{OH21}	O_1 to O_{64}, I_{OH2} = –10 mA	123			V
	V_{OH22}	O_1 to O_{64}, I_{OH2} = –30 mA	110			V
Low-Level Output Voltage	V_{OL21}	O_1 to O_{64}, I_{OL2} = 10 mA			5.0	V
	V_{OL22}	O_1 to O_{64}, I_{OL2} = 30 mA			15	V
Input Leakage Current	I_{IL}	V_I = V_{DD1} or V_{SS1}			±1.0	μA
High-Level Input Voltage	V_{IH}		0.7 V_{DD1}			V
Low-Level Input Voltage	V_{IL}				0.2 V_{DD1}	V
Static Current Dissipation	I_{DD1}	Logic, T_A = –40 to +85°C			100	μA
	I_{DD1}	Logic, T_A = 25°C			10	μA
	I_{DD2}	Driver, T_A = –40 to +85°C			1000	μA
	I_{DD2}	Driver, T_A = 25°C			100	μA

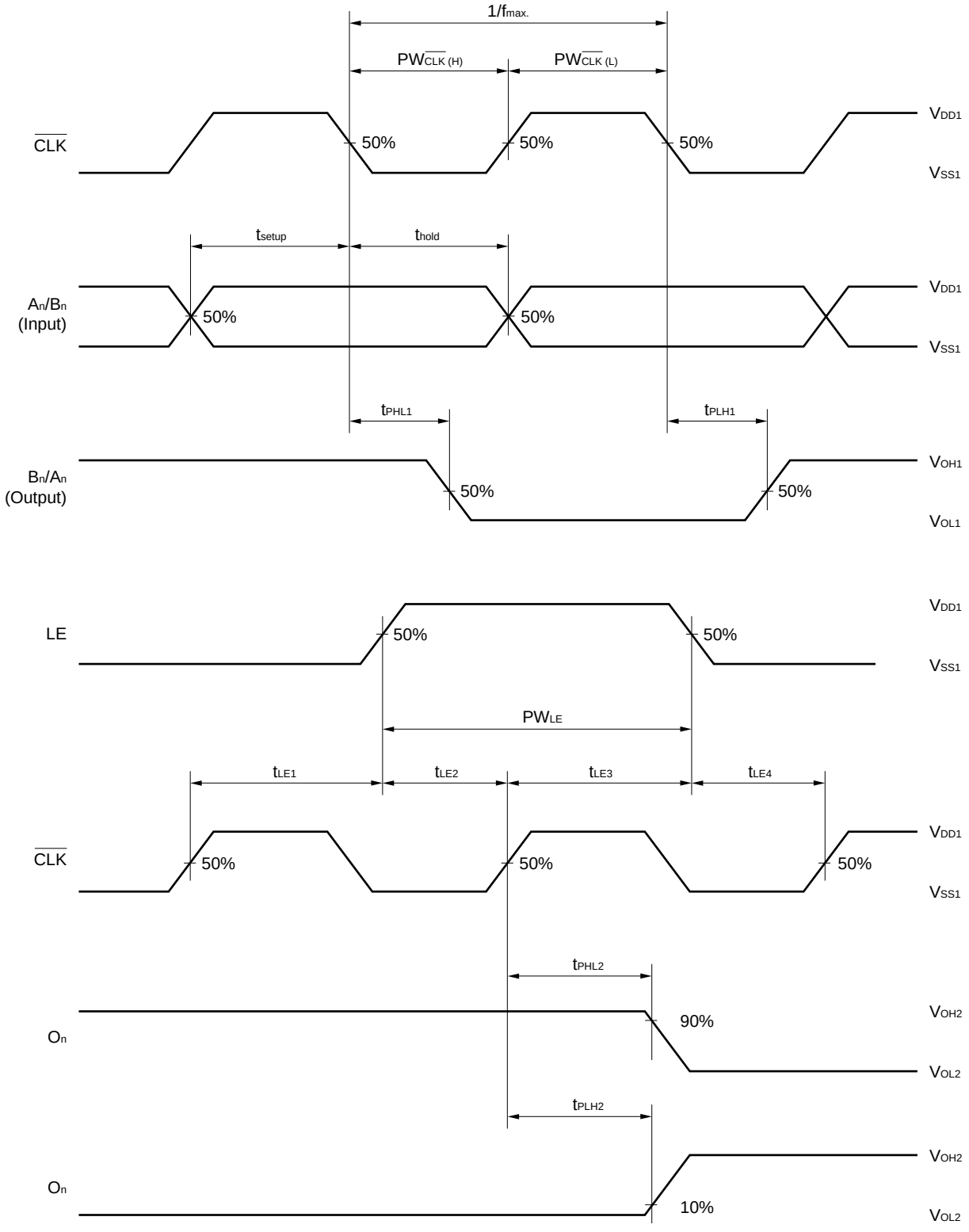
SWITCHING CHARACTERISTICS (T_A = 25°C, V_{DD1} = 5.0 V, V_{DD2} = 130 V, V_{SS1} = V_{SS2} = 0 V, logic C_L = 15 pF, driver C_L = 50 pF, t_r = t_f = 6.0 ns)

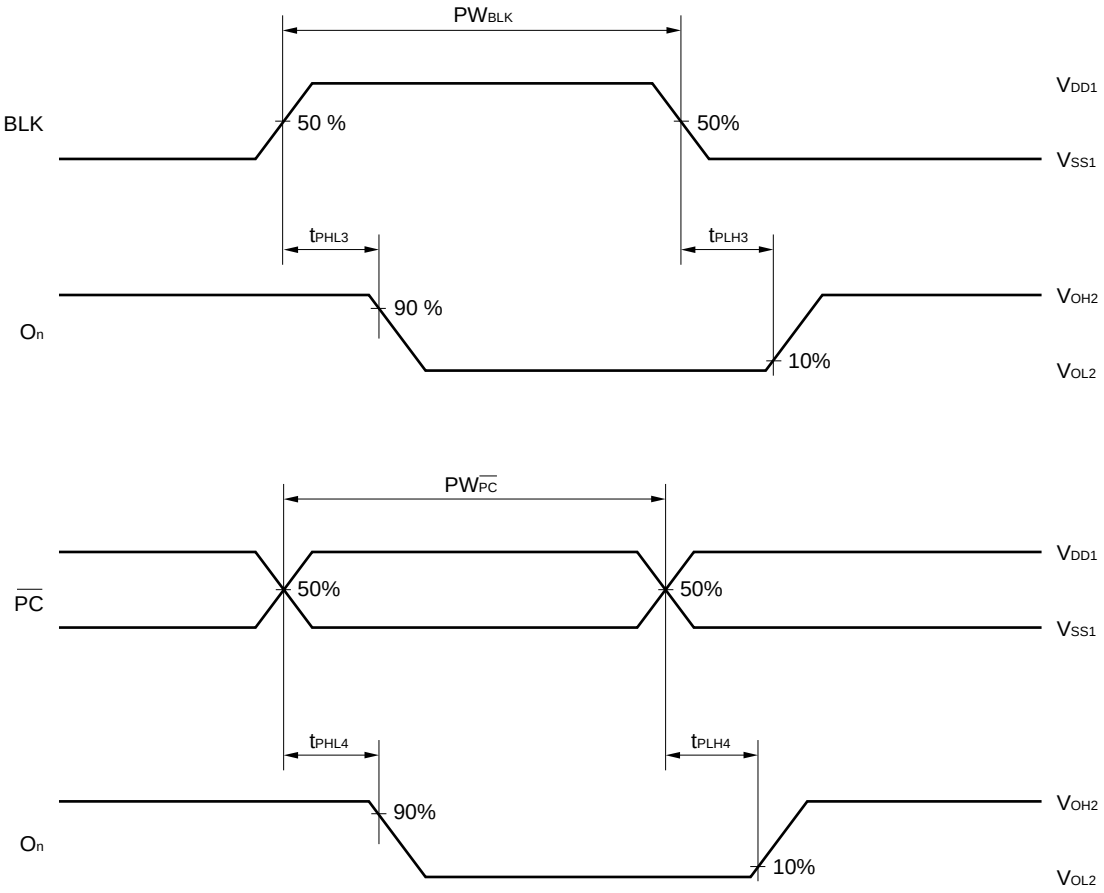
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transmission Delay Time	t_{PHL1}	$\overline{CLK}$ ↓ → A/B			40	ns
	t_{PLH1}				40	ns
	t_{PHL2}	$\overline{CLK}$ ↑ (LE = H) → O_1 to O_{64}			180	ns
	t_{PLH2}				180	ns
	t_{PHL3}	BLK → O_1 to O_{64}			165	ns
	t_{PLH3}				165	ns
	t_{PHL4}	$\overline{PC}$ → O_1 to O_{64}			160	ns
	t_{PLH4}				160	ns
Rise Time	t_{TLH}	O_1 to O_{64}			200	ns
Fall Time	t_{THL}	O_1 to O_{64}			200	ns
Maximum Clock Frequency	$f_{max.}$	When data is read, duty 50% T_A = –40 to +85°C V_{DD1} = 4.5 to 5.5 V	25			MHz
		When a cascade connection is made with a duty of 50% T_A = –40 to +85°C V_{DD1} = 4.5 to 5.5 V	20			MHz
Input Capacitance	C_I				15	pF

TIMMING REQUIREMENT (T_A = –40 to +85°C, V_{DD1} = 4.5 to 5.5 V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 6.0 ns)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	$PW_{\overline{CLK}}$		20			ns
Latch Enable Pulse Width	PW_{LE}		30			ns
Blank Pulse Width	PW_{BLK}		500			ns
$\overline{PC}$ Pulse Width	$PW_{\overline{PC}}$		500			ns
Data Setup Time	t_{setup}		10			ns
Data Hold Time	t_{hold}		10			ns
Latch Enable Time 1	t_{LE1}		20			ns
Latch Enable Time 2	t_{LE2}		10			ns
Latch Enable Time 3	t_{LE3}		20			ns
Latch Enable Time 4	t_{LE4}		10			ns

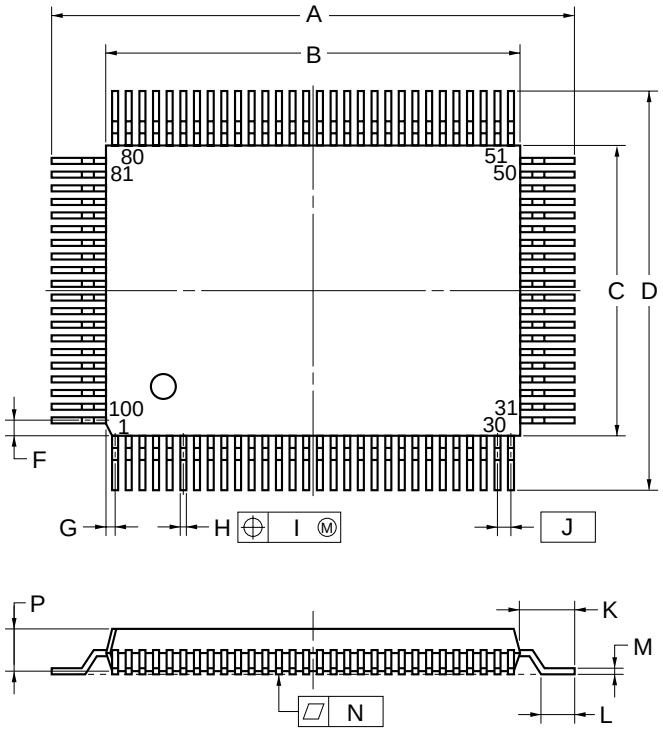
SWITCHING CHARACTERISTICS WAVEFORM

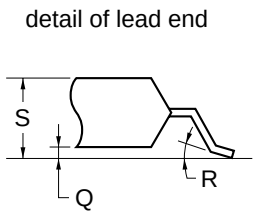



PWBLK
BLK
50 %
50%
VDD1
VSS1
tPHL3
tPLH3
On
90 %
10%
VOH2
VOL2
PWPC
PC
50%
50%
VDD1
VSS1
tPHL4
tPLH4
On
90%
10%
VOH2
VOL2

PACKAGE DRAWINGS

100 PIN PLASTIC QFP (14×20)





NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.2±0.2	$0.913^{+0.009}_{-0.008}$
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.2	0.677±0.008
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S100GF-65-3BA-3

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended below.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

SURFACE MOUNT TYPE

For details of recommended soldering conditions, refer to the information document **"Semiconductor Device Mounting Technology Manual" (C10535E)**.

μPD16337GF-3BA

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230°C, Duration: 30 sec. MAX. (at 210°C or above), Number of times: Twice, Time limit: None[Note]	IR30-00-2
VPS	Package peak temperature: 215°C, Duration: 40 sec. MAX. (at 200°C or above), Number of times: Twice, Time limit: None[Note]	VP15-00-2
Pin partial heating	Pin partial temperature: 300°C MAX., Duration: 10 sec. MAX., Time limit: None[Note]	

Note For the storage period after dry-pack decapsulation, storage conditions are max. 25°C, 65% RH.

Caution Use of more than one soldering method should be avoided (except in the case of pin partial heating).

REFERENCES

NEC Semiconductor Device Reliability/Quality Control System (IEI-1212)
Quality Grade on NEC Semiconductor Devices (C11531E)

[MEMO]

[MEMO]

[MEMO]