ACTT2X-800E

AC Thyristor Triac power switch

Rev. 2 — 26 October 2011 Product data sheet

1. Product profile

1.1 General description

Planar passivated AC Thyristor Triac power switch in a SOT186A (TO-220F) "full pack" plastic package with self-protective capabilities against low and high energy transients.

1.2 Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- Direct interfacing with low power drivers and microcontrollers
- Full cycle AC conduction
- Isolated mounting base package
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability
- Safe clamping capability for low energy over-voltage transients
- Self-protective turn-on during high energy voltage transients
- Sensitive gate for easy logic level triggering
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt

1.3 Applications

- AC Fan controllers
- Highly inductive, resistive and safety loads of lower power
- Large and small appliances (White Goods)
- Loads such as contactors, circuit breakers, valves, dispensers and door locks
- Pump motor circuits

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; see Figure 5; see Figure 6	-	-	14	A
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq$ 106 °C; see Figure 1; see Figure 2; see Figure 4	-	-	2	A

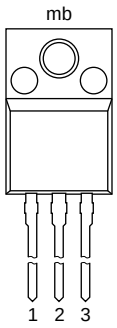
Table 1. Quick reference data *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; gate open circuit; exponential waveform; see Figure 13	500	-	-	V/µs
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; T_j = 25 °C	850	-	-	V
V_{PP}	peak pulse voltage	T_j = 25 °C; non-repetitive, off-state; see Figure 3	-	-	2	kV

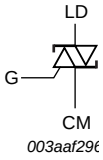
2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common		
2	LD	load		
3	G	gate		
mb	n.c.	mounting base; isolated		



SOT186A (TO-220F)



3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
ACTT2X-800E	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 106$ °C; see Figure 1; see Figure 2; see Figure 4	-	2	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms	-	15.4	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; see Figure 5; see Figure 6	-	14	A
I^2t	I^2t for fusing	$t_p = 10$ ms; sine-wave pulse	-	0.98	A^2s
dI_T/dt	rate of rise of on-state current	$I_T = 3$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs	-	100	A/µs
I_{GM}	peak gate current	t = 20 µs	-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	°C
T_j	junction temperature		-	125	°C
V_{PP}	peak pulse voltage	$T_j = 25$ °C; non-repetitive, off-state; see Figure 3	-	2	kV

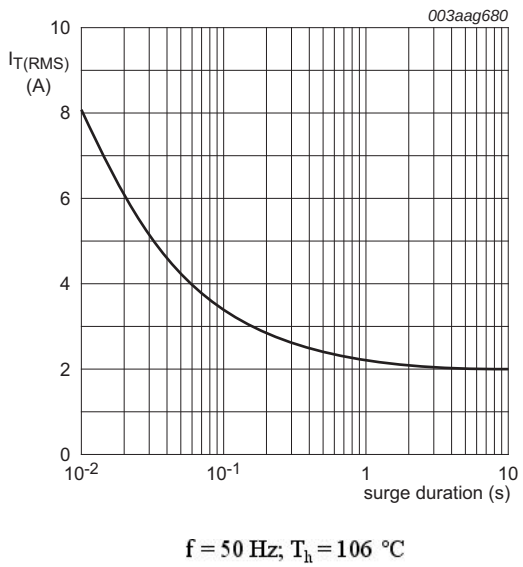


Fig 1. RMS on-state current as a function of surge duration; maximum values

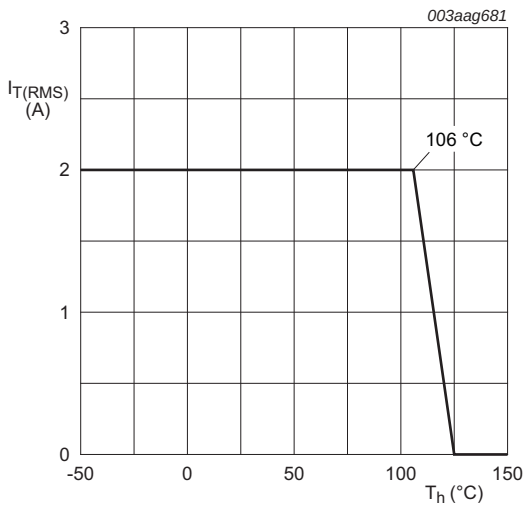


Fig 2. RMS on-state current as a function of heatsink temperature; maximum values

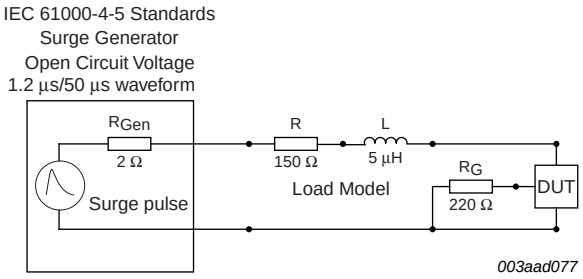
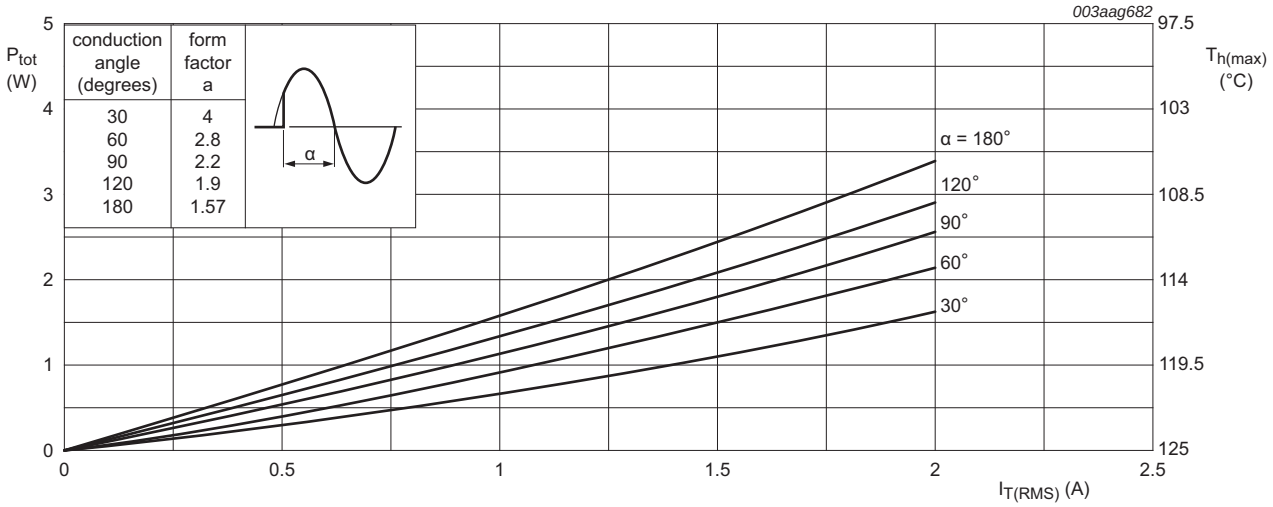


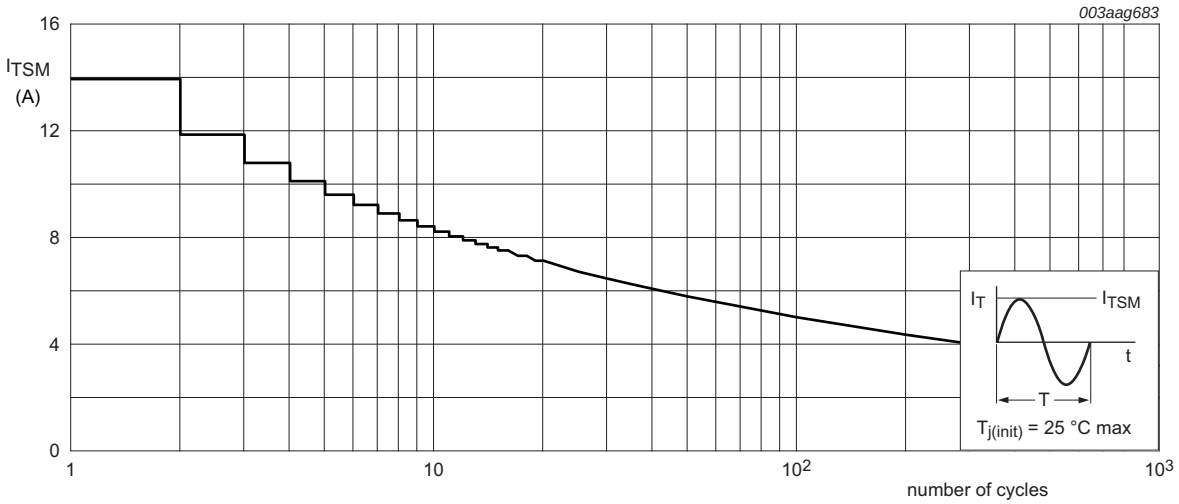
Fig 3. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5



α = conduction angle

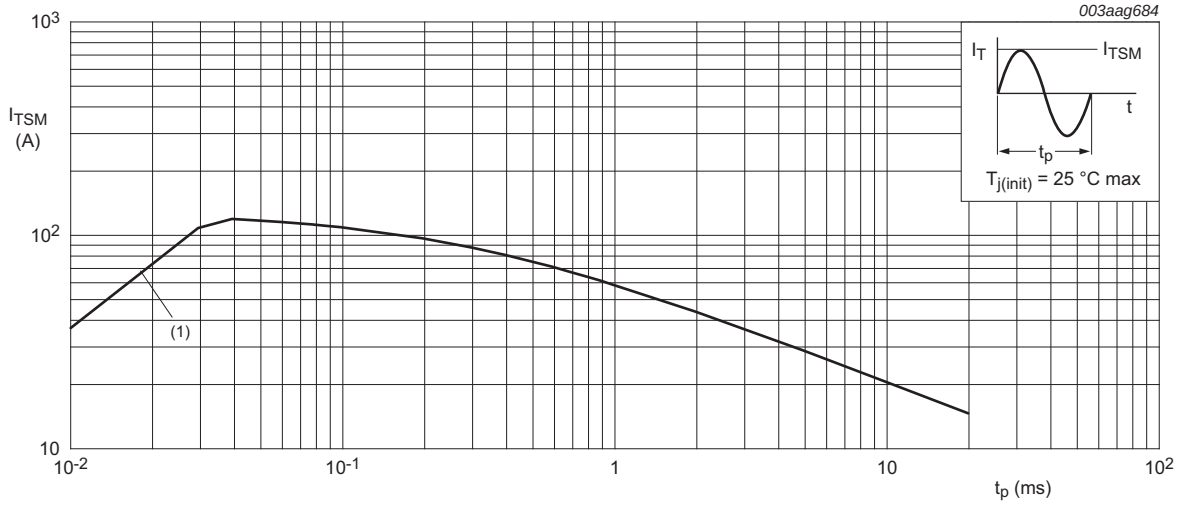
a = form factor = $I_{T(RMS)} / I_{T(AV)}$

Fig 4. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$ ms; (1) dI_T / d_t limit

Fig 6. Non-repetitive peak on-state current as a function of pulse width; maximum values

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	full or half cycle with heatsink compound; see Figure 7	-	-	5.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	55	-	K/W

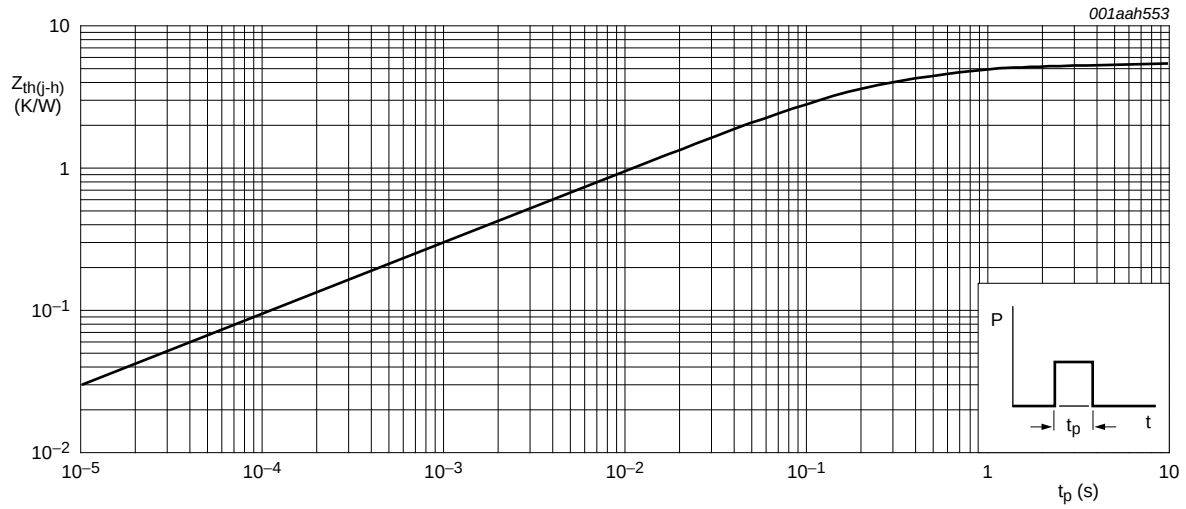


Fig 7. Transient thermal impedance from junction to heatsink as a function of pulse width

6. Isolation characteristics

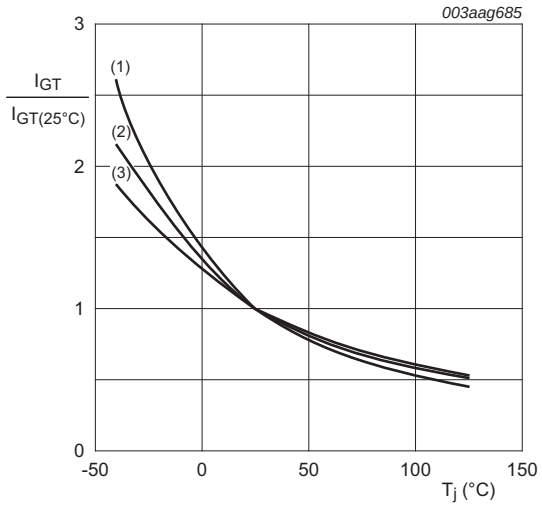
Table 6. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; T_h = 25 °C; sinusoidal waveform; from all pins to external heatsink; clean and dust free	-	-	2500	V
C_{isol}	isolation capacitance	T_h = 25 °C; from LD pin to external heatsink; f = 1 MHz	-	10	-	pF

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{GT}	gate trigger current	V_D = 12 V; I_T = 100 mA; LD+ G+; T_j = 25 °C; see Figure 8	-	-	10	mA
		V_D = 12 V; I_T = 100 mA; LD+ G-; T_j = 25 °C; see Figure 8	-	-	10	mA
		V_D = 12 V; I_T = 100 mA; LD- G-; T_j = 25 °C; see Figure 8	-	-	10	mA
I_L	latching current	V_D = 12 V; I_G = 100 mA; LD+ G+; T_j = 25 °C; see Figure 9	-	-	25	mA
		V_D = 12 V; I_G = 100 mA; LD+ G-; T_j = 25 °C; see Figure 9	-	-	35	mA
		V_D = 12 V; I_G = 100 mA; LD- G-; T_j = 25 °C; see Figure 9	-	-	25	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; see Figure 10	-	-	25	mA
V_T	on-state voltage	I_T = 3 A; T_j = 25 °C; see Figure 11	-	-	2	V
V_{GT}	gate trigger voltage	V_D = 400 V; I_T = 100 mA; T_j = 125 °C; see Figure 12	0.2	-	-	V
		V_D = 12 V; I_T = 100 mA; T_j = 25 °C; see Figure 12	-	-	1.5	V
I_D	off-state current	V_D = 800 V; T_j = 25 °C	-	-	10	µA
		V_D = 800 V; T_j = 125 °C	-	-	0.5	mA
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; gate open circuit; exponential waveform; see Figure 13	500	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 2 A; dV_{com}/dt = 10 V/µs; gate open circuit; see Figure 14; see Figure 15	3	-	-	A/ms
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; T_j = 25 °C	850	-	-	V



(1) LD− G−
(2) LD+ G+
(3) LD+ G−

Fig 8. Normalized gate trigger current as a function of junction temperature

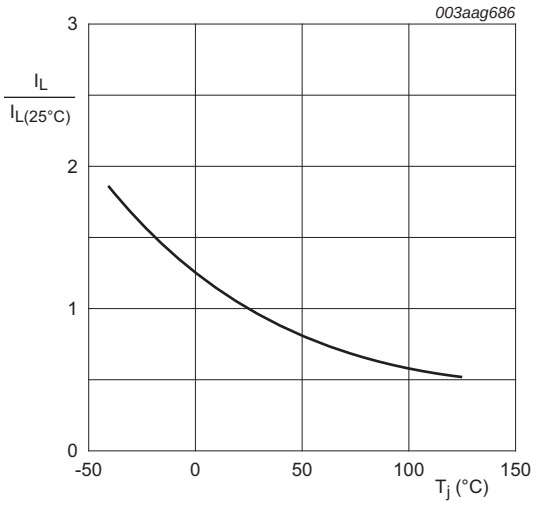


Fig 9. Normalized latching current as a function of junction temperature

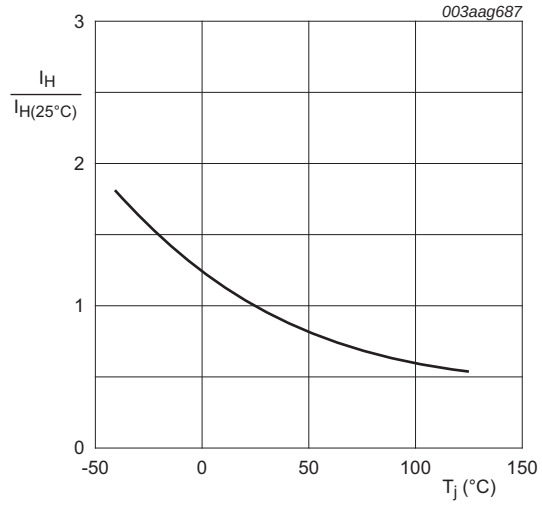
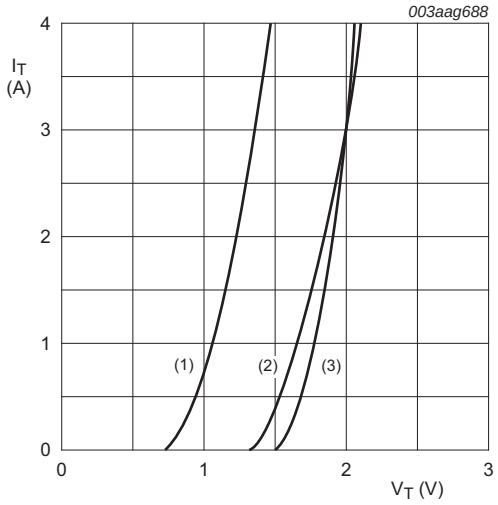


Fig 10. Normalized holding current as a function of junction temperature



$V_O = 1.612$ V; $R_S = 0.120$ Ω;
(1) $T_j = 125$ °C; typical values;
(2) $T_j = 125$ °C; maximum values;
(3) $T_j = 25$ °C; maximum values

Fig 11. On-state current as a function of on-state voltage

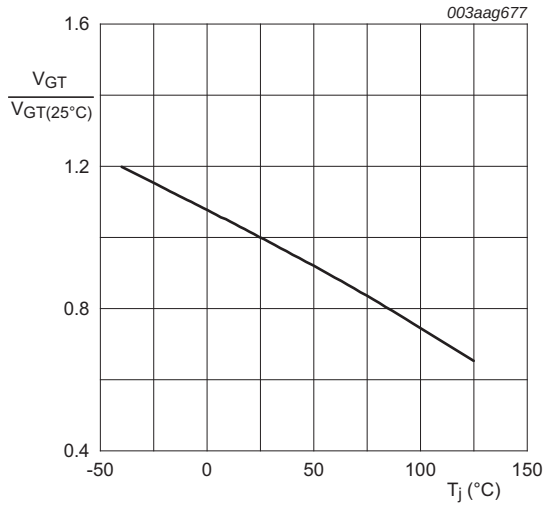
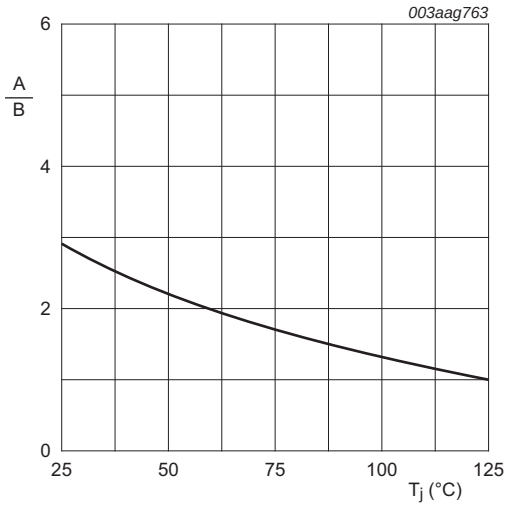
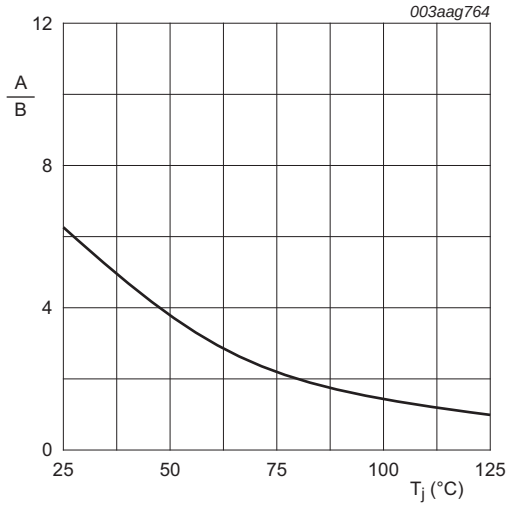


Fig 12. Normalized gate trigger voltage as a function of junction temperature



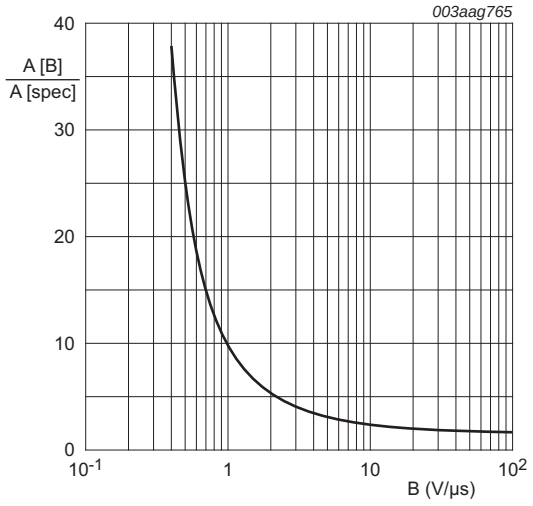
A is dV_D/dt at condition T_j °C
B is dV_D/dt at condition T_j 125 °C

Fig 13. Normalized rate of rise of off-state voltage as a function of junction temperature



A is dI_{com}/dt at condition T_j °C
B is dI_{com}/dt at condition T_j 125 °C
$V_D = 400$ V

Fig 14. Normalized critical rate of rise of commutating current as a function of junction temperature



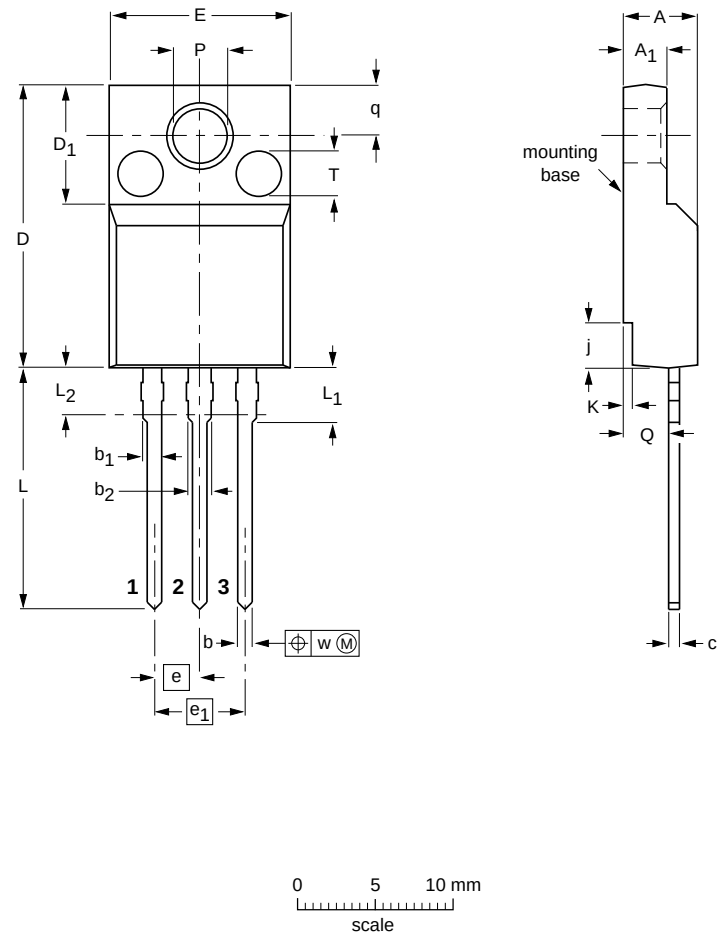
A[B] is dI_{com}/dt at condition B, dV_{com}/dt
A[spec] is the specified data sheet value of dI_{com}/dt
turn-off time less than 20 ms

Fig 15. Normalized critical rate of change of commutating current as a function of critical rate of change of commutating voltage; minimum values

8. Package outline

Plastic single-ended package; isolated heatsink mounted;
1 mounting hole; 3-lead TO-220 'full pack'

SOT186A



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j	K	L	L_1	L_2 (1) max.	P	Q	q	T (2)	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.0	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 1.7	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

Notes

1. Terminal dimensions within this zone are uncontrolled.
2. Both recesses are ∅ 2.5 × 0.8 max. depth

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3-lead TO-220F				~~02-04-09~~ 06-02-14

Fig 16. Package outline SOT186A (TO-220F)

9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ACTT2X-800E v.2	20111026	Product data sheet	-	ACTT2X-800E v.1
Modifications:	• Various changes to content.			
ACTT2X-800E v.1	20110919	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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12. Contents

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