10-Bit and 12-Bit, 1MSPS SAR ADCs

ISL267440, ISL267450A

The ISL267440 and ISL267450A are 10-bit and 12-bit, 1MSPS sampling SAR-type ADCs featuring excellent linearity over supply and temperature variations, which are drop-in compatible with the AD7440 and AD7450A. The robust, fully-differential input offers high impedance to minimize errors due to leakage currents, and the specified measurement accuracy is maintained with input signals up to the supply rails.

The reference accepts inputs from 0.1V to 2.2V for 3V operation and 0.1V to 3.5V for 5V operation, which provides design flexibility in a wide variety of applications. The ISL267440, ISL267450A also feature up to 8kV Human Body Model ESD survivability.

The serial digital interface is SPI compatible and is easily interfaced to all popular FPGAs and microcontrollers. Power dissipation is 8.5mW at a sampling rate of 1MSPS, and just 5µW between conversions utilizing Auto Power-Down mode (with a 5V supply), making the ISL267440, ISL267450A excellent solutions for remote industrial sensors and battery-powered instruments.

The ISL267440, ISL267450A are available in an 8 lead MSOP package, and are specified for operation over the Industrial temperature range (–40°C to +85°C).

Features

- Drop-in Compatible with AD7440, AD7450A
- Differential Input
- Simple SPI-compatible Serial Digital Interface
- Guaranteed No Missing Codes
- 1MHz Sampling Rate
- 3V or 5V Operation
- Low Operating Current
  - 1.25mA at 1MSPS with 3V Supplies
  - 1.70mA at 1MSPS with 5V Supplies
- Power-down Current between Conversions: 1µA
- Excellent Differential Non-Linearity
- Low THD: -83dB (typ)
- Pb-Free (RoHS Compliant)
- Available in MSOP Package

Applications

- Remote Data Acquisition
- Battery Operated Systems
- Industrial Process Control
- Energy Measurement
- Data Acquisition Systems
- Pressure Sensors
- Flow Controllers

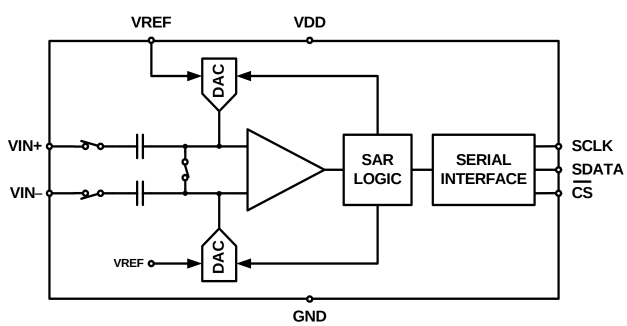


FIGURE 1. BLOCK DIAGRAM

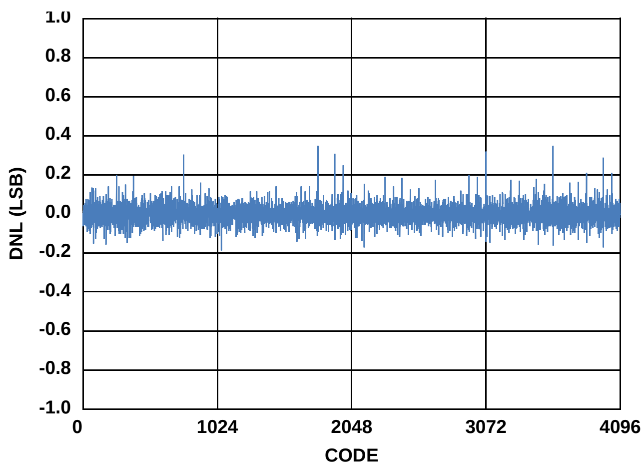
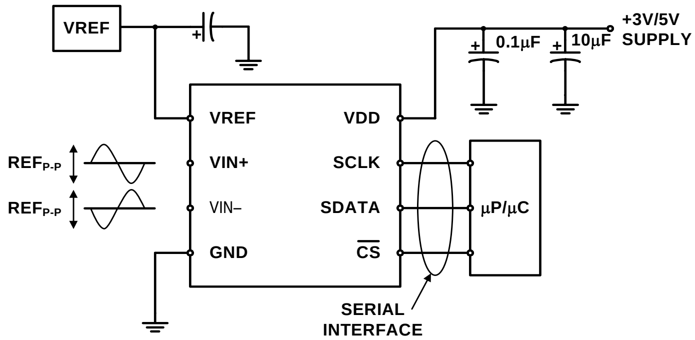


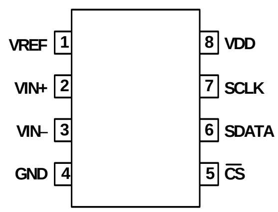
FIGURE 2. DIFFERENTIAL LINEARITY ERROR vs CODE

Typical Connection Diagram



Pin Configuration

ISL267440, ISL267450A
(8 LD MSOP)
TOP VIEW



Pin Descriptions

ISL267440, ISL267450A		
PIN NAME	PIN NUMBER	DESCRIPTION
VDD	8	Supply voltage, +2.7V to 5.25V.
SCLK	7	Serial clock input. Controls digital I/O timing and clocks the conversion.
SDATA	6	Digital conversion output.
$\overline{CS}$	5	Chip select input. Generally controls the start of a conversion though not always the sampling signal.
GND	4	Ground
VIN–	3	Negative analog input.
VIN+	2	Positive analog input.
VREF	1	Reference voltage.

Ordering Information

PART NUMBER (Note 4)	PART MARKING	V_{DD} RANGE (V)	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
ISL267440IUZ (Note 3)	67440	2.7 to 5.25	-40°C to +85°C	8 Ld MSOP	M8.118
ISL267440IUZ-T (Notes 1, 3)	67440	2.7 to 5.25	-40°C to +85°C	8 Ld MSOP	M8.118
ISL267440IUZ-T7A (Notes 1, 3)	67440	2.7 to 5.25	-40°C to +85°C	8 Ld MSOP	M8.118
ISL267450AIUZ (Note 3)	7450A	2.7 to 5.25	-40°C to +85°C	8 Ld MSOP	M8.118
ISL267450AIUZ -T (Notes 1, 3)	7450A	2.7 to 5.25	-40°C to +85°C	8 Ld MSOP	M8.118
ISL267450AIUZ -T7A (Notes 1, 3)	7450A	2.7 to 5.25	-40°C to +85°C	8 Ld MSOP	M8.118
Coming Soon ISL267440IHZ-T (Notes 1, 2)	7440	2.7 to 5.25	-40°C to +85°C	8 Ld SOT-23	P8.064
Coming Soon ISL267440IHZ-T7A (Notes 1, 2)	7440	2.7 to 5.25	-40°C to +85°C	8 Ld SOT-23	P8.064
Coming Soon ISL267450AIHZ-T (Notes 1, 2)	450A	2.7 to 5.25	-40°C to +85°C	8 Ld SOT-23	P8.064
Coming Soon ISL267450AIHZ-T7A (Notes 1, 2)	450A	2.7 to 5.25	-40°C to +85°C	8 Ld SOT-23	P8.064

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate -e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL267440 or ISL267450A. For more information on MSL please see techbrief TB363.

Table of Contents

Absolute Maximum Ratings

Any Pin to GND . . . . -0.3V to +6.0V
Analog Input to GND. . . . . -0.3V to V_{DD}+0.3V
Digital I/O to GND. . . . . -0.3V to V_{DD}+0.3V
Digital Input Voltage to GND . . . . -0.3V to V_{DD}+0.3V
Maximum Current In to Any Pin 10mA
ESD Rating
  Human Body Model (Tested per JESD22-A114F). 8kV
  Machine Model (Tested per JESD22-A115B) 400V
  Charged Device Model (Tested per JESD22-C101E). 1.5kV
Latch Up (Tested per JESD78C; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld MSOP Package (Notes 5, 6).	165	64
8 Ld SOT-23 Package (Notes 5, 6).	135	99

Operating Temperature . . . . -40°C to +85°C
Storage Temperature . . . . -65°C to +150°C
Junction Temperature . . . . +150°C
Pb-Free Reflow Profile . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

V_{DD} = +3.0V to +3.6V, f_{SCLK} = 18MHz, f_S = 1MSPS, V_{REF} = 2.0V; V_{DD} = +4.75V to +5.25V, f_{SCLK} = 18MHz, f_S = 1MSPS, V_{REF} = 2.5V; V_{CM} = V_{REF}, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	ISL267440			ISL267450A			UNITS
			MIN (Note 7)	TYP	MAX (Note 7)	MIN (Note 7)	TYP	MAX (Note 7)	
DYNAMIC PERFORMANCE									
SINAD	Signal-to (Noise + Distortion) Ratio	f_{IN} = 100kHz V_{DD} = +4.75V to +5.25V	**61.0**	61.6		**70.0**	71.4		dB
		f_{IN} = 100kHz V_{DD} = +3.0V to +3.6V	**60.7**	61.5		**68.5**	70.5		
THD	Total Harmonic Distortion	f_{IN} = 100kHz V_{DD} = +4.75V to +5.25V		-82	**-74**		-84	**-76**	dB
		f_{IN} = 100kHz V_{DD} = +3.0V to +3.6V		-80	**-72**		-84	**-74**	dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 100kHz V_{DD} = +4.75V to +5.25V		-82	**-76**		-87	**-76**	dB
		f_{IN} = 100kHz V_{DD} = +3.0V to +3.6V		-82	**-74**		-85	**-74**	dB
IMD	Intermodulation Distortion	2nd and 3rd order, f_{IN} = 90kHz, 110kHz		-92			-95		dB
tpd	Aperture Delay			1			1		ns
Δtpd	Aperture Jitter			15			15		ps
β3dB	Full Power Bandwidth	@ –3dB		15			15		MHz
DC ACCURACY									
N	Resolution		**10**			**12**			Bits
INL	Integral Nonlinearity		**-0.5**	±0.1	**0.5**	**-1**	±0.4	**1**	LSB
DNL	Differential Nonlinearity	Guaranteed no missed codes to 12 bits (ISL267450A) or 10 bits (ISL267440)	**-0.5**	±0.1	**0.5**	**-0.95**	±0.3	**0.95**	LSB
OFFSET	Zero-Code Error	Zero Volt Differential Input	**-2.5**	±0.2	**2.5**	**-6**	±0.2	**6**	LSB
GAIN	Positive Gain Error	± REF input range	**-1**	±0.1	**1**	**-2**	±0.1	**2**	LSB
	Negative Gain Error		**-1**	±0.1	**1**	**-2**	±0.1	**2**	
ANALOG INPUT (Note 8)									
|AIN|	Full-Scale Input Span	2 x V_{REF}		VIN+ - VIN–			VIN+ - VIN–		V

Electrical Specifications V_{DD} = +3.0V to +3.6V, f_{SCLK} = 18MHz, f_S = 1MSPS, V_{REF} = 2.0V; V_{DD} = +4.75V to +5.25V, f_{SCLK} = 18MHz, f_S = 1MSPS, V_{REF} = 2.5V; V_{CM} = V_{REF}, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	ISL267440 MIN (Note 7)	ISL267440 TYP	ISL267440 MAX (Note 7)	ISL267450A MIN (Note 7)	ISL267450A TYP	ISL267450A MAX (Note 7)	UNITS
VIN+, VIN–	Absolute Input Voltage Range	$V_{CM} = V_{REF}$							
	VIN+			$V_{CM}±V_{REF}/2$			$V_{CM}±V_{REF}/2$		
	VIN–			$V_{CM}±V_{REF}/2$			$V_{CM}±V_{REF}/2$		
I_{LEAK}	Input DC Leakage Current		**-1**		**1**	**-1**		**1**	µA
C_{VIN}	Input Capacitance	Track/Hold mode		13/5			13/5		pF
REFERENCE INPUT									
REF	REF Input Voltage Range	V_{DD} = 3V (1% tolerance for specified performance)		2.0			2.0		V
		V_{DD} = 5V (1% tolerance for specified performance)		2.5			2.5		V
I_{LEAK}	DC Leakage Current		**-1**		**1**	**-1**		**1**	µA
C_{REF}	REF Input Capacitance	Track/Hold mode		21/18.5			21/18.5		pF
LOGIC INPUTS									
V_{IH}	Input High Voltage		**2.4**			**2.4**			V
V_{IL}	Input Low Voltage				**0.8**			**0.8**	V
I_{LEAK}	Input Leakage Current		**-1**		**1**	**-1**		**1**	µA
C_{IN}	Input Capacitance			**10**			**10**		pF
LOGIC OUTPUTS									
V_{OH}	Output High Voltage	I_{SOURCE} = 200µA	**V_{DD} - 0.3**			**V_{DD} - 0.3**			V
V_{OL}	Output Low Voltage	I_{SINK} = 200µA			**0.4**			**0.4**	V
I_{OZ}	Floating-State Output Current		**-1**		**1**	**-1**		**1**	µA
C_{OUT}	Floating-State Output Capacitance			**10**			**10**		pF
	Output Coding		Two's Complement						
CONVERSION RATE									
t_{CONV}	Conversion Time	f_{SCLK} = 18MHz			**888**			**888**	ns
t_{ACQ}	Acquisition Time				**200**			**200**	ns
f_{max}	Throughput Rate				**1000**			**1000**	kSPS
POWER REQUIREMENTS									
V_{DD}	Positive Supply Voltage Range		**2.7**		**3.6**	**2.7**		**3.6**	V
			4.75		**5.25**	**4.75**		**5.25**	V
I_{DD}	Positive Supply Input Current								
	Static				**1**			**1**	µA
	Dynamic	3V			**1250**			**1250**	µA
		5V			**1700**			**1700**	µA
	Power Dissipation								
	Static Mode	V_{DD} = 3V			**3**			**3**	µW
		V_{DD} = 5V			**5**			**5**	µW
	Dynamic	V_{DD} = 3V, f_{smpl} = 1MSPS			**3.75**			**3.75**	mW
		V_{DD} = 5V, f_{smpl} = 1MSPS			**8.50**			**8.50**	mW

NOTES:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
8. The absolute voltage applied to each analog input must be between GND and V_{DD} to guarantee datasheet performance.

Timing Specifications

Limits established by characterization and are not production tested. V_{DD} = 3.0V to 3.6V, f_{SCLK} = 18MHz, f_S = 1MSPS, V_{REF} = 2.0V; V_{DD} = 4.75V to 5.25V, f_{SCLK} = 18MHz, f_S = 1MSPS, V_{REF} = 2.5V; V_{CM} = V_{REF} unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
f_{SCLK}	Clock Frequency		**0.01**		**18**	MHz
t_{SCLK}	Clock Period		**55**			ns
t_{ACQ}	Acquisition Time				**200**	ns
t_{CONV}	Conversion Time				**888**	ns
t_{CSW}	$\overline{CS}$ Pulse Width		**10**			ns
t_{CSS}	$\overline{CS}$ Falling Edge to S_{CLK} Falling Edge Setup Time		**10**			ns
t_{CDV}	$\overline{CS}$ Falling Edge to SDATA Valid				**20**	ns
t_{CLKDV}	SCLK Falling Edge to SDATA Valid				**40**	ns
t_{SDH}	SCLK Falling Edge to SDATA Hold		**10**			ns
t_{SW}	SCLK Pulse Width		**0.4 x t_{SCLK}**			ns
$t_{DISABLE}$	SCLK Falling Edge to SDATA Disable Time (Note 9)	Extrapolated back to true bus relinquish	**10**		**35**	ns
t_{QUIET}	Quiet Time Before Sample		**60**			ns

NOTE:

9. During characterization, $t_{DISABLE}$ is measured from the release point with a 10pF load (see Figure 4) and the equivalent timing using the AD7440/450A loading (25pF) is calculated.

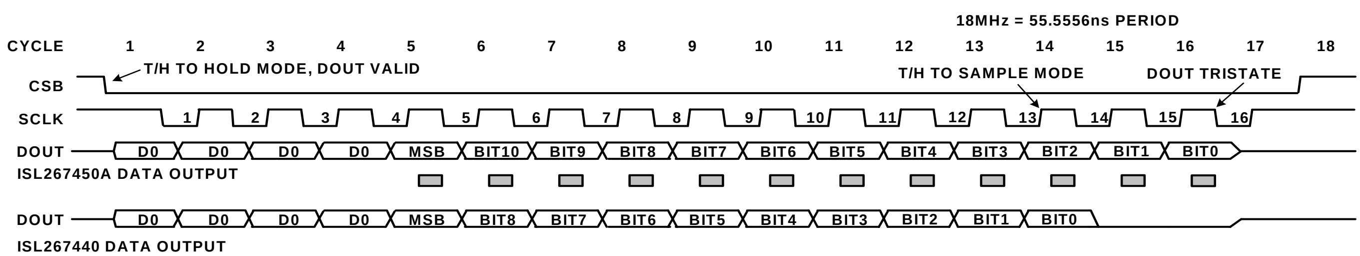


FIGURE 3. SERIAL INTERFACE TIMING DIAGRAM

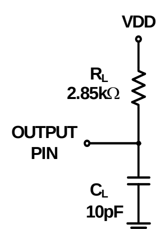


FIGURE 4. EQUIVALENT LOAD CIRCUIT

Typical Performance Characteristics

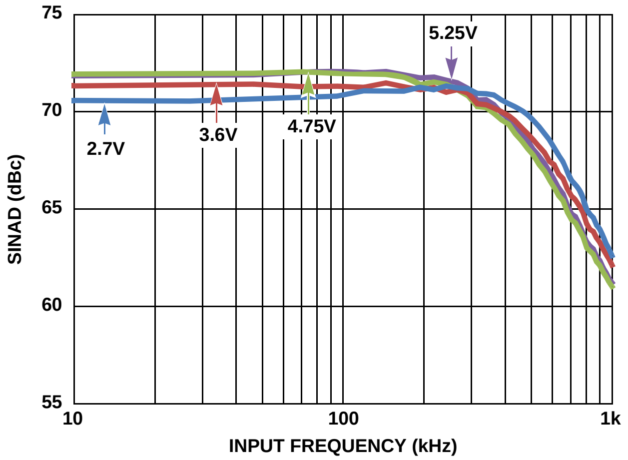


FIGURE 5. ISL267450A SINAD vs ANALOG INPUT FREQUENCY FOR VARIOUS SUPPLY VOLTAGES

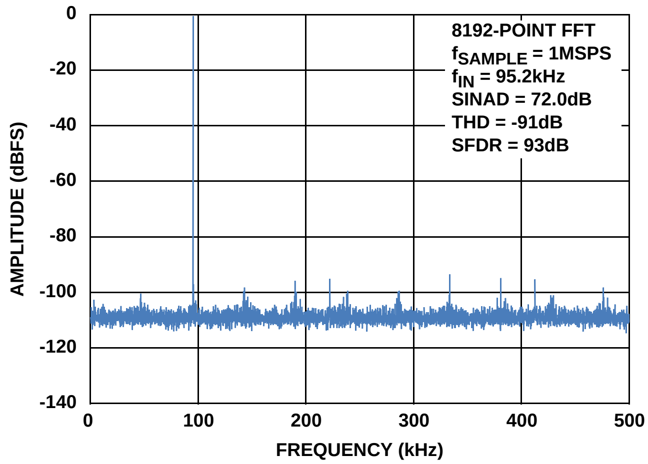


FIGURE 6. ISL267450A DYNAMIC PERFORMANCE WITH V_{DD} = 5V

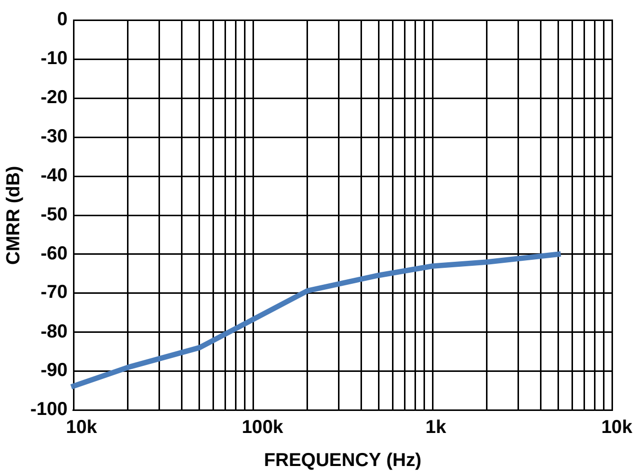


FIGURE 7. CMRR vs FREQUENCY FOR V_{DD} = 5V

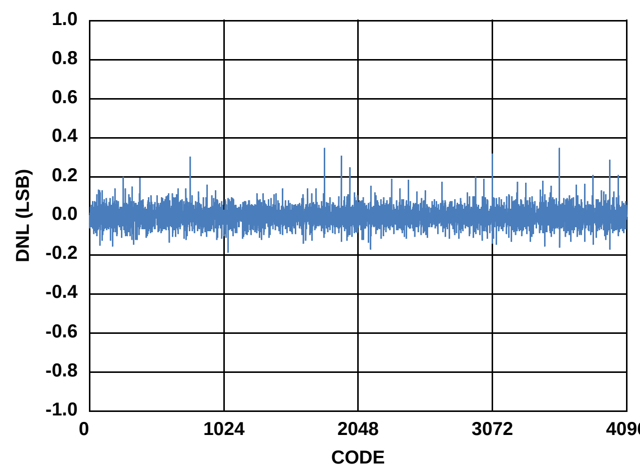


FIGURE 8. TYPICAL DNL FOR THE ISL267450A FOR V_{DD} = 5V

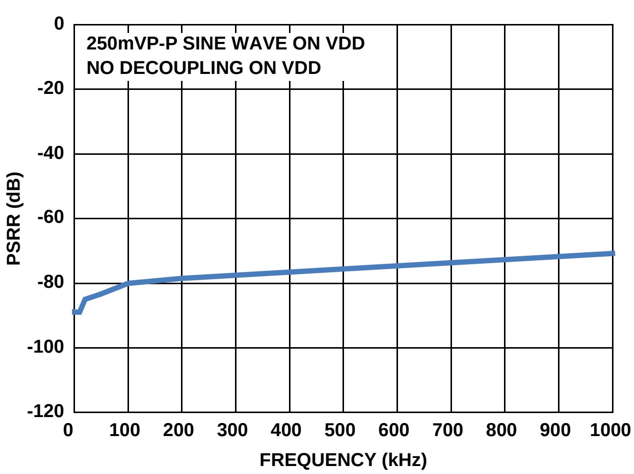


FIGURE 9. PSRR vs SUPPLY RIPPLE FREQUENCY WITHOUT SUPPLY DECOUPLING

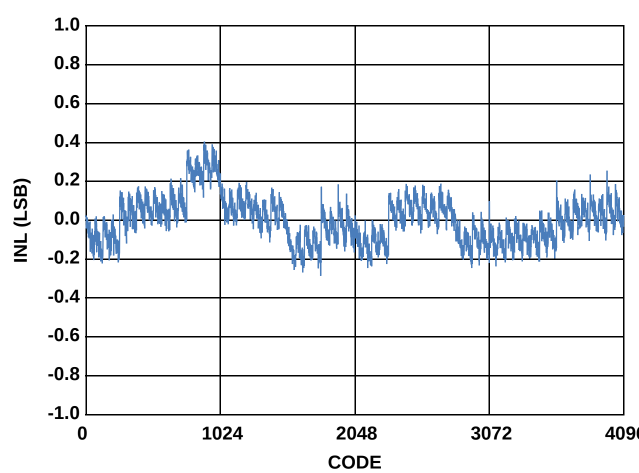


FIGURE 10. TYPICAL INL FOR THE ISL267450A FOR V_{DD} = 5V

Typical Performance Characteristics (Continued)

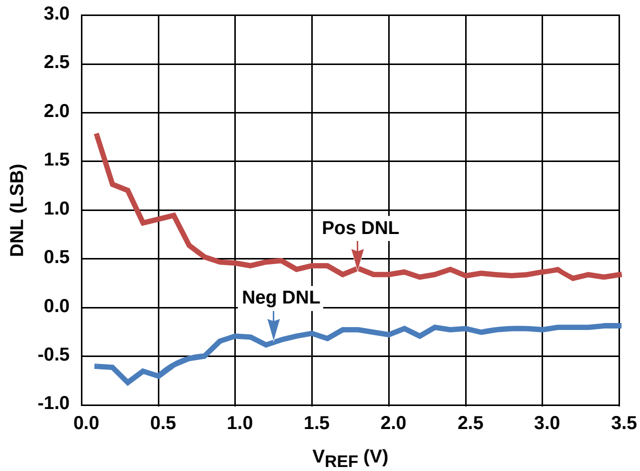


FIGURE 11. CHANGE IN DNL vs VREF FOR THE ISL267450A FOR V_{DD} = 5V

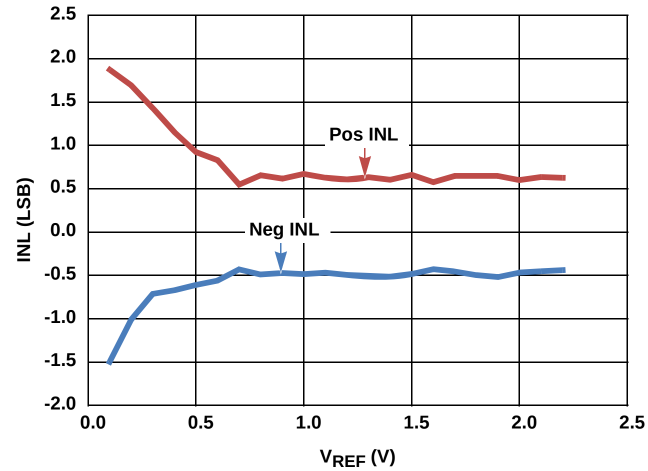


FIGURE 12. CHANGE IN INL vs VREF FOR THE ISL267450A FOR V_{DD} = 3V

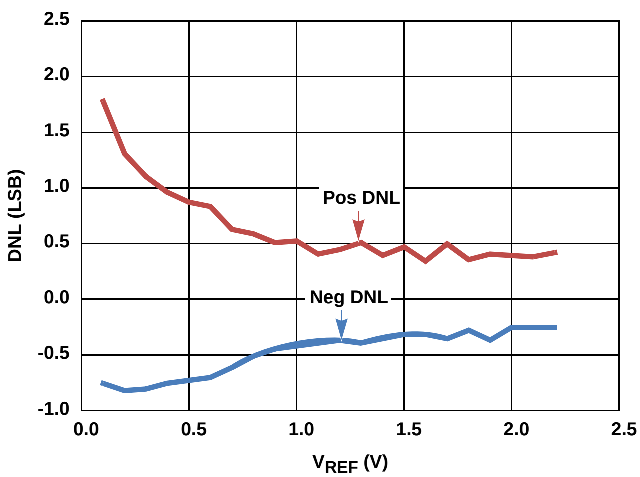


FIGURE 13. CHANGE IN DNL VS. VREF FOR THE ISL267450A FOR V_{DD} = 3V

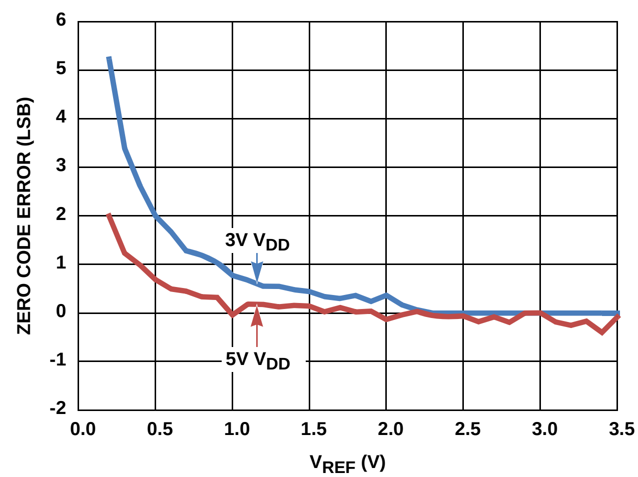


FIGURE 14. CHANGE IN OFFSET ERROR vs REFERENCE VOLTAGE FOR V_{DD} = 5V AND 3V FOR THE ISL267450A

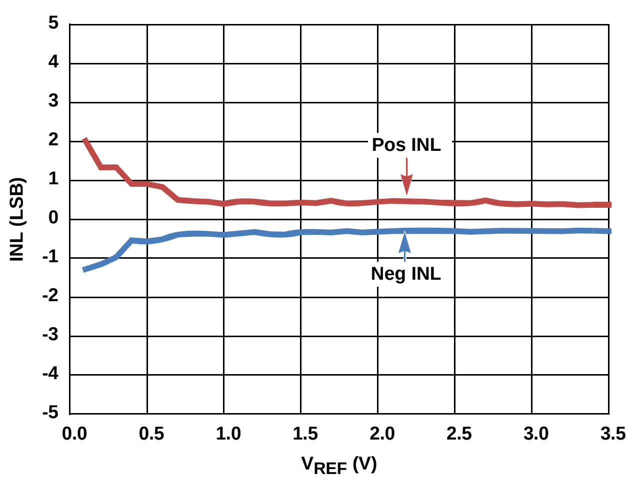


FIGURE 15. CHANGE IN INL vs VREF FOR THE ISL267450A FOR V_{DD} = 5V

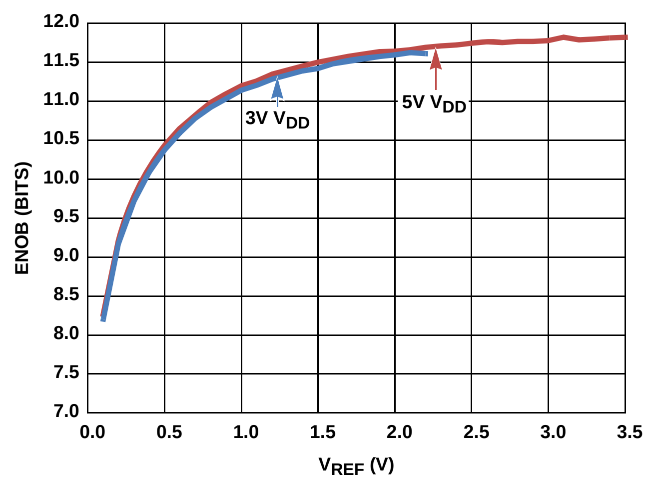


FIGURE 16. CHANGE IN ENOB vs REFERENCE VOLTAGE FOR V_{DD} = 5V AND 3V FOR THE ISL267450A

Typical Performance Characteristics (Continued)

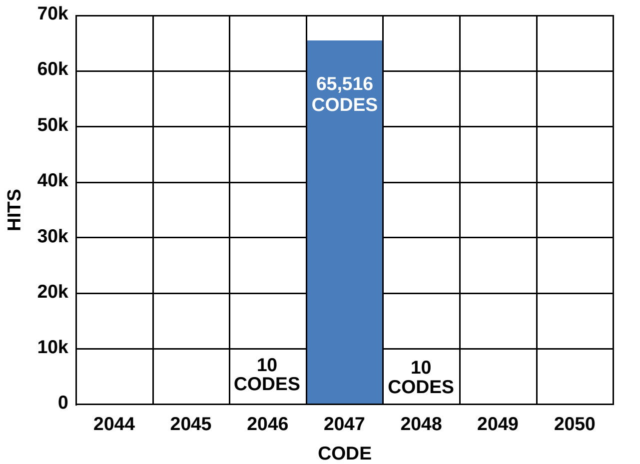


FIGURE 17. HISTOGRAM OF 10,000 CONVERSIONS OF A DC INPUT FOR THE ISL267450A WITH V_{DD} = 5V

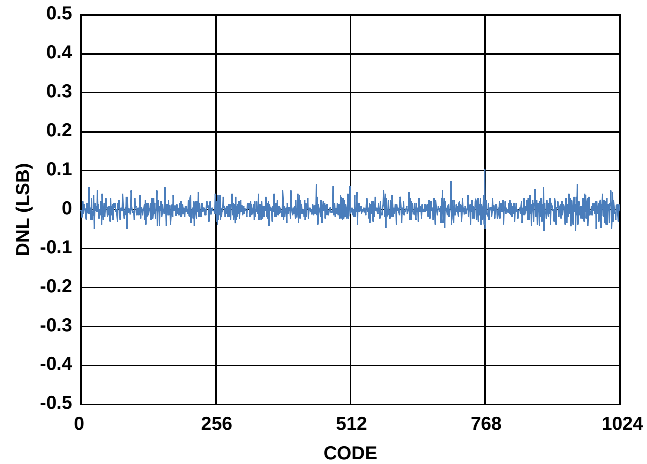


FIGURE 18. TYPICAL DNL FOR THE ISL267440 FOR V_{DD} = 5V

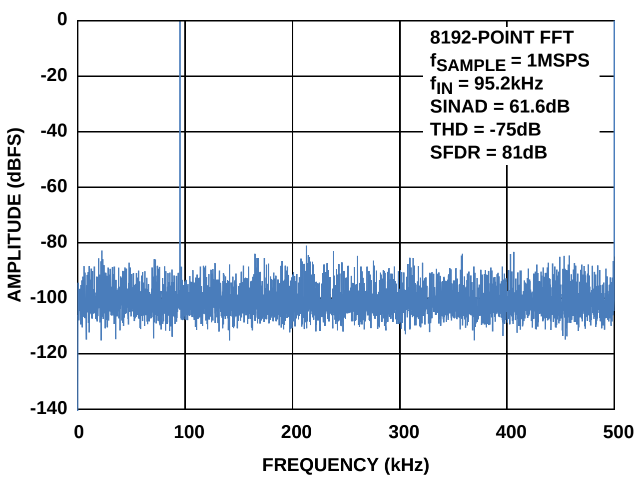


FIGURE 19. ISL267440 DYNAMIC PERFORMANCE WITH V_{DD} = 5V

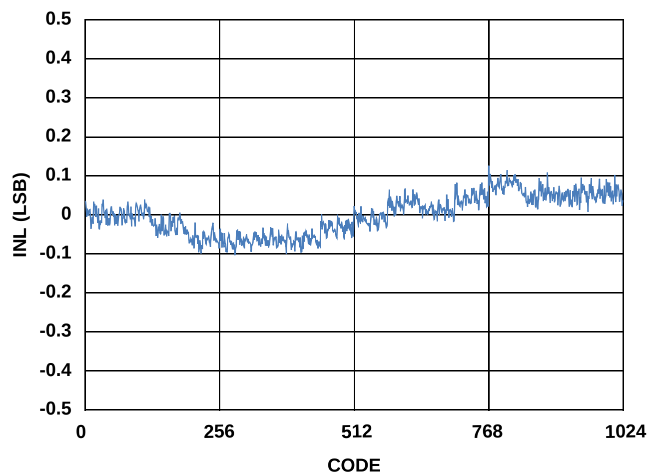


FIGURE 20. TYPICAL INL FOR THE ISL267440 FOR V_{DD} = 5V

Functional Description

The ISL267440, ISL267450A are based on a successive approximation register (SAR) architecture utilizing capacitive charge redistribution digital to analog converters (DACs). Figure 21 shows a simplified representation of the converter. During the acquisition phase (ACQ) the differential input is stored on the sampling capacitors (CS). The comparator is in a balanced state since the switch across its inputs is closed. The signal is fully acquired after t_{ACQ} has elapsed, and the switches then transition to the conversion phase (CONV) so the stored voltage may be converted to digital format. The comparator will become unbalanced when the differential switch opens and the input switches transition (assuming that the stored voltage is not exactly at mid-scale). The comparator output reflects whether the stored voltage is above or below mid-scale, which sets the value of the MSB. The SAR logic then forces the capacitive DACs to adjust up or down by one quarter of full-scale by switching in binarily weighted capacitors. Again, the comparator output reflects whether the stored voltage is above or below the new value, setting the value of the next lowest bit. This process repeats until all 12 bits have been resolved.

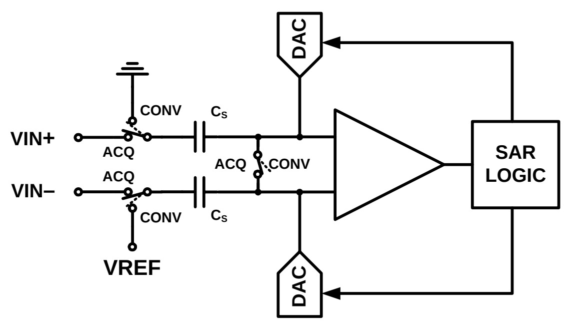


FIGURE 21. SAR ADC ARCHITECTURAL BLOCK DIAGRAM

An external clock must be applied to the SCLOCK pin to generate a conversion result. The allowable frequency range for SCLOCK is 10kHz to 18MHz (556SPS to 1MSPS). Serial output data is transmitted on the falling edge of SCLOCK. The receiving device (FPGA, DSP or Microcontroller) may latch the data on the rising edge of SCLOCK to maximize set-up and hold times.

A stable, low-noise reference voltage must be applied to the VREF pin to set the full-scale input range and common-mode voltage. See “Voltage Reference Input” on page 12 for more details.

ADC Transfer Function

The output coding for the ISL267440, ISL267450A is twos complement. The first code transition occurs at successive LSB values (i.e., 1 LSB, 2 LSB, and so on). The LSB size of the ISL267450A is 2*VREF/4096, while the LSB size of the ISL267440 is 2*VREF/1024. The ideal transfer characteristic of the ISL267440, ISL267450A is shown in Figure 22.

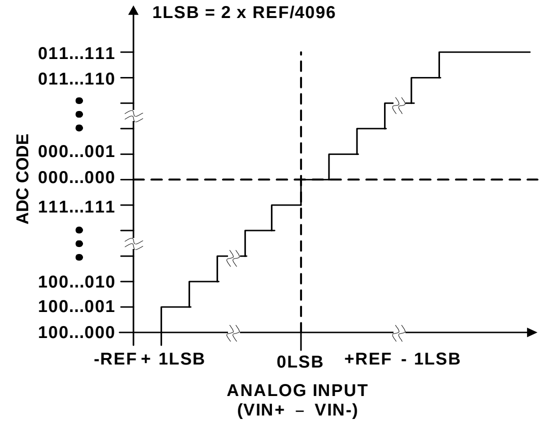


FIGURE 22. IDEAL TRANSFER CHARACTERISTICS

Analog Input

The ISL267440, ISL267450A feature a fully differential input with a nominal full-scale range equal to twice the applied VREF voltage. Each input swings VREF V_{P-P}, 180° out of phase from one another for a total differential input of 2*VREF (refer to Figure 23). Differential signaling offers several benefits over a single-ended input, such as:

- Doubling of the full-scale input range (and therefore the dynamic range)
- Improved even order harmonic distortion
- Better noise immunity due to common mode rejection

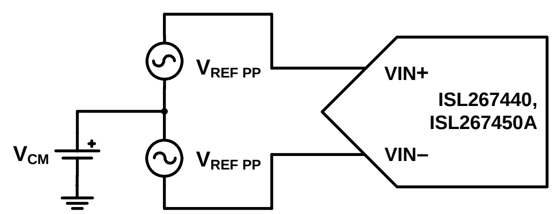


FIGURE 23. DIFFERENTIAL INPUT SIGNALING

Figure 24 shows the relationship between the reference voltage and the full-scale input range for two different values of VREF.

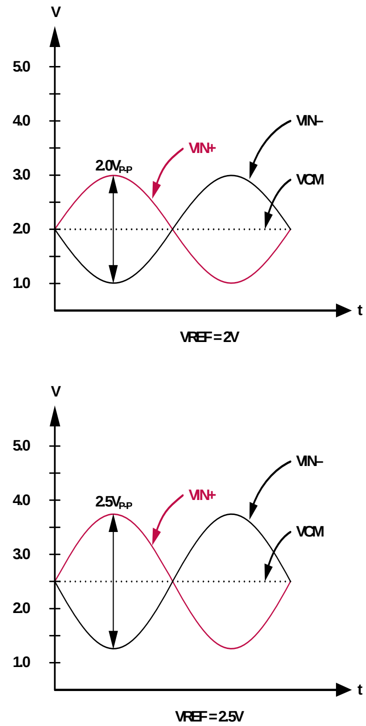


FIGURE 24. RELATIONSHIP BETWEEN VREF AND FULL-SCALE RANGE

Note that there is a trade-off between VREF and the allowable common mode input voltage (VCM). The full-scale input range is proportional to VREF; therefore the VCM range must be limited for larger values of VREF in order to keep the absolute maximum and minimum voltages on the VIN+ and VIN– pins within specification. Figures 25 and 26 illustrate this relationship for 5V and 3V operation, respectively. The dashed lines show the theoretical VCM range based solely on keeping the VIN+ and VIN– pins within the supply rails. Additional restrictions are imposed due to the required headroom of the input circuitry, resulting in practical limits shown by the shaded area.

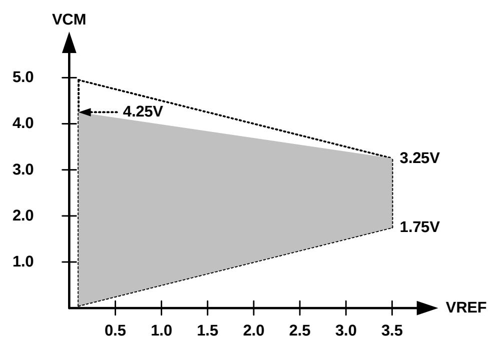


FIGURE 25. RELATIONSHIP BETWEEN VREF AND VCM FOR V_{DD} = 5V

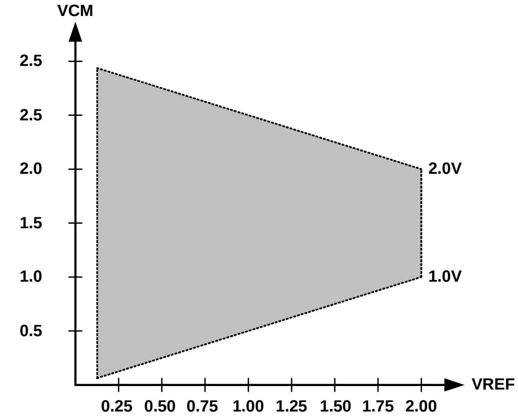


FIGURE 26. RELATIONSHIP BETWEEN VREF AND VCM FOR V_{DD} = 3V

Voltage Reference Input

An external low-noise reference voltage must be applied to the VREF pin to set the full-scale input range of the converter. The reference input accepts voltages ranging from 0.1V to 2.2V for 3V operation and 0.1V to 3.5V for 5V operation. The device is specified with a reference voltage of 2.5V for 5V operation and 2.0V for 3V operation. This pin should be decoupled with a combination of a 1µF electrolytic capacitor and a 0.1µF ceramic capacitor on the PC board.

Since the full-scale input range is proportional to the applied VREF, any noise or drift will appear as an error in the conversion result. A low-noise, low-drift reference, such as the ISL2100x family, may be used to maximize system performance, as shown in Figure 27. The VREF pin typically draws 4µA and the current is dependent upon the sampled voltage. This can result in a code-dependent error if there is excessive series resistance or the reference lacks sufficient load regulation; therefore, buffering may be necessary.

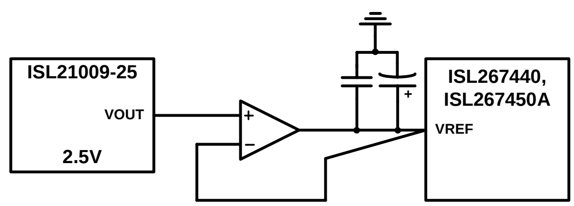


FIGURE 27. BUFFERED VOLTAGE REFERENCE

Power-Down/Standby Modes

The mode of operation of the ISL267440, ISL267450A is selected by controlling the logic state of the $\overline{CS}$ signal during a conversion. There are two possible modes of operation: dynamic mode or static mode. When $\overline{CS}$ is high (deasserted) the ADC will be in static mode. Conversely, when $\overline{CS}$ is low (asserted) the device will be in dynamic mode. There are no minimum or maximum number of SCLOCK cycles required to enter static mode, which simplifies power management and allows the user to easily optimize power dissipation versus throughput for different application requirements.

DYNAMIC MODE

This mode is entered when a conversion result is desired by asserting $\overline{CS}$. Figure 28 shows the general diagram of operation in this mode. The conversion is initiated on the falling edge of $\overline{CS}$, as described in "Serial Digital Interface" on page 13. As soon as $\overline{CS}$ is brought high, the conversion will be terminated and SDATA will go back into three-state. Sixteen serial clock cycles are required to complete the conversion and access the complete conversion result. $\overline{CS}$ may idle high until the next conversion or idle low until sometime prior to the next conversion. Once a data transfer is complete, i.e., when SDATA has returned to three-state, another conversion can be initiated by again bringing $\overline{CS}$ low.

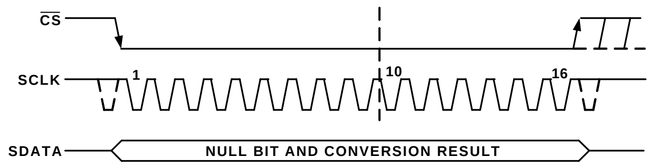


FIGURE 28. NORMAL MODE OPERATION

STATIC MODE

The ISL267440, ISL267450A enter the power-saving static mode automatically any time $\overline{CS}$ is deasserted. It is not required that the user force a device into this mode following a conversion in order to optimize power consumption.

SHORT CYCLING

In cases where a lower resolution conversion is acceptable, $\overline{CS}$ can be pulled high before 12 SCLOCK falling edges have elapsed. This is referred to as short cycling, and it can be used to further optimize power dissipation. In this mode a lower resolution result will be acquired, but the ADC will enter static mode sooner and exhibit a lower average power dissipation than if the complete conversion cycle were carried out. The acquisition time (t_{ACQ}) requirement must be met for the next conversion to be valid.

POWER-ON RESET

The ISL267440, ISL267450A performs a power-on reset when the supplies are first activated, which requires approximately 2.5ms to execute. After this is complete, a single dummy cycle must be executed in order to initialize the switched capacitor track and hold. A dummy cycle will take 1µs with an 18MHz SCLOCK. Once the dummy cycle is complete, the ADC mode will be determined by the state of $\overline{CS}$. At this point, switching between dynamic and static modes is controlled by $\overline{CS}$ with no delay required between states.

POWER vs THROUGHPUT RATE

The ISL267440, ISL267450A provide reduced power consumption at lower conversion rates by automatically switching into a low-power mode after completing a conversion. The average power consumption of the ADC decreases at lower throughput rates. Figure 29 shows the typical power consumption over a wide range of throughput rates.

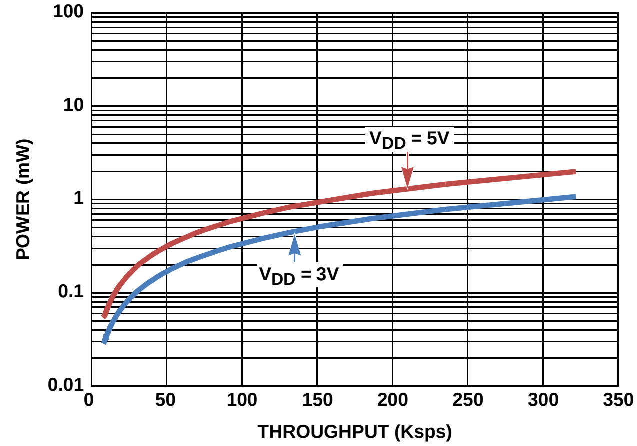


FIGURE 29. POWER CONSUMPTION vs THROUGHPUT RATE

Serial Digital Interface

Conversion data is accessed with an SPI-compatible serial interface. The interface consists of the data clock (SCLOCK), serial data output (SDATA), and chip select ($\overline{CS}$).

A falling edge on the $\overline{CS}$ signal initiates a conversion by placing the part into the acquisition (ACQ) phase. After t_{ACQ} has elapsed, the part enters the conversion (CONV) phase and begins outputting the conversion result starting with a null bit followed by the most significant bit (MSB) and ending with the least significant bit (LSB). The $\overline{CS}$ pin can be pulled high at this point to put the device into Standby mode and reduce the power consumption. If $\overline{CS}$ is held low after the LSB bit has been output, the serial output enters a high impedance state. The ISL267440, ISL267450A will remain in this state, dissipating typical dynamic power levels, until $\overline{CS}$ transitions high then low to initiate the next conversion.

Data Format

Output data is encoded in two's complement format as shown in Table 1. The voltage levels in the table are idealized and don't account for any gain/offset errors or noise.

TABLE 1. TWO'S COMPLEMENT DATA FORMATTING

INPUT	VOLTAGE	DIGITAL OUTPUT
–Full Scale	–VREF	1000 0000 0000
–Full Scale + 1LSB	–VREF+ 1LSB	1000 0000 0001
Midscale	0	0000 0000 0000
+Full Scale – 1LSB	+VREF– 1LSB	0111 1111 1110
+Full Scale	+VREF	0111 1111 1111

Applications Information

Adjustable Low-Noise Reference

Figure 30 illustrates how a Digitally Controlled Potentiometer (DCP) can be used in conjunction with a low-noise, low-drift reference to realize an adjustable input range with high system accuracy. The voltage reference output is connected to the high terminal of the DCP and the wiper terminal is buffered and connected to the ADC reference. Buffering is required since the ISL267440, ISL267450A reference input current will cause a voltage drop across the DCP element (100kΩ from RH to RL), impacting accuracy and increasing temperature drift.

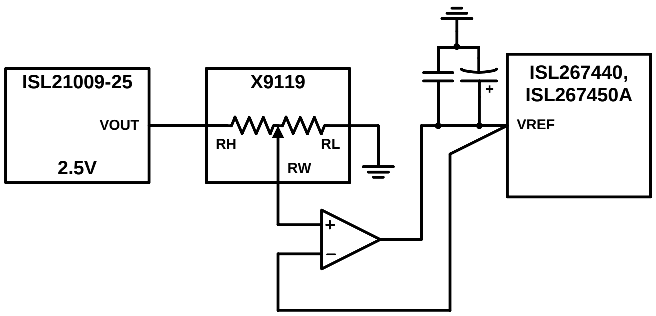


FIGURE 30. ADJUSTABLE BUFFERED VOLTAGE REFERENCE

Terminology

Signal-to-(Noise + Distortion) Ratio (SINAD)

This is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding DC. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\text{Signal-to-(Noise + Distortion)} = (6.02\,N + 1.76)\,dB \qquad \text{(EQ. 1)}$$

Thus, for a 12-bit converter this is 74dB, and for a 10-bit this is 62dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the ISL267440, ISL267450A, it is defined as:

$$THD(dB) = 20\log\sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}{V_1^2}} \qquad \text{(EQ. 2)}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second to the sixth harmonics.

Peak Harmonic or Spurious Noise (SFDR)

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to fs/2 and excluding DC) to the rms value of the fundamental (also referred to as Spurious Free Dynamic Range (SFDR)). Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m and n = 0, 1, 2 or 3. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb), and (fa –2fb).

The ISL267440, ISL267450A is tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

Aperture Delay

This is the amount of time from the leading edge of the sampling clock until the ADC actually takes the sample.

Aperture Jitter

This is the sample-to-sample variation in the effective point in time at which the actual sample is taken.

Full Power Bandwidth

The full power bandwidth of an ADC is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input.

Common-Mode Rejection Ratio (CMRR)

The common-mode rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 250mV$_{P-P}$ sine wave applied to the common-mode voltage of VIN+ and VIN– of frequency fs:

$$CMRR(dB) = 10\log(Pfl/Pfs) \qquad \text{(EQ. 3)}$$

Pf is the power at the frequency f in the ADC output; *Pfs* is the power at frequency fs in the ADC output.

Integral Nonlinearity (INL)

This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity (DNL)

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Zero-Code Error

This is the deviation of the midscale code transition (111...111 to 000...000) from the ideal VIN+ – VIN– (i.e., 0 LSB).

Positive Gain Error

This is the deviation of the last code transition (011...110 to 011...111) from the ideal VIN+ – VIN– (i.e., +REF – 1 LSB), after the zero code error has been adjusted out.

Negative Gain Error

This is the deviation of the first code transition (100...000 to 100...001) from the ideal VIN+ – VIN– (i.e., – REF + 1 LSB), after the zero code error has been adjusted out.

Track and Hold Acquisition Time

The track and hold acquisition time is the minimum time required for the track and hold amplifier to remain in track mode for its output to reach and settle to within 0.5 LSB of the applied input signal.

Power Supply Rejection Ratio (PSRR)

The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f, to ADC VDD supply of frequency f_S. The frequency of this input varies from 1kHz to 1MHz.

$$PSRR(dB) = 10\log(Pf/Pfs) \quad \text{(EQ. 4)}$$

Pf is the power at frequency f in the ADC output; *Pfs* is the power at frequency f_S in the ADC output.

Application Hints

Grounding and Layout

The printed circuit board that houses the ISL267440, ISL267450A should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes since it gives the best shielding. Digital and analog ground planes should be joined in only one place, and the connection should be a star ground point established as close to the GND pin on the ISL267440, ISL267450A as possible. Avoid running digital lines under the device, as this will couple noise onto the die. The analog ground plane should be allowed to run under the ISL267440, ISL267450A to avoid noise coupling.

The power supply lines to the device should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board.

In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with µF tantalum capacitors in parallel with 0.1µF capacitors to GND. To achieve the best from these decoupling components, they must be placed as close as possible to the device.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
December 5, 2011	FN7708.0	Initial release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL267440, ISL267450A

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

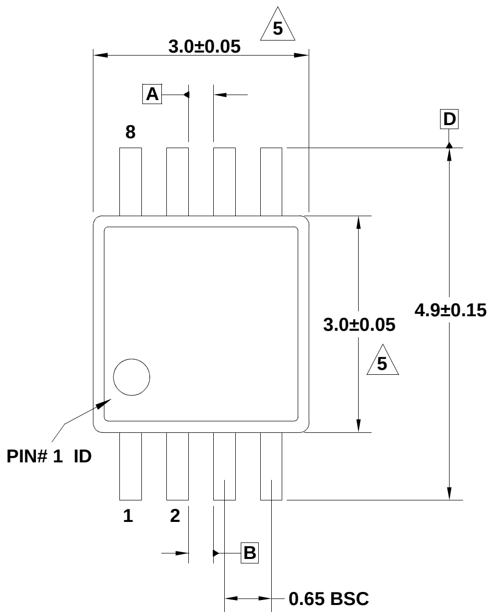
FITs are available from our website at: http://rel.intersil.com/reports/search.php

Package Outline Drawing

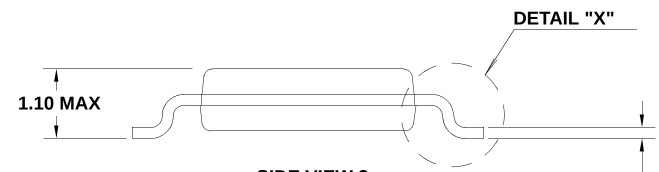
M8.118

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

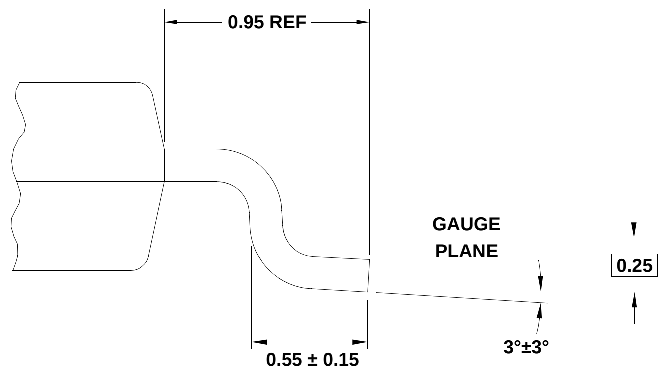
Rev 4, 7/11



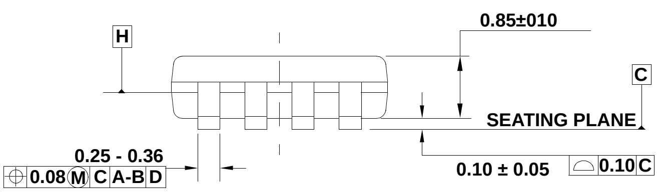
TOP VIEW



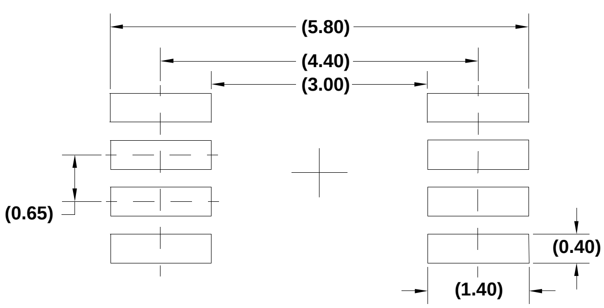
SIDE VIEW 2



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.