M56693FP/GP

Bi-CMOS & DMOS 32BIT SERIAL-INPUT LATCHED DRIVER

DESCRIPTION

The M56693 is a semiconductor integrated circuit that has a built-in, 32-bit shift register and a latch of CMOS structure with serial input and serial/parallel output, and a 32-bit totem-pole-type parallel output driver of high pressure proof DMOS structure. Employed are BI-CMOS and high pressure proof DMOS processing technology.

FEATURES

- Serial input–serial/parallel output
- Cascade connections possible through serial output
- Latch circuit included for each stage
- Driver supply voltage: V_H=120V
- Operating temperature: -20 – 75°C

APPLICATION

Vacuum Fluorescent Display ANODE DRIVER

FUNCTION

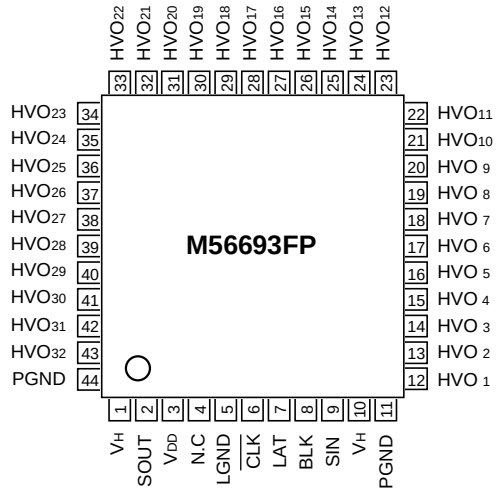
The M56693 comprises a 32-bit D type flip-flop with a 32 latches connected to its output.

In accordance with truth table 1, inputting data to SIN and clock pulse to $\overline{CLK}$ allows SIN signal to be put into the internal shift register when the clock changes from “H” to “L”, and simultaneously shift register data to be shifted sequentially.

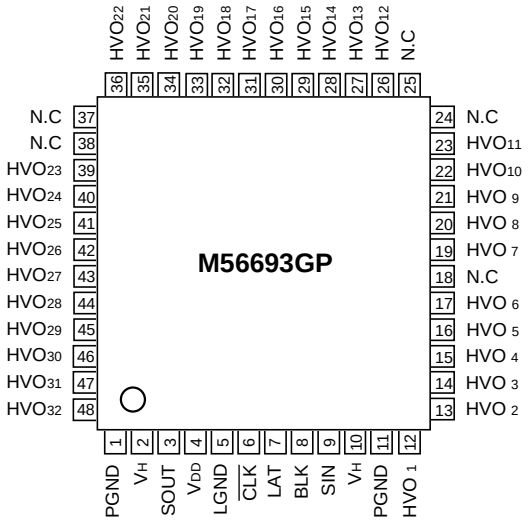
Serial output SOUT is used by connecting to the next stage M56693 SIN when more than one M56693 is used to expand bits in the series.

In accordance with truth table 2, parallel output allows the latch to pass data through if LAT input is turned to “H”, and data to be retained if LAT is turned to “L”. Driver output HVOn allows data from the latch to be output if BLK input is turned to “L”, and “L” to be output if BLK input is turned to “H”, irrespective of data from the latch.

PIN CONFIGURATION (TOP VIEW)



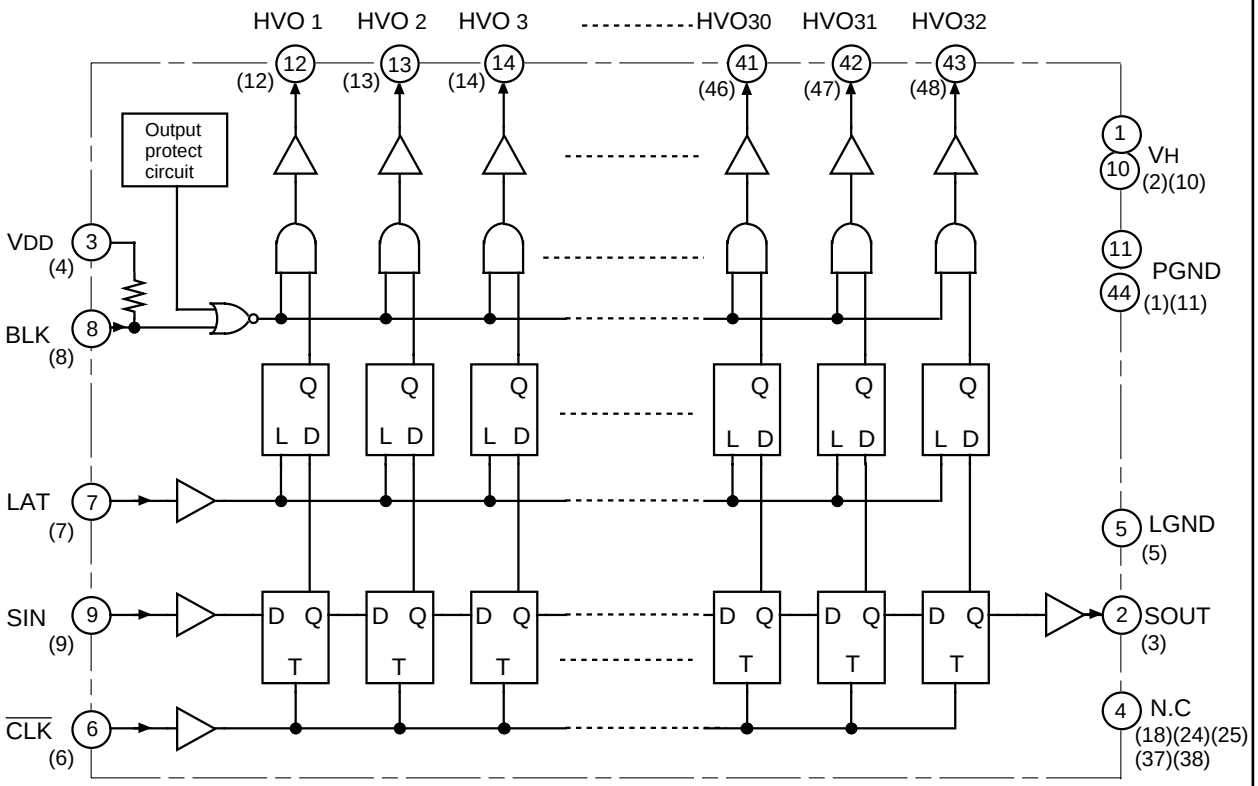
Outline 44P6N-A (FP)



Outline 48P6D-A (GP)

N.C: no connection

BLOCK DIAGRAM (Note : Pin No. in paretheses are of M56693GP)



TRUTH TABLE

Truth table 1. Shift register section

$\overline{CLK}$	Shift register operation
↓	DATA is shifted.
H or L	No changes.

Truth table 2. Latch and driver sections

Dn	LAT	BLK	HVOn
X	X	H	Output all “L”
H	H	L	H
L	H	L	L
X	L	L	Latch’s data output.

Dn=nth bit DFF retention data
HVOn=nth bit driver output
L=“L” level
H=“H” level
X=“L” level or “H” level

PIN FUNCTION DESCRIPTION

Pin name	Function
V_{DD}	Logic stage supply voltage
LGND	Logic stage ground
V_H	Output stage supply voltage
PGND	Output stage ground
$\overline{CLK}$	Clock input for the internal shift resister. The data enter the internal shift resisters and the data in the shift registers will be shifted in order by High to Low change of the clock.
SIN	Serial data input
SOUT	Serial data output
LAT	Latch input. When the LATCH is set to “H”, the data in the shift resister will enter the each latch circuit. When the LATCH input is set to “L”, the data will be held.
BLK	Enable input for output control. When the BLK input is set to “L”, data in the latch circuit will appear at outputs. When the BLK input is set to “H”, all outputs will be set to “L”.
HVO1 – 32	Output driver (push-pull)

ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Logic stage supply voltage		-0.3 – 7	V
V_H	Output stage supply voltage		-0.3 – 120	V
VI	Logic inputs voltage		-0.3 – V_{DD}+0.3	V
V_O	Logic outputs voltage	Data output	-0.3 – V_{DD}+0.3	V
V_{HVO}	Outputs voltage	High supply voltage output pin	-0.3 – V_H	V
Pd	Power dissipation range	Ta ≤ 25°C	940	mW
Tstg	Storage temperature range		-55 – 150	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage		4.5 – 5.5	V
V_H	Supply voltage		10 – 110	V
Topr	Operating temperature		-20 – 75	°C

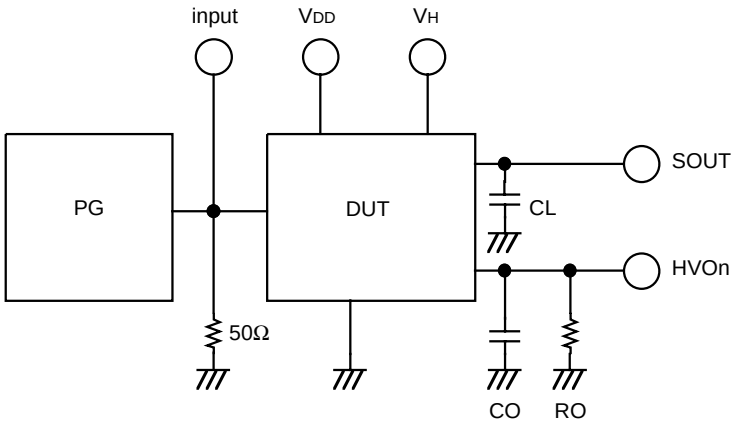
ELECTRICAL CHARACTERISTICS (V_{DD}=5V, V_H=110V and Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{DD}	Supply current 1	No load			1	2	mA
I_H	Supply current 2	Output all “L”, no load			0	50	μA
		Output all “H”, no load			2	4	mA
I_{IH}	“H” input current	V_{IH}=5V	Input pin		0	2	μA
I_{IL}	“L” input current	V_{IL} = 0V	SIN, LAT, $\overline{CLK}$		0	-2	μA
			BLK		-20	-100	μA
V_{HVOH}	Driver output voltage	I_{HVOH} = -0.5mA		100	106		V
V_{HVOL}		I_{HVOL} = 0.5mA			0.7	2	
V_{OH}	Logic output voltage	I_{OH} = -0.1mA		4.5	4.95		V
V_{OL}		I_{OL} = 0.1mA			0.04	0.4	
I_{HVOH}	“H” output current	High supply voltage output pin			-1	-3	mA
I_{HVOL}	“L” output current	High supply voltage output pin			1	3	mA
V_{TH}	Output protect operating voltage				3.4		V
V_{TL}					3.1		V

SWITCHING CHARACTERISTICS (V_{DD}=5V, V_H=110V and Ta=25°C, unless otherwise noted)

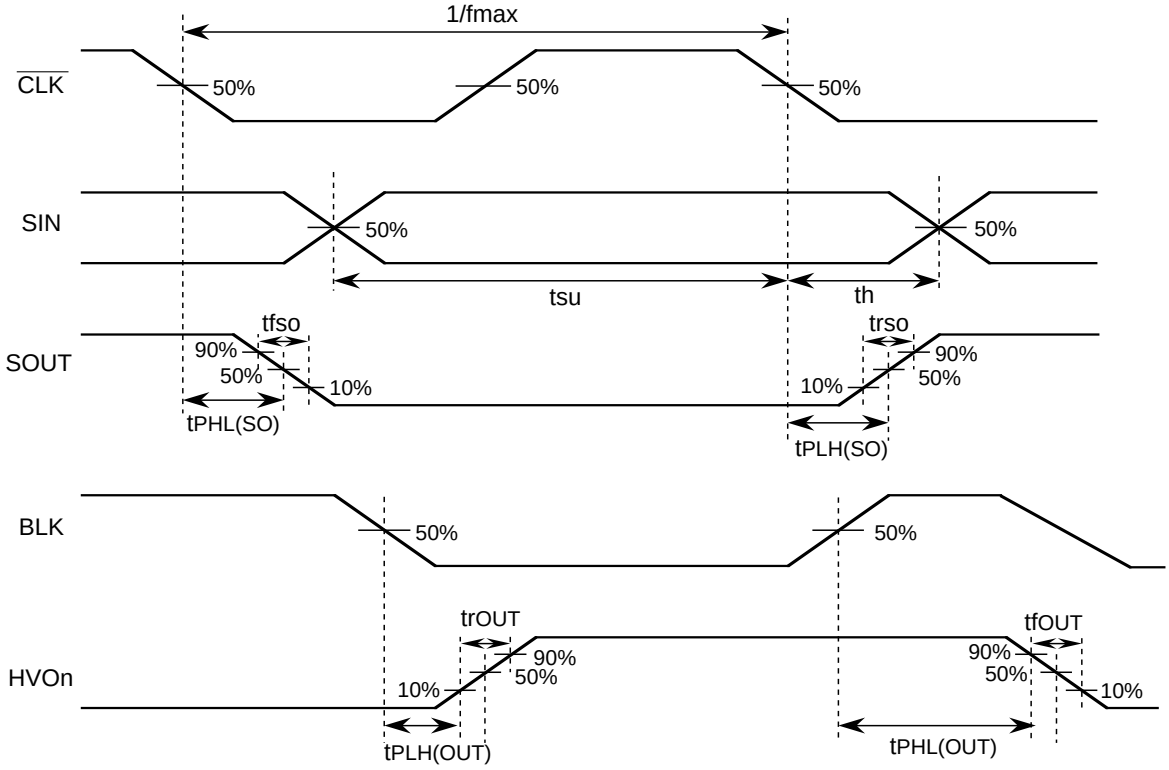
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$f\overline{CLK}$	Clock frequency	Duty = 45 – 55%			8	MHz
tPLH(SO)	Logic output propagation time	CL = 15pF		120	300	ns
tPHL(SO)				100	300	ns
tPLH(OUT)	Driver output propagation time	RO = 220KΩ CO = 50pF		1	2	µs
tPHL(OUT)				0.16	1	µs
trout	Driver output rise and fall time			1.3	2.5	µs
tfout				0.35	2	µs

TEST CIRCUIT



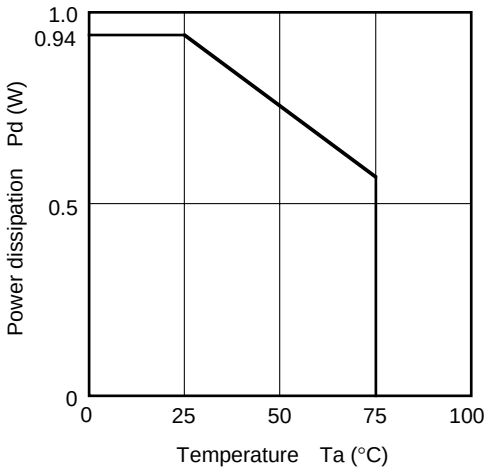
(1) Pulse generator characteristics
tr≤20ns tf≤20ns
(2) Capacitance CL includes connection floating capacitance and probe input capacitance.
: RO=220KΩ
: CO=50pF

TIMING WAVEFORM

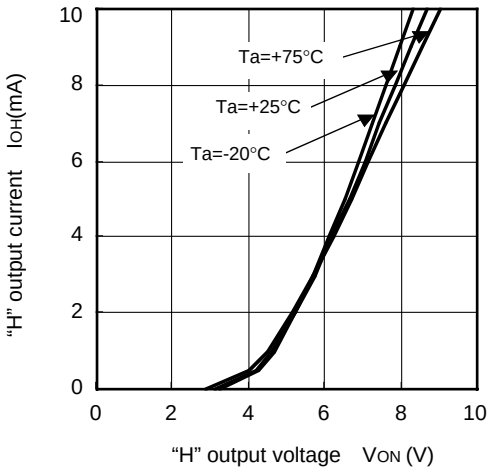


TYPICAL CHARACTERISTICS

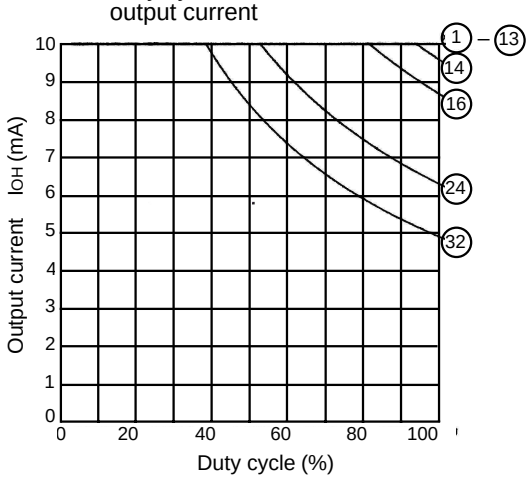
Thermal derating



Driver output V_{ON}–I_{OH}

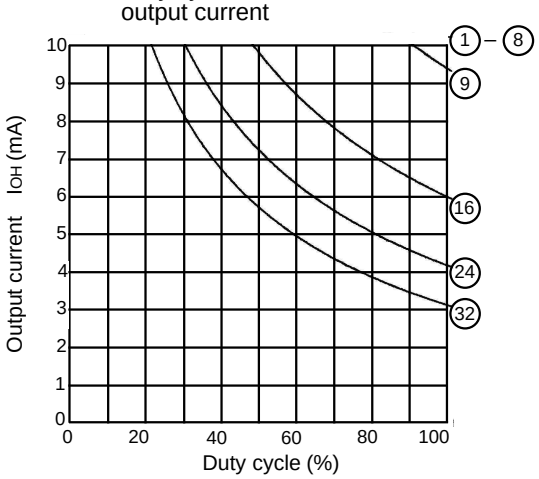


Duty cycle vs Permissible output current



Note • Ta=25°C
• Repeated frequency >100Hz
• Figure in the circle represents the number of concurrently operating output circuits.
• Current value denotes a numerical value per circuit.

Duty cycle vs Permissible output current



Note • Ta=75°C
• Repeated frequency >100Hz
• Figure in the circle represents the number of concurrently operating output circuits.
• Current value denotes a numerical value per circuit.

Note 1. V_{DD}=5V and V_H=110V, unless otherwise noted
2. Thermal derating characteristics represent those of an individual IC unit.
3. Allowable duty cycle output current characteristics represent that when a standard substrate is mounted. (Standard substrate: 70x70x1.6mm glass epoxy)