

DATA SHEET

TDA9859

Universal hi-fi audio processor for
TV

Preliminary specification
File under Integrated Circuits, IC02

1997 Sep 01

Universal hi-fi audio processor for TV

TDA9859

FEATURES

- Multi-source selector switches six AF inputs (three stereo sources or six mono sources)
- Each of the input signals can be switched to each of the outputs (crossbar switch)
- Outputs for loudspeaker channel and peri-TV connector (SCART)
- Switchable spatial stereo and pseudo stereo effects
- Audio surround decoder can be added externally
- Two general purpose logic output ports
- I²C-bus control of all functions.



GENERAL DESCRIPTION

The TDA9859 provides control facilities for the main and the SCART channel of a TV set. Due to extended switching possibilities, signals from three stereo sources can be handled.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _P	positive supply voltage (pin 6)	7.2	8.0	8.8	V
I _P	supply current	–	25	–	mA
V _{i(rms)}	input signal levels for 0 dB gain (RMS value)	2	–	–	V
V _{o(rms)}	output signal levels for 0 dB gain (RMS value)	2	–	–	V
G _v	voltage gain in main channel				
	volume control (1 dB steps, balance included)	–63	–	+15	dB
	mute	–80	–	–	dB
	bass control (1.5 dB steps)	–12	–	+15	dB
	treble control (3 dB steps)	–12	–	+12	dB
THD	total harmonic distortion	–	0.1	–	%
S/N	signal-to-noise ratio	–	85	–	dB
T _{amb}	operating ambient temperature	0	–	70	°C

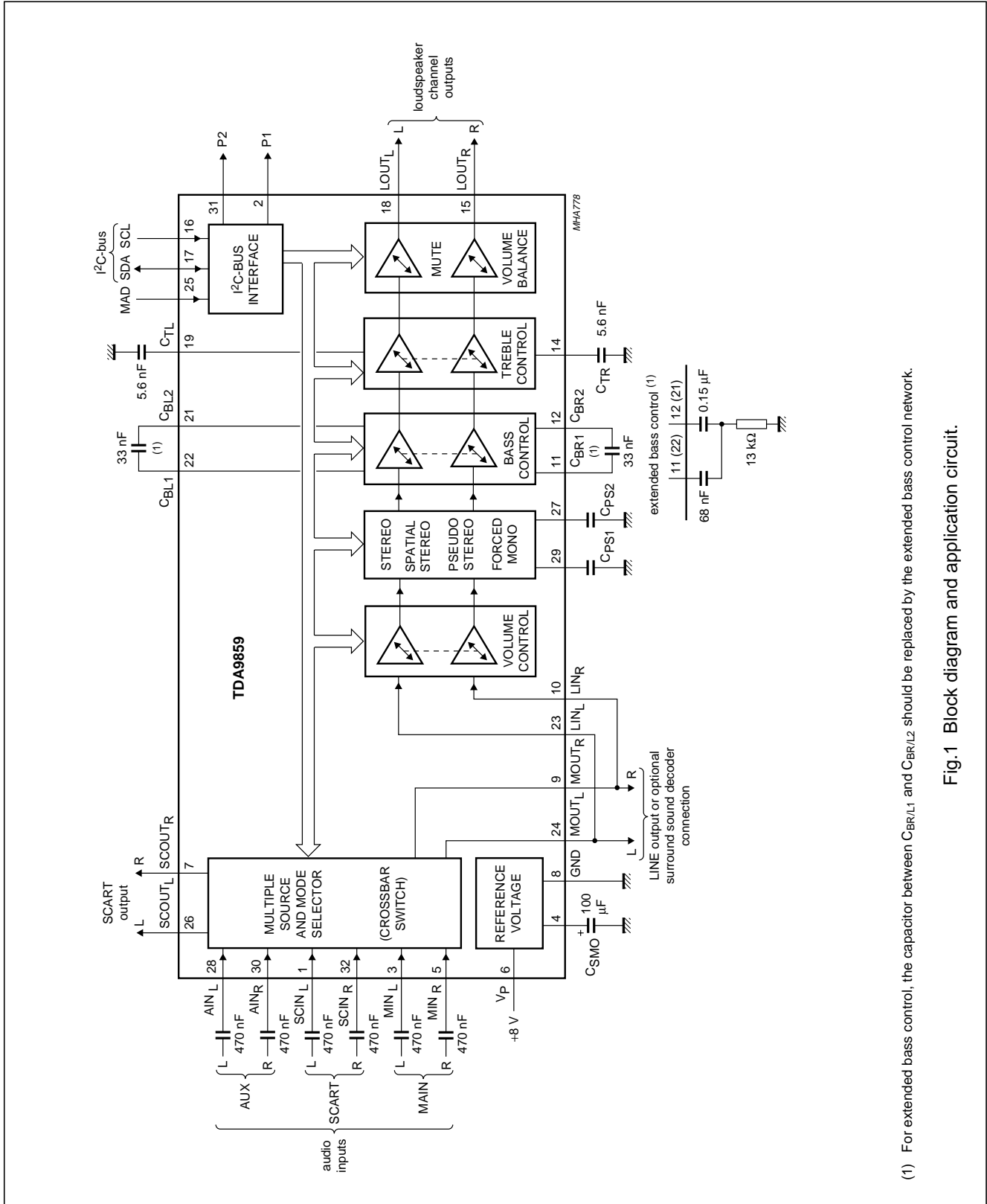
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9859	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1

Universal hi-fi audio processor for TV

TDA9859

BLOCK DIAGRAM



(1) For extended bass control, the capacitor between C_{BR1/L1} and C_{BR2/L2} should be replaced by the extended bass control network.

Fig.1 Block diagram and application circuit.

Universal hi-fi audio processor for TV

TDA9859

PINNING

SYMBOL	PIN	DESCRIPTION
SCIN _L	1	SCART input; left channel
P1	2	port 1 output
MIN _L	3	MAIN input; left channel
C _{SMO}	4	smoothing capacitor of reference voltage
MIN _R	5	MAIN input; right channel
V _P	6	supply voltage
SCOUT _R	7	SCART output; right channel
GND	8	ground
MOU _T _R	9	MAIN output; right channel
LIN _R	10	input to right loudspeaker channel
C _{BR1}	11	bass capacitor connection 1; right channel
C _{BR2}	12	bass capacitor connection 2; right channel
n.c.	13	not connected
C _{TR}	14	treble capacitor connection; right channel
LOU _T _R	15	loudspeaker output; right channel
SCL	16	serial clock input; I ² C-bus
SDA	17	serial data input/output; I ² C-bus
LOU _T _L	18	loudspeaker output; left channel
C _{TL}	19	treble capacitor connection; left channel
n.c.	20	not connected
C _{BL2}	21	bass capacitor connection 2; left channel
C _{BL1}	22	bass capacitor connection 1; left channel
LIN _L	23	input to left loudspeaker channel
MOU _T _L	24	MAIN output; left channel
MAD	25	module address select input
SCOUT _L	26	SCART output; left channel
C _{PS2}	27	pseudo stereo capacitor 2
AIN _L	28	AUX input; left channel
C _{PS1}	29	pseudo stereo capacitor 1
AIN _R	30	AUX input; right channel
P2	31	port 2 output
SCIN _R	32	SCART input signal RIGHT

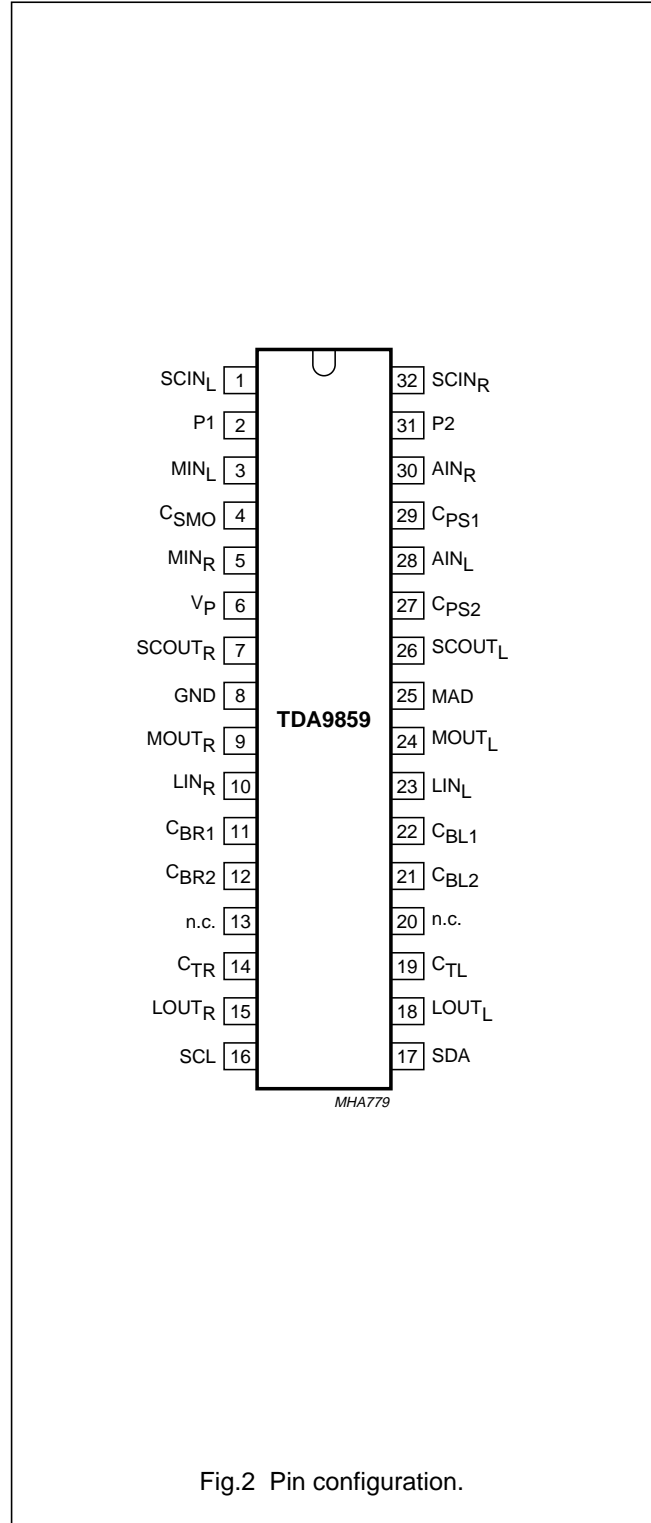


Fig.2 Pin configuration.

Universal hi-fi audio processor for TV

TDA9859

FUNCTIONAL DESCRIPTION

The TDA9859 consists of the following functions:

- Source select switching block
- Loudspeaker channel with effect controls
- Two port outputs for general purpose
- I²C-bus control.

Source select switching block

The TDA9859 selects and switches the input signals from three stereo or six mono sources MAIN, AUX and SCART (see Fig.1) to the outputs SCART and loudspeaker (crossbar-switching; Table 4). The main channel (LINE outputs) is looped outside the circuit (from pins 9 and 24 to pins 10 and 23), so signals can be used as LINE output or a surround sound decoder can be inserted.

Loudspeaker channel

Volume control is divided into volume control common and volume control left/right. The common part (–40 to +15 dB) controls the left and right channels

simultaneously; the left/right part (–23 to 0 dB) controls the volume of left and right channels independently. Treble control provides a control range from –12 to +12 dB and bass control from –12 to +15 dB. Extended bass control can be provided by an external T-network (see Fig.1) from –15 to +19 dB (2 dB steps).

Effect controls

'Linear stereo', 'stereo with spatial effect (30% or 52% anti-phase crosstalk)' and 'forced mono with or without pseudo-stereo effect' are controlled by three bits. A muting of 85 dB is provided.

I²C-bus control

All settings of control are stored in subaddress registers. Data transmission is simplified by auto-incrementing the subaddresses. The on-chip Power-on reset sets the mute bit to active, so both the SCART and the loudspeaker outputs are muted.

The muting can be switched off by writing a '0' (non-muted) into the mute control bits.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V _P	supply voltage (pin 6)	0	10	V
V _n	voltage on all pins, ground excluded	0	V _P	V
I _O	output current			
	at LOUT and SCOUT pins	–	2.5	mA
	at port output pins	–	1.5	mA
P _{tot}	total power dissipation	–	850	mW
T _{amb}	operating ambient temperature	0	70	°C
T _{stg}	storage temperature	–25	+150	°C
V _{es}	electrostatic handling for all pins; note 1	–	±300	V
	electrostatic handling for all pins; note 2	–	±2000	V

Notes

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor (Machine Model).
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor (Human Body Model).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	60	K/W

Universal hi-fi audio processor for TV

TDA9859

CHARACTERISTICS

$V_P = 8\text{ V}$; $T_{amb} = 25\text{ °C}$; treble and bass in linear positions (0 dB); volume control left/right 0 dB; spatial function, pseudo-stereo function and forced-mono function in off position and measurements taken in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 6)		7.2	8.0	8.8	V
I_P	supply current (pin 6)		–	25	–	mA
V_{ref}	internal reference voltage		–	$0.5V_P$	–	V
V_4	voltage at pin 4		–	$V_P - 0.1$	–	V
DC voltage on pins						
V_I	DC input voltage at pins 1, 3, 5, 10, 23, 28, 30 and 32 (inputs SCIN, MIN, LIN and AIN)		–	$0.5V_P$	–	V
V_O	DC output voltage at pins 7, 9, 15, 18, 24, 26 (outputs SCOUT, MOUT and LOU)		–	$0.5V_P$	–	V
V_C	DC voltage on capacitors (pins 11, 12, 14, 19, 21, 22, 27 and 29)		–	$0.5V_P$	–	V
Audio select switch; line and SCART outputs (controlled via I²C-bus); see Table 4						
$V_{i(rms)}$	maximum AF input signal on pins SCIN, MIN and AIN (RMS value)	THD $\leq 0.5\%$ on output pins	2	–	–	V
R_i	input resistance (pins SCIN, MIN and AIN)		20	30	40	k Ω
$B_{-0.5\text{ dB}}$	–0.5 dB bandwidth for pins SCOUT, MOUT and LOU.		20	–	20 000	Hz
$V_{o(rms)}$	maximum AF output signal on pins SCOUT and MOUT (RMS value)	THD $\leq 0.5\%$	2	–	–	V
R_L	allowed external load resistance on output (pins MOUT) on output (pins SCOUT)		10	–	–	k Ω
			5	–	–	k Ω
G_v	voltage gain from any input to SCART and MAIN outputs		–	0	–	dB
α_{cr}	switch crosstalk on outputs between AF inputs at $f = 10\text{ kHz}$	unused inputs connected to ground	–	90	–	dB
Volume control common (f = 1 kHz, 55 steps)						
$V_{i(rms)}$	maximum input signal (RMS value; pins LIN)	$G_v = 0$; THD $\leq 0.5\%$ on output pins 15 and 18	2	–	–	V
R_i	input resistance (pins LIN)		7.5	10	–	k Ω
G_v	volume control common voltage gain nominal minimum		–40	–	+15	dB
			–38	–	+14	dB

Universal hi-fi audio processor for TV

TDA9859

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG_V	volume control common voltage gain step width	$G_V = -32$ to $+15$ dB $G_V = -40$ to -33 dB	0.5 0.25	1.0 1.0	1.5 1.75	dB dB
	volume control common voltage gain set error	$G_V = -32$ to $+15$ dB $G_V = -40$ to -33 dB	– –	– –	1 2	dB dB
Volume control left/right (f = 1 kHz, 24 steps)						
G_V	volume control left/right voltage gain nominal		–24	–	0	dB
	minimum		–23	–	–1	dB
	mute position		–80	–85	–	dB
ΔG_V	volume control left/right voltage gain step width		0.5	1.0	1.5	dB
	volume control left/right voltage gain tracking error		–	–	2	dB
Bass control						
G_V	bass control voltage gain maximum boost	$C_B = 33$ nF f = 40 Hz	14	15	16	dB
	maximum attenuation	f = 40 Hz	11	12	13	dB
ΔG_V	bass control voltage gain step width		1	1.5	2	dB
$G_{V(\text{extended})}$	extended bass control voltage gain maximum boost	see Fig.1 f = 60 Hz	18	19	20	dB
	maximum attenuation	f = 60 Hz	14	15	16	dB
$\Delta G_{V(\text{extended})}$	extended bass control voltage gain step width		1	2	3	dB
Treble control						
G_V	treble control voltage gain maximum boost	f = 15 kHz	11	12	13	dB
	maximum attenuation	f = 15 kHz	11	12	13	dB
ΔG_V	treble control voltage gain step width		2.5	3	3.5	dB
Effect controls						
$\alpha_{\text{ct}(\text{spat}1)}$	anti-phase crosstalk by spatial effect 1		–	52	–	%
$\alpha_{\text{ct}(\text{spat}2)}$	anti-phase crosstalk by spatial effect 2		–	30	–	%
φ	phase shift by pseudo-stereo		see Fig.3			
Loudspeaker channel outputs (pins 15 and 18)						
$V_{o(\text{max})}(\text{rms})$	maximum output signal (RMS value)	THD \leq 0.5%; $R_L >$ 10 k Ω ; $C_L <$ 1.5 nF	2	–	–	V

Universal hi-fi audio processor for TV

TDA9859

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta V_{15,18}$	maximum DC offset voltage between adjoining step and any step to mute for volume control	$G_V = 0$ to +15 dB/mute	–	2	15	mV
		$G_V = -64$ to 0 dB/mute	–	0.5	10	mV
	for bass control	$G_V = 0$ to +15 dB/mute	–	2	15	mV
		$G_V = -12$ to 0 dB/mute	–	0.5	10	mV
	for treble control	$G_V = -12$ to +12 dB/mute	–	0.5	10	mV
R_o	output resistance		–	–	100	Ω
$R_{o(L)}$	allowed output load resistor		10	–	–	k Ω
$C_{o(L)}$	allowed output load capacitor		–	–	1.5	nF
$V_{no(W)}$	weighted noise voltage at output (quasi-peak level)	CCIR 468-3 weighted				
		$G_V = +15$ dB	–	102	–	μ V
		$G_V = 0$ dB	–	32	–	μ V
		$G_V = -40$ dB	–	27	–	μ V
		$G_V = -80$ dB (mute)	–	20	–	μ V
B_{-1} dB	–1 dB bandwidth for loudspeaker channel		20	–	20000	Hz
THD	total harmonic distortion for $V_{i(rms)} = 0.2$ V for $V_{i(rms)} = 1$ V for $V_{i(rms)} = 2$ V	$f = 20$ to 12500 Hz				
		$G_V = -30$ to +15 dB	–	0.1	0.3	%
		$G_V = -30$ to 0 dB	–	0.1	0.3	%
		$G_V = -30$ to –6 dB	–	0.1	0.3	%
$\alpha_{cs(l-r)}$	stereo channel separation	$f = 10$ kHz; $G_V = 0$ dB; opposite input grounded by 1 k Ω resistor	–	75	–	dB
$\alpha_{ct(bus)}$	crosstalk from I ² C-bus to AF outputs $\alpha_{bus} = 20 \log \frac{V_{bus(p-p)}}{V_{o(rms)}}$ (V_{bus} = spurious I ² C-bus signal voltage on AF output).	$G_V = 0$ dB	–	100	–	dB
$PSRR_{100}$	power supply ripple rejection with 100 Hz ripple	$G_V = 0$ dB; $V_{R(rms)} < 200$ mV	–	55	–	dB
SCART output (pins 7 and 26)						
$V_{o(max)(rms)}$	maximum output signal (RMS value)	THD $\leq 0.5\%$; $R_L > 5$ k Ω	2	–	–	V
$R_{o(L)}$	output load resistor		5	–	–	k Ω
Power-on reset						
V_{PONR}	increasing supply voltage start of reset end of reset		–	–	2.5	V
			5.2	6.0	6.8	V
V_{PONR}	decreasing supply voltage start of reset		4.4	5.2	6.0	V
I²C-bus, SCL and SDA (pins 16 and 17)						
V_{IH}	HIGH-level input voltage		3	–	V_P	V

Universal hi-fi audio processor for TV

TDA9859

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{IL}	LOW-level input voltage		0	–	1.5	V
I _I	input current		–	–	±10	μA
V _{ACK}	output voltage at acknowledge (pin 17)	I ₁₇ = –3 mA	–	–	0.4	V
Module address (pin 25)						
V _{IL}	LOW-level input voltage		0	–	1.5	V
V _{IH}	HIGH-level input voltage		3	–	V _P	V
Port outputs P1 and P2 (open-collector outputs pins 2 and 31)						
V _{OL}	LOW-level output voltage	I _{O(sink)} = 1 mA	–	–	0.3	V
I _{O(sink)}	port output sink current		–	–	1	mA

Universal hi-fi audio processor for TV

TDA9859

I²C-BUS PROTOCOL

This circuit operates as a slave receiver only. For more information about the I²C-bus, see "The I²C-bus and how to use it", order number 9398 393 40011.

I²C-bus format

S	SLAVE ADDRESS	\bar{W}	A	SUBADDRESS	A	DATA ⁽¹⁾	A ⁽¹⁾	P
---	---------------	-----------	---	------------	---	---------------------	------------------	---

Note

- Multiple DATA-A (acknowledge) sequences may occur.

Table 1 Explanation of I²C-bus format

NAME	DESCRIPTION
S	START condition (SCL HIGH, SDA HIGH-to-LOW)
SLAVE ADDRESS	100 0000 ($V_{25} = \text{LOW}$) or 100 0001 ($V_{25} = \text{HIGH}$)
\bar{W}	0
A	acknowledge (SDA = LOW); generated by the device
SUBADDRESS	subaddress (byte); see Table 2
DATA ⁽¹⁾	data byte; see Table 2
P	STOP condition (SCL = HIGH, SDA = LOW-to-HIGH)

Note

- If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed by the device.

Table 2 I²C-bus transmission

FUNCTION	SUBADDRESS		DATA BITS							
	BINARY	HEX	D7	D6	D5	D4	D3	D2	D1	D0
Loudspeaker channel										
Volume control common	0000 0000	00	0	0	V05	V04	V03	V02	V01	V00
Volume control left	0000 0001	01	0	0	0	VL4	VL3	VL2	VL1	VL0
Volume control right	0000 0010	02	0	0	0	VR4	VR3	VR2	VR1	VR0
Bass control	0000 0011	03	0	0	0	BA4	BA3	BA2	BA1	BA0
Treble control	0000 0100	04	0	0	0	0	TR3	TR2	TR1	TR0
Switching control byte										
SCART output ⁽¹⁾	0000 1000	08	0	MU1	P1	P2	I13	I12	I11	I10
Loudspeaker output	0000 1001	09	EF2	MU2	EF1	ST	I23	I22	I21	I20

Note

- If auto-increment of the subaddress is used, it is necessary to insert three dummy data words between the treble control byte and the switching control bytes.

Universal hi-fi audio processor for TV

TDA9859

Table 3 Function of the bits in Table 2

BITS	FUNCTION
V00 to V05	volume control common for loudspeaker channel; see Table 9
VL0 to VL4	volume control for left loudspeaker channel; see Table 6
VR0 to VR4	volume control for right loudspeaker channel; see Table 6
BA0 to BA4	bass control for left and right loudspeaker channels; see Table 7
TR0 to TR3	treble control for left and right loudspeaker channels; see Table 8
I10 to I13	input selection for SCART channels; see Table 4
I20 to I23	input selection for loudspeaker channels; see Table 4
MU1 and MU2	mute control bits (MU1 for SCART channel, MU2 for loudspeaker channel) 0 = channel not muted 1 = channel muted
EF1, EF2 and ST	effect control bits for loudspeaker channel; see Table 5
P1 and P2	control bits for ports P1 (pin 2) and P2 (pin 31) control bit = 0: ports P1 = LOW control bit = 1: ports P1 = HIGH

Table 4 Input selection

INPUT	BITS OF DATA BYTE 8 AND 9								
	HEX	D7	D6	D5	D4	D3	D2	D1	D0
AUX LEFT	XB ⁽¹⁾	(1)	MU	(1)	(1)	1	0	1	1
AUX RIGHT	X9 ⁽¹⁾	(1)	MU	(1)	(1)	1	0	0	1
AUX STEREO	X7 ⁽¹⁾	(1)	MU	(1)	(1)	0	1	1	1
SCART LEFT	XA ⁽¹⁾	(1)	MU	(1)	(1)	1	0	1	0
SCART RIGHT	X5 ⁽¹⁾	(1)	MU	(1)	(1)	0	1	0	1
SCART STEREO	X6 ⁽¹⁾	(1)	MU	(1)	(1)	0	1	1	0
MAIN LEFT	XC ⁽¹⁾	(1)	MU	(1)	(1)	1	1	0	0
MAIN RIGHT	XD ⁽¹⁾	(1)	MU	(1)	(1)	1	1	0	1
MAIN STEREO	X8 ⁽¹⁾	(1)	MU	(1)	(1)	1	0	0	0

Note

- Byte 8 (SCART channels): The value of X depends on MU1 and control bits P1 and P2.
Byte 9 (loudspeaker channels): see Table 5 for the programming of these bits. The value of X depends on the selected effects and MU2.

Universal hi-fi audio processor for TV

TDA9859

Table 5 Effect controls

SETTING SPECIAL EFFECTS	DATA BYTE TO SUBADDRESS 09								
	HEX	EF2	MU2	EF1	ST	I23	I22	I21	I20
Stereo with spatial effect 1 (52%)	BX ⁽¹⁾	1	0	1	1	(1)	(1)	(1)	(1)
Stereo with spatial effect 2 (30%)	3X ⁽¹⁾	0	0	1	1	(1)	(1)	(1)	(1)
Stereo without spatial effect	1X ⁽¹⁾	0	0	0	1	(1)	(1)	(1)	(1)
Forced mono with pseudo stereo	2X ⁽¹⁾	0	0	1	0	(1)	(1)	(1)	(1)
Forced mono without pseudo stereo	0X ⁽¹⁾	0	0	0	0	(1)	(1)	(1)	(1)

Note

1. See Table 4. The value of X depends on the selected input.

Table 6 Volume control left/right

G _v (dB)	DATA BITS					
	HEX	VL4	VL3	VL2	VL1	VL0
		VR4	VR3	VR2	VR1	VR0
0	1F	1	1	1	1	1
-1	1E	1	1	1	1	0
-2	1D	1	1	1	0	1
-3	1C	1	1	1	0	0
-4	1B	1	1	0	1	1
-5	1A	1	1	0	1	0
-6	19	1	1	0	0	1
-7	18	1	1	0	0	0
-8	17	1	0	1	1	1
-9	16	1	0	1	1	0
-10	15	1	0	1	0	1
-11	14	1	0	1	0	0
-12	13	1	0	0	1	1
-13	12	1	0	0	1	0
-14	11	1	0	0	0	1
-15	10	1	0	0	0	0
-16	0F	0	1	1	1	1
-17	0E	0	1	1	1	0
-18	0D	0	1	1	0	1
-19	0C	0	1	1	0	0
-20	0B	0	1	0	1	1
-21	0A	0	1	0	1	0
-22	09	0	1	0	0	1
-23	08	0	1	0	0	0
Mute	07	0	0	1	1	1

Table 7 Bass control

G _v (dB)	DATA BITS					
	HEX	BA4	BA3	BA2	BA1	BA0
+15	19	1	1	0	0	1
+13.5	18	1	1	0	0	0
+12	17	1	0	1	1	1
+10.5	16	1	0	1	1	0
+9	15	1	0	1	0	1
+7.5	14	1	0	1	0	0
+6	13	1	0	0	1	1
+4.5	12	1	0	0	1	0
+3	11	1	0	0	0	1
+1.5	10	1	0	0	0	0
0	0F	0	1	1	1	1
0	0E	0	1	1	1	0
-1.5	0D	0	1	1	0	1
-3	0C	0	1	1	0	0
-4.5	0B	0	1	0	1	1
-6	0A	0	1	0	1	0
-7.5	09	0	1	0	0	1
-9	08	0	1	0	0	0
-10.5	07	0	0	1	1	1
-12	06	0	0	1	1	0

Universal hi-fi audio processor for TV

TDA9859

Table 8 Treble control

G _v (dB)	DATA BITS					
	HEX	0	TR3	TR2	TR1	TR0
+12	0A	0	1	0	1	0
+9	09	0	1	0	0	1
+6	08	0	1	0	0	0
+3	07	0	0	1	1	1
0	06	0	0	1	1	0
-3	05	0	0	1	0	1
-6	04	0	0	1	0	0
-9	03	0	0	0	1	1
-12	02	0	0	0	1	0

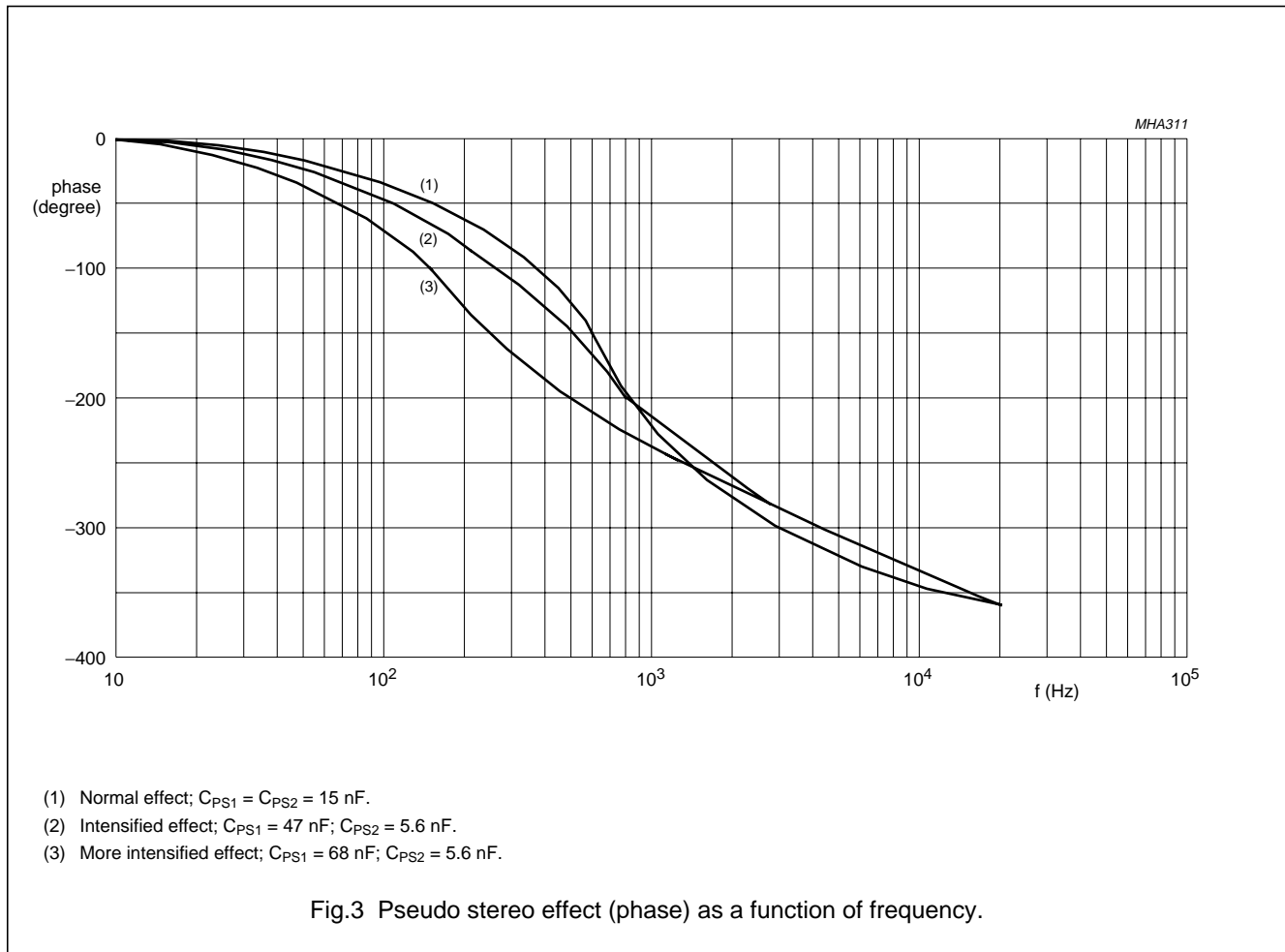
Table 9 Volume control common

G _v (dB)	DATA BITS						
	HEX	V05	V04	V03	V02	V01	V00
+15	3F	1	1	1	1	1	1
+14	3E	1	1	1	1	1	0
+13	3D	1	1	1	1	0	1
+12	3C	1	1	1	1	0	0
+11	3B	1	1	1	0	1	1
+10	3A	1	1	1	0	1	0
+9	39	1	1	1	0	0	1
+8	38	1	1	1	0	0	0
+7	37	1	1	0	1	1	1
+6	36	1	1	0	1	1	0
+5	35	1	1	0	1	0	1
+4	34	1	1	0	1	0	0
+3	33	1	1	0	0	1	1
+2	32	1	1	0	0	1	0
+1	31	1	1	0	0	0	1
0	30	1	1	0	0	0	0
-1	2F	1	0	1	1	1	1
-2	2E	1	0	1	1	1	0
-3	2D	1	0	1	1	0	1
-4	2C	1	0	1	1	0	0
-5	2B	1	0	1	0	1	1
-6	2A	1	0	1	0	1	0

G _v (dB)	DATA BITS						
	HEX	V05	V04	V03	V02	V01	V00
-7	29	1	0	1	0	0	1
-8	28	1	0	1	0	0	0
-9	27	1	0	0	1	1	1
-10	26	1	0	0	1	1	0
-11	25	1	0	0	1	0	1
-12	24	1	0	0	1	0	0
-13	23	1	0	0	0	1	1
-14	22	1	0	0	0	1	0
-15	21	1	0	0	0	0	1
-16	20	1	0	0	0	0	0
-17	1F	0	1	1	1	1	1
-18	1E	0	1	1	1	1	0
-19	1D	0	1	1	1	0	1
-20	1C	0	1	1	1	0	0
-21	1B	0	1	1	0	1	1
-22	1A	0	1	1	0	1	0
-23	19	0	1	1	0	0	1
-24	18	0	1	1	0	0	0
-25	17	0	1	0	1	1	1
-26	16	0	1	0	1	1	0
-27	15	0	1	0	1	0	1
-28	14	0	1	0	1	0	0
-29	13	0	1	0	0	1	1
-30	12	0	1	0	0	1	0
-31	11	0	1	0	0	0	1
-32	10	0	1	0	0	0	0
-33	0F	0	0	1	1	1	1
-34	0E	0	0	1	1	1	0
-35	0D	0	0	1	1	0	1
-36	0C	0	0	1	1	0	0
-37	0B	0	0	1	0	1	1
-38	0A	0	0	1	0	1	0
-39	09	0	0	1	0	0	1
-40	08	0	0	1	0	0	0

Universal hi-fi audio processor for TV

TDA9859



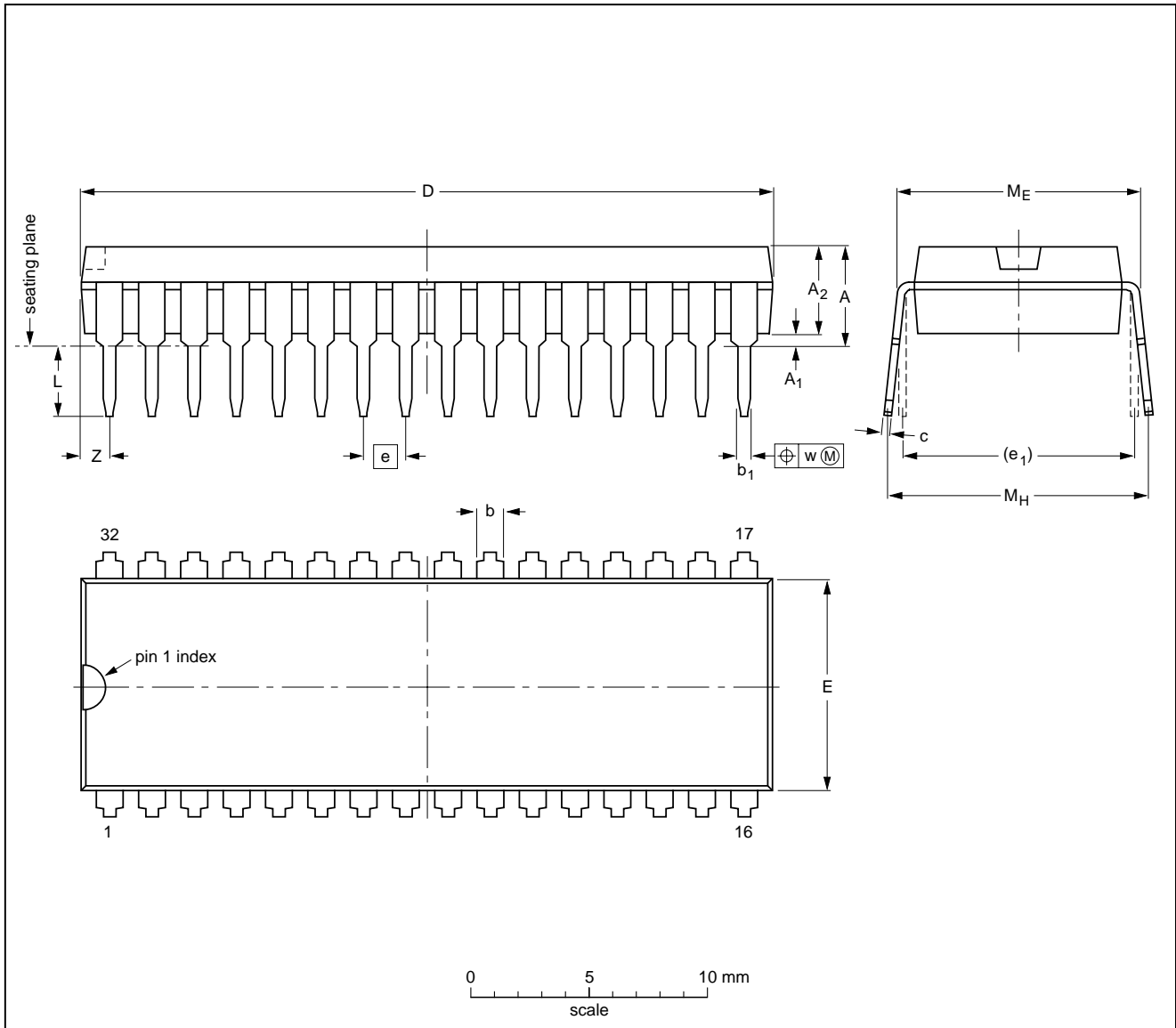
Universal hi-fi audio processor for TV

TDA9859

PACKAGE OUTLINE

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil)

SOT232-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	29.4 28.5	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT232-1						92-11-17 95-02-04

Universal hi-fi audio processor for TV

TDA9859

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact

with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

Universal hi-fi audio processor for TV

TDA9859

NOTES

Universal hi-fi audio processor for TV

TDA9859

NOTES

Universal hi-fi audio processor for TV

TDA9859

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax. +381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: <http://www.semiconductors.philips.com>

© Philips Electronics N.V. 1997

SCA55

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

547047/1200/01/pp20

Date of release: 1997 Sep 01

Document order number: 9397 750 02004

Let's make things better.

Philips
Semiconductors



PHILIPS