PI3EQX3851B

3.3V, 1-port, SATA2 *i/m* ReDriver™ with Analog Output Adjustment

Features

- SATA2 *i, m*; external SATA2
- Two 3.0Gbps differential signal pairs
- Adjustable Receiver Equalization
- 100-Ohm Differential CML I/O's
- Independent Analog output swing adjustment
- Independent Analog Output Emphasis Control
- Input signal level detect and squelch for each channel
- OOB Support
- Low Power (200mW per Channel)
- Stand-by Mode – Power Down State
- V_{DD} Operating Range: 3.3V
- Packaging:
  - − 20-TQFN (3.5x 4.5mm, ZH)
  - − 20-TQFN (4x 4mm, ZD)

Description

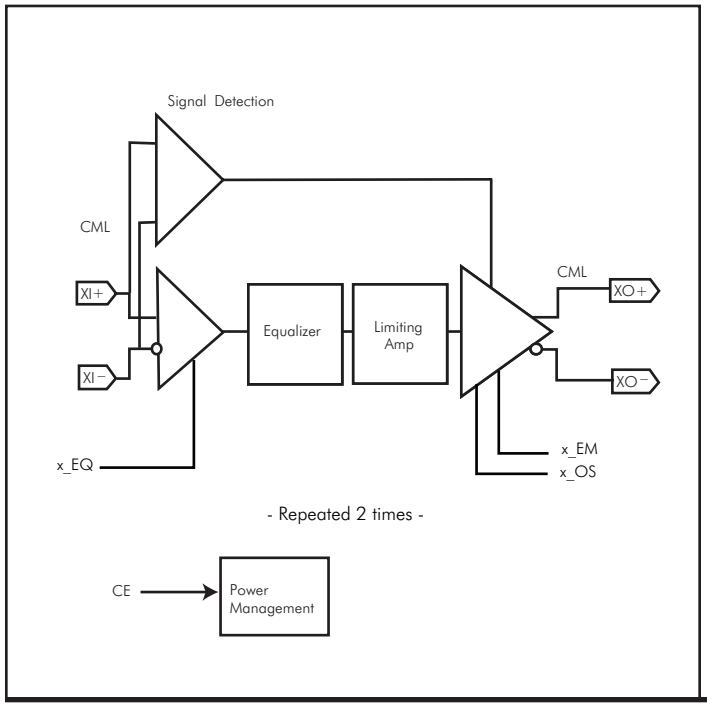
Pericom Semiconductor's PI3EQX3851B is a low power, signal ReDriver. The device provides programmable equalization, to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference. PI3EQX3851B supports two 100-Ohm Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a backplane, or to extend the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver.

A low-level input signal detection and output squelch function is provided for each channel. Each channel operates fully independently. When the channels are enabled (CE=1) and operating, that channels input signal level (on xI+/-) determines whether the output is active. If the input signal level of the channel falls below the active threshold level (Vth-) then the outputs are driven to the common mode voltage.

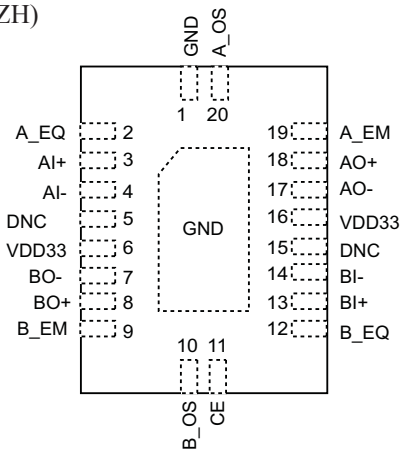
In addition to signal conditioning, when CE = 0, the device enters a low power standby mode.

Block Diagram

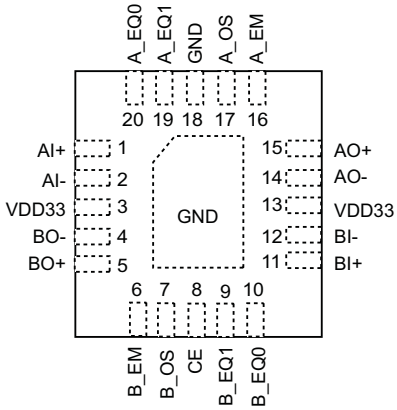


Pin Diagram (Top Side View)

3.5x4.5mm (ZH)



4x4mm (ZD)



08-0252

Pin Description

ZD Pin #	ZH Pin #	Pin Name	Type	Description
16	19	A_EM	Input	Output emphasis adjustment for channel A. Connects to resistor (tied to ground) to allow fine adjustment of emphasis level. (See Output Adjustment table.)
20 19	2 -	A_EQ0 A_EQ1	Input	Selection pin(s) for equalizer of AI±, See Input Equalizer Adjustment table. With internal 50K-Ohm pull-up resistor.
17	20	A_OS	Input	Output swing adjustment for channel A. Connects to resistor (tied to ground) to allow fine adjustment of output swing level. (See Output Swing Adjustment Table.)
1 2	3 4	AI+ AI-	Input	CML input forward channel A. With internal 50-Ohm pull up, connected to internal bias voltage.
15 14	18 17	AO+ AO-	Output	CML output channel A. With internal 50-Ohm pull up, connected to internal bias voltage.
6	9	B_EM	Input	Output emphasis adjustment for channel B. Connects to resistor (tied to ground) to allow fine adjustment of emphasis level. (See Output Adjustment table.)
10 9	12 -	B_EQ0 B_EQ1	Input	Selection pin(s) for equalizer of BI±. See Input equalizer Adjustment table. With internal 50K-Ohm pull-up resistor.
7	10	B_OS	Input	Output swing adjustment for channel B. Connects to resistor (tied to ground) to allow fine adjustment of output swing level. (See Output Adjustment Table.)
11 12	13 14	BI+ BI-	Input	CML input return channel B. With internal 50-Ohm pull up, connected to internal bias voltage.
5 4	8 7	BO+ BO-	Output	Positive CML output channel B. With internal 50-Ohm pull up, connected to internal bias voltage.
8	11	CE	Input	Chip Enable "high" provides normal operation. "Low" for power down mode. With internal 50K-Ohm pull-up resistor.
18, Center Pad	1, Center Pad	GND	GND	Supply ground.
3, 13	6, 16	VDD33	Power	3.3V supply voltage ± 10%. Place 100nF and 1nF bypass capacitors to ground, as close to the device as possible.
-	5, 15	DNC	-	Do Not Connect

Input Equalizer Adjustment (ZH)

x_EQ	Compliance Channel @ 1.5 GHz
0	3.5dB ± 1.0dB
1	7.5dB ± 1.0dB

Input Equalizer Adjustment (ZD)

x_EQ1	x_EQ0	Compliance Channel @ 1.5 GHz
0	0	3.5dB ± 1.0dB
0	1	4.5dB ± 1.0dB
1	0	6.5dB ± 1.0dB
1	1	7.5dB ± 1.0dB

Output Adjustment

Swing		Pre-emph 0dB (mV)	Pre-emph 0dB (mV)	Pre-emph 0dB (mV)	Pre-emph 0dB (mV)	Pre-emph 0dB (mV)	Pre-emph 0dB (mV)	Pre-emph 0dB (mV)	Pre-emph 0dB (mV)
dB	K-Ohm	K-Ohm	K-Ohm	K-Ohm	K-Ohm	K-Ohm	K-Ohm	K-Ohm	K-Ohm
–0.5	500	500	561	595	630	667	749	840	942
0	530	530	595	630	667	749	840	942	1057
0.5	561	561	630	667	749	840	942	1057	1187
1	595	595	667	749	840	942	1057	1187	1331
2	667	667	749	840	942	1057	1187	1331	
3	749	749	840	942	1057	1187	1331		
4	840	840	942	1057	1187	1331			
5	942	942	1057	1187	1331				
6	1057	1057	1187	1331					
7	1187	1187	1331						
8	1331	1331							

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +4.6V
DC SIG Voltage	–0.5V to V_{DD} +0.5V
Current Output	-25mA to +25mA
Power Dissipation Continuous	500mW
Operating Temperature	0 to +70°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$I_{DD-STANDBY}$	I_{DD} Current, Standby	CE = LVCMOS Low			0.55	mA
$I_{DD-ACTIVE}$	I_{DD} Current, Active	CE = LVCMOS High			100	
$P_{STANDBY}$	Supply Power, Standby	CE = LVCMOS Low			2	mW
P_{ACTIVE}	Supply Power, Active	CE = LVCMOS High			360	
t_{PD}	Latency	From input to output		2.0		ns
CML Receiver Input						
Z_{RX-DC}	DC Input Impedance		40	50	60	Ohm
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance		80	100	120	
$V_{RX-DIFFP-P}$	Differential Input Peak-to-peak Voltage		0.200			V
$V_{RX-CM-ACP}$	AC Peak Common Mode Input Voltage				150	mV
V_{TH-SD}	Signal detect Threshold	CE = 1	50(2)		200 (3)	mVppd
S_{dd11_RX}	RX differential mode return loss	75MHz-300MHz 300MHz-600MHz 600MHz-1.2GHz 1.2GHz-2.4GHz 2.4GHz-3.0GHz 3.0 GHz-5.0GHz	18 14 10 8 3 1			dB
S_{cc11_RX}	RX common mode return loss	150MHz-600MHz 600MHz-1.2GHz 1.2GHz-5.0GHz	5 2 1			dB
S_{dc11_RX}	RX impedance balance	150MHz-600MHz 600MHz-1.2GHz 1.2GHz-2.4GHz 2.4GHz-5.0GHz	30 20 10 4			dB
Equalization						
J_{RS}	Residual Jitter(1,2)	Total Jitter			0.3	Ulp-p
J_{RM}	Random Jitter(1,2)			1.5		psrms

Notes

1. K28.7 pattern is applied differentially at point A as shown in Figure 1.
2. Total jitter does not include the signal source jitter. Total jitter (TJ) = (14.1 × RJ + DJ) where RJ is random RMS jitter and DJ is maximum deterministic jitter. Signal source is a K28.5 ± pattern (00 1111 1010 11 0000 0101) for the deterministic jitter test and K28.7 (0011111000) or equivalent for random jitter test. Residual jitter is that which remains after equalizing media-induced losses of the environment of Figure 1 or its equivalent. The deterministic jitter at point B must be from media-induced loss, and not from clock source modulation. Jitter is measured at 0V at point C of Figure 1.
3. Using Compliance test at 1.5Gbps and 3Gbps. Also using OOB (OOB is formed by ALIGNp primitive or D24.3) test patterns at 1.5Gbps. The ALIGN primitive (K28.5+D10.2+D27.3 = 0011111010+0101010101+0010011100). The D24.3 = 00110011001100110011

AC/DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
CML Transmitter Output (100Ω differential)						
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance		80	100	120	Ohm
$V_{TX-DIFFP-P}$	Differential Peak-to-peak Output Voltage	$V_{TX-DIFFP-P} = 2 * \lvert V_{TX-D+} - V_{TX-D-} \rvert$	250		800	mV
		For ROS=3.2K, REM=7.3K	475		525	
V_{TX-C}	Common-Mode Voltage	$\lvert V_{TX-D+} + V_{TX-D-} \rvert /2$	1		1.8	V
t_F, t_R	Transition Time	20% to 80%(1)			150	ps
t_F-t_R	Mis-match Transition Time	3G only; HFTP, MFTP			20	%
V_{amp_bal}	TX amplitude imbalance	3G only; HFTP, MFTP			10	%
T_{skew}	TX differential skew	1.5G and 3G; HFTP, MFTP			20	ps
V_{cm_ac}	TX AC common mode voltage	3G only; MFTP			50	mVpp
V_{cmOOB}	OOB common mode delta voltage				50	mV
$V_{diffOOB}$	OOB differential delta voltage				25	
$V_{TX-Pre-Ratio-max}$	Max TX Pre-emphasis Level				4	dB
S_{dd11_TX}	TX differential mode return loss	75MHz-300MHz 300MHz-600MHz 600MHz-2.4GHz 2.4GHz-3.0GHz 3.0 GHz-5.0GHz	14 18 6 3 1			dB
S_{cc11_TX}	TX common mode return loss	150MHz-300MHz 300MHz-600MHz 600MHz-1.2GHz 1.2GHz-5.0GHz	8 5 2 1			dB
S_{dc11_TX}	TX impedance balance	150MHz-300MHz 300MHz-600MHz 600MHz-2.4GHz 2.4GHz-5.0GHz	30 20 10 4			dB
LVCMOS Control Pins						
V_{IH}	Input High Voltage		0.65 × V_{DD}			V
V_{IL}	Input Low Voltage				0.35 × V_{DD}	
I_{IH}	Input High Current				5	µA
I_{IL}	Input Low Current				100	

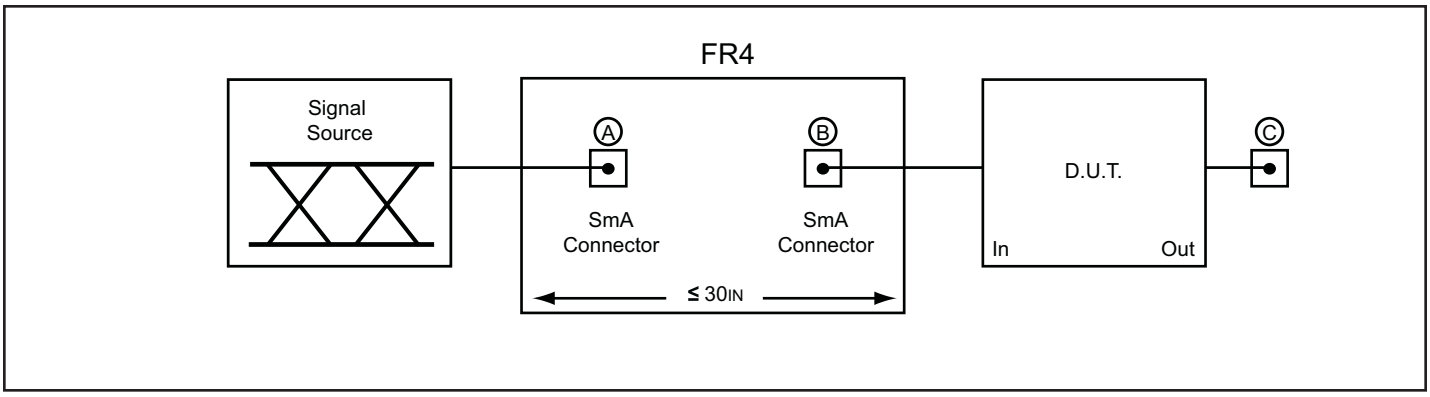


Figure 1. Test Condition Referenced in the Electrical Characteristic Table

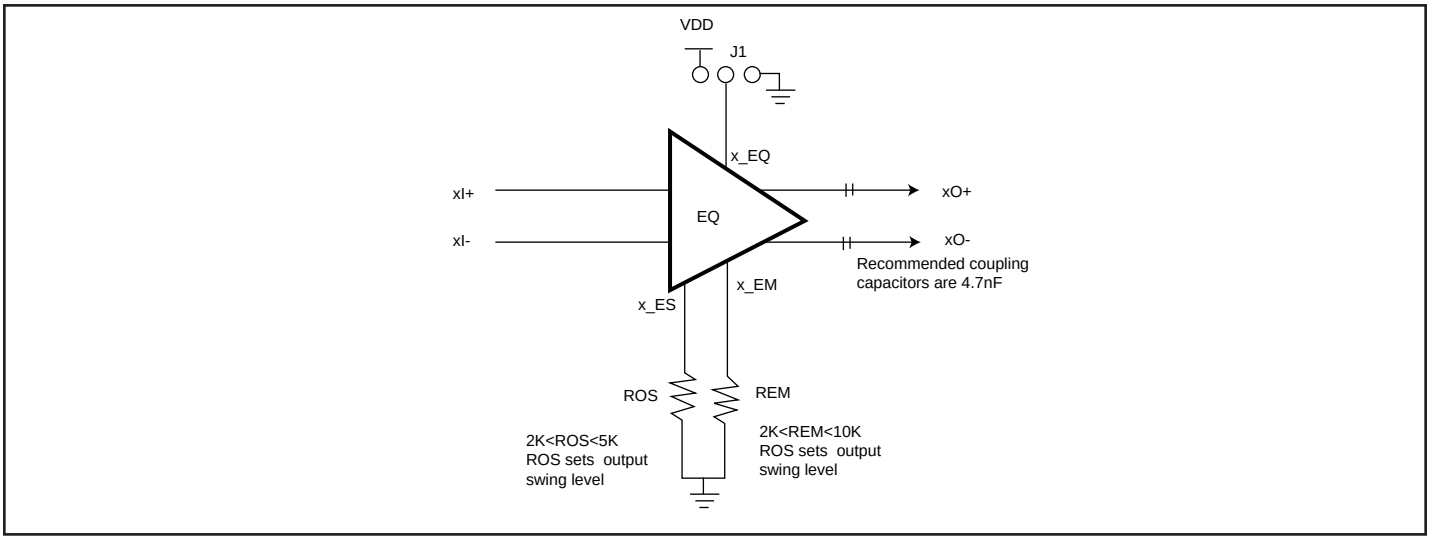
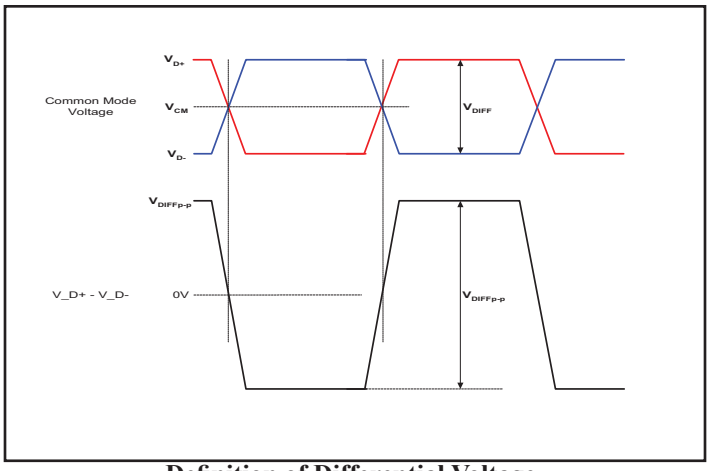
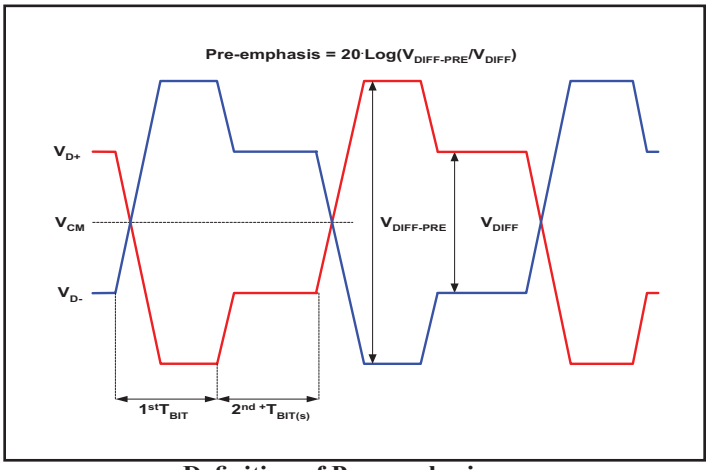


Figure 2. System Implementation Diagram

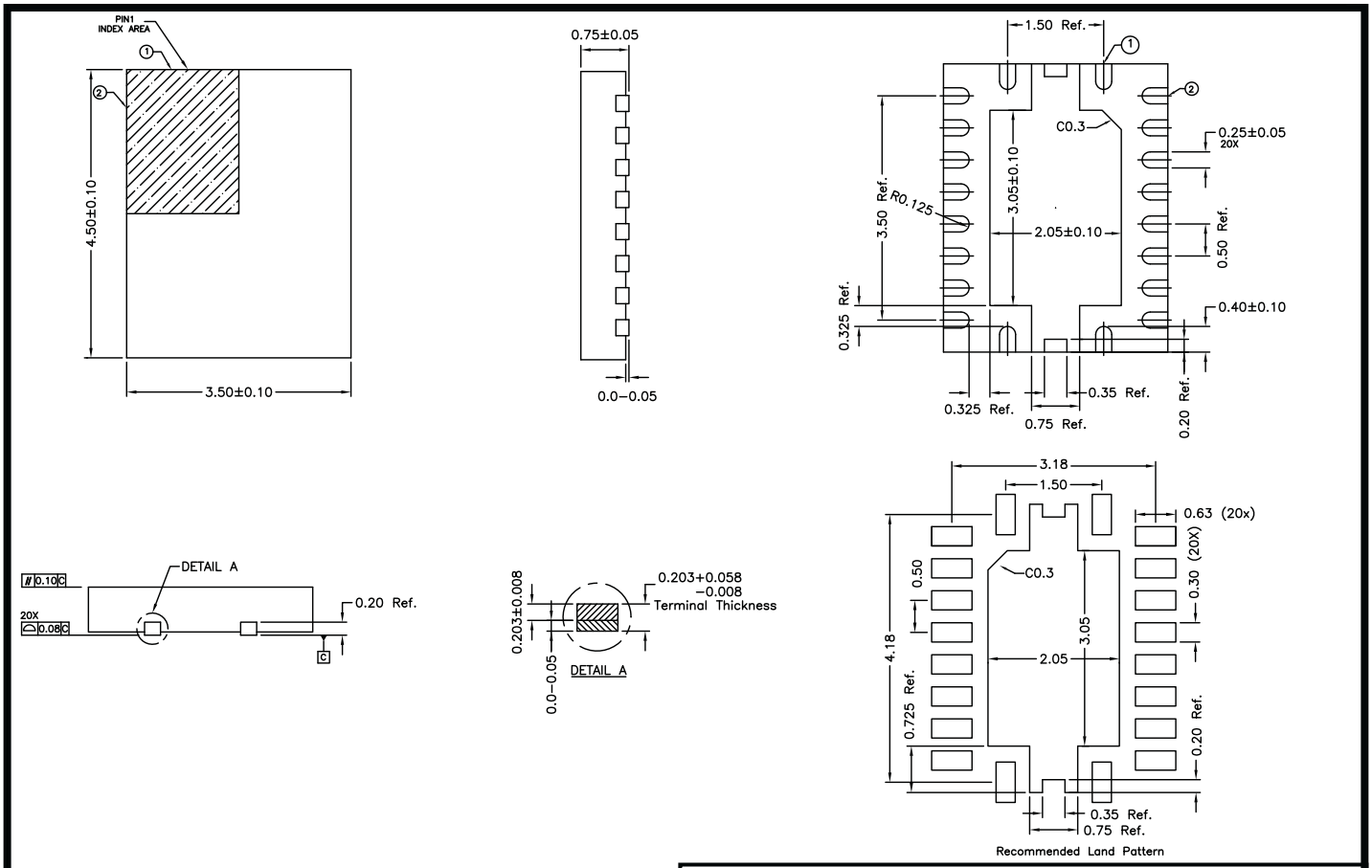


Definition of Differential Voltage and Differential Voltage Peak-to-Peak



Definition of Pre-emphasis

Packaging Mechanical: 20-contact TQFN (ZH)



NOTE :

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO–241

PERICOM Semiconductor Corporation

DATE: 03/14/08

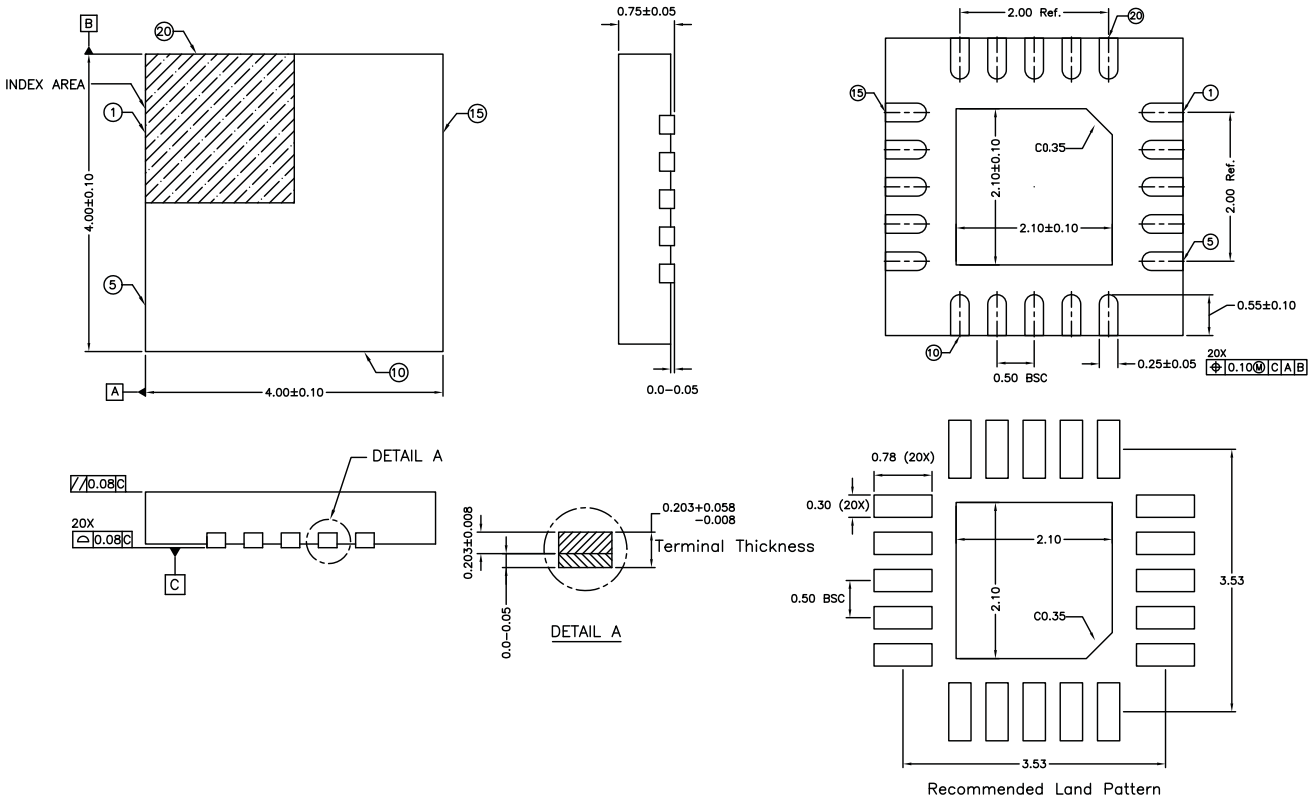
DESCRIPTION: 20-Contact, Very Thin Quad Flat No-Lead, TQFN

PACKAGE CODE: ZH20

DOCUMENT CONTROL #: PD-2032 REVISION: A

08-0122

Packaging Mechanical: 20-contact TQFN (ZD)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.08 mm.
4. REFER JEDEC MO–220.

PERICOM Semiconductor Corporation — DATE: 09/11/08

DESCRIPTION: 20-Lead, Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZD20

DOCUMENT CONTROL #: PD-2084 REVISION: --

08-0456

Ordering Information

Ordering Number	Package Code	Package Description
PI3EQX3851BZHE	ZH	Pb-Free and Green 20-contact TQFN (3.5x4.5mm)
PI3EQX3851BZDE	ZD	Pb-Free and Green 20-contact TQFN (4x4mm)

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel