PI3EQX3811C

3.3V, 1-Port, SATA2 *i/m* ReDriver™ with Equalization and Output Emphasis

Features

- SATA *i/m* output drive
- Two 3.2Gbps differential signal pairs
- Adjustable Output Emphasis
- 100-Ohm Differential CML I/O's
- Input signal level detect and squelch for each channel
- OOB fully supported
- Low Power (180mW per Channel)
- Stand-by Mode – Power Down State
- V_{DD} Operating Range: 3.3V ± 10%
- Packaging (Pb-free & Green):
  → 20-lead SSOP

Description

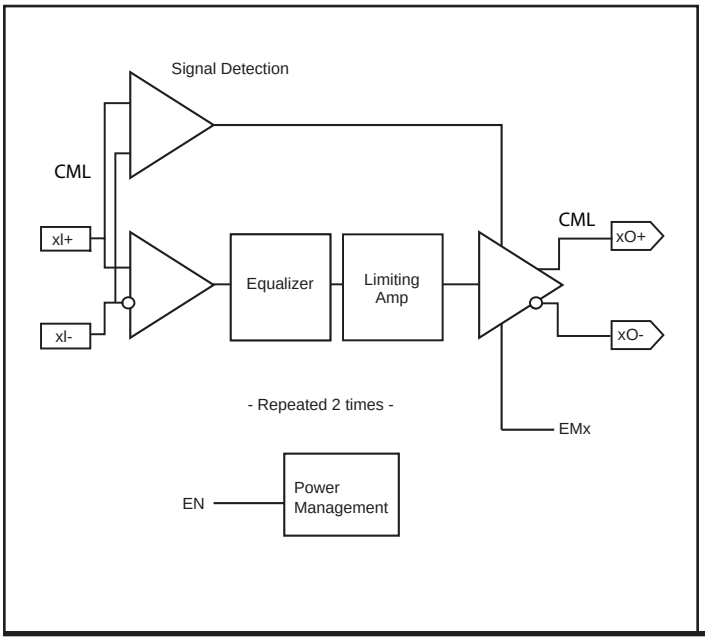
Pericom Semiconductor's PI3EQX3811C ReDriver is a low-power signal conditioner. The device provides programmable output emphasis by using 2 select bits, EMA and EMB, to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference. PI3EQX3811C supports two 100-Ohm Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a backplane, or to extend the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver. Whereas the integrated de-emphasis circuitry provides flexibility with signal integrity of the signal after the ReDriver.

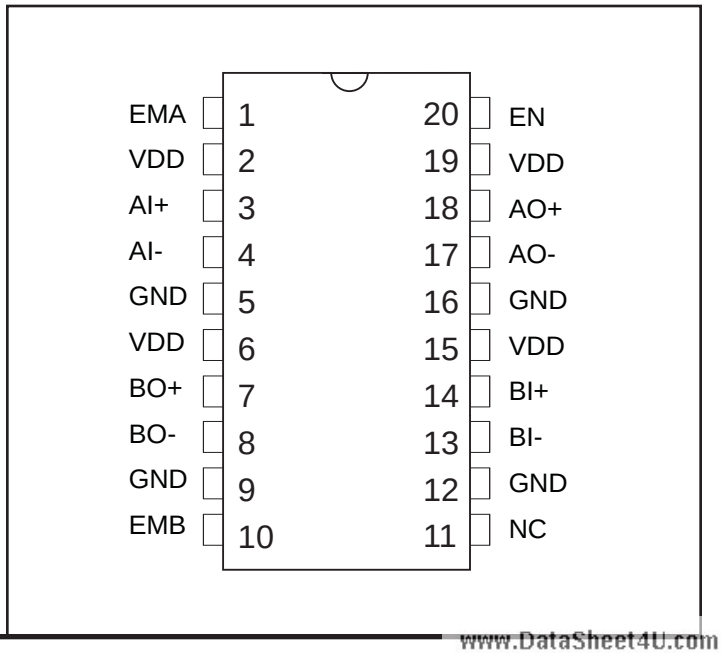
A low-level input signal detection and output squelch function is provided for each channel. Each channel operates fully independently. When the channels are enabled (EN=1) and operating, a channel's input signal level (on xI+/-) determines whether the output is enabled. If the input level of the channel falls below the active threshold level (Vth-) then the outputs are driven to the common mode voltage.

In addition to providing signal re-conditioning, Pericom's PI3EQX3811C also provides power management Stand-by mode operated by the Enable pin.

Block Diagram



Pin Description (Top-Side view)



Pin Description

Pin #	Pin Name	I/O	Description
3 4	AI+ AI-	I I	CML Inputs Channel A with internal 50-Ohm pull-up to internal bias voltage
18 17	AO+ AO-	O O	CML Outputs Channel A with internal 50-Ohm pull-up to internal bias voltage
14 13	BI+ BI-	I I	CML Inputs Channel B with internal 50-Ohm pull-up to internal bias voltage
7 8	BO+ BO-	O O	CML Outputs Channel B with internal 50-Ohm pull-up to internal bias voltage
20	EN	I	EN is the enable pin with 50K-Ohm internal pull-up to V_{DD}. A LVCMOS high provides normal operation. A LVCMOS low selects a low power down mode.
5, 9, 12, 16	GND	PWR	Supply Ground
1 10	EMA EMB	I I	Selection pins for output emphasis level (see Output Emphasis Selection Table), with 50k-Ohm internal pull-up to V_{DD}.
2, 6, 15, 19	V_{DD}	PWR	3.3V ±10% Supply Voltage
11	NC	-	Do Not Connect

Output Emphasis Selection

EMx	Emphasis Level
0	0dB
1	3dB

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C
Supply Voltage to Ground Potential ..... –0.5V to +4.6V
DC SIG Voltage ..... –0.5V to V_{DD} +0.5V
Current Output ..... -25mA to +25mA
Power Dissipation Continuous 500mW
Operating Temperature ..... 0 to +70°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Power Supply Voltage		3.0		3.6	V
$I_{DD-STANDBY}$	I_{DD} Current, Standby	EN = LVCMOS Low, V_{DD} = 3.6V			0.55	mA
$I_{DD-ACTIVE}$	I_{DD} Current, Active	EN = LVCMOS High, V_{DD} = 3.6V			100	mA
$P_{STANDBY}$	Supply Power, Standby	EN = LVCMOS Low, V_{DD} = 3.6V			2	mW
P_{ACTIVE}	Supply Power, Active	EN = LVCMOS High, V_{DD} = 3.6V			360	
	Latency	From input to output		2.0		ns
CML Receiver Input						
Z_{RX-DC}	DC Input Impedance		40	50	60	Ohm
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance		80	100	120	
$V_{RX-DIFFP-P}$	Differential Input Peak-to-peak Voltage		0.200			V
$V_{RX-CM-ACP}$	AC Peak Common Mode Input Voltage				150	mV
V_{TH-SD}	Signal Detect Threshold[1]	EN = High	65		200	
RL_{dd11_RX}	RX differential mode return loss	75MHz-300MHz 300MHz-600MHz 600MHz-1.2GHz 1.2GHz-2.4GHz 2.4GHz-3.0GHz 3.0 GHz-5.0GHz	18 14 10 8 3 1			dB
RL_{cc11_RX}	RX common mode return loss	150MHz – 300MHz 300MHZ – 600MHz 600MHz – 1.2GHz 1.2GHz – 2.4GHz 2.4GHz – 3.0GHz 3.0GHz – 5.0GHz	5 5 2 2 1 1			dB
RL_{dc11_RX}	RX impedance balance	150MHz – 300MHz 300MHz – 600MHz 600MHz – 1.2GHz 1.2GHz – 2.4GHz 2.4GHz – 3.0GHz 3.0GHz – 5.0GHz	30 30 20 10 4 4			dB

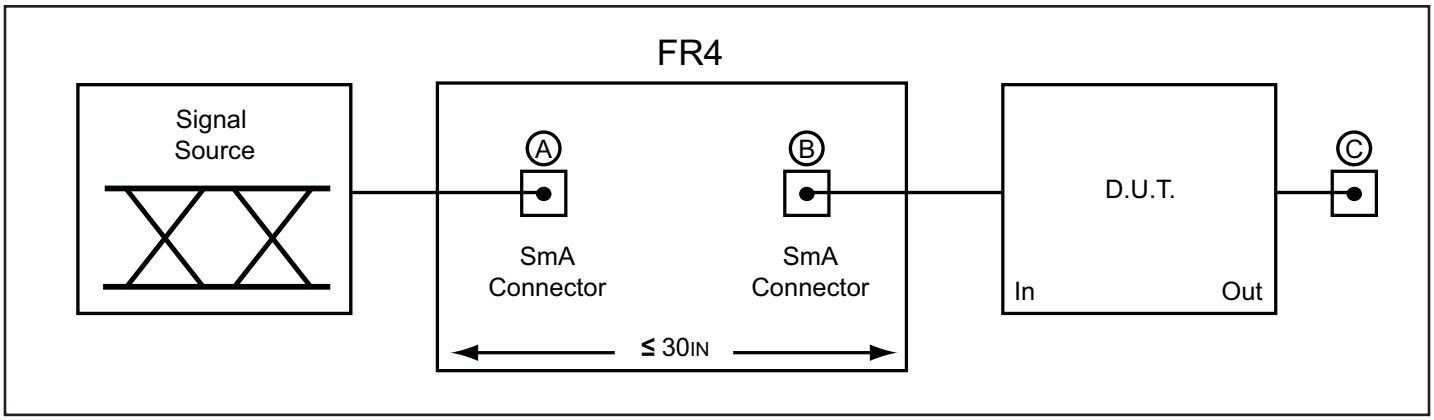
Notes
1. Using Compliance test at 1.5Gbps and 3Gbps. Also using OOB (OOB is formed by ALIGN primitive or D24.3) test patterns at 1.5Gbps. The ALIGN primitive (K28.5+D10.2+D27.3 = 0011111010+0101010101+0010011100). The D24.3 = 0011001100110011

AC/DC Electrical Characteristics

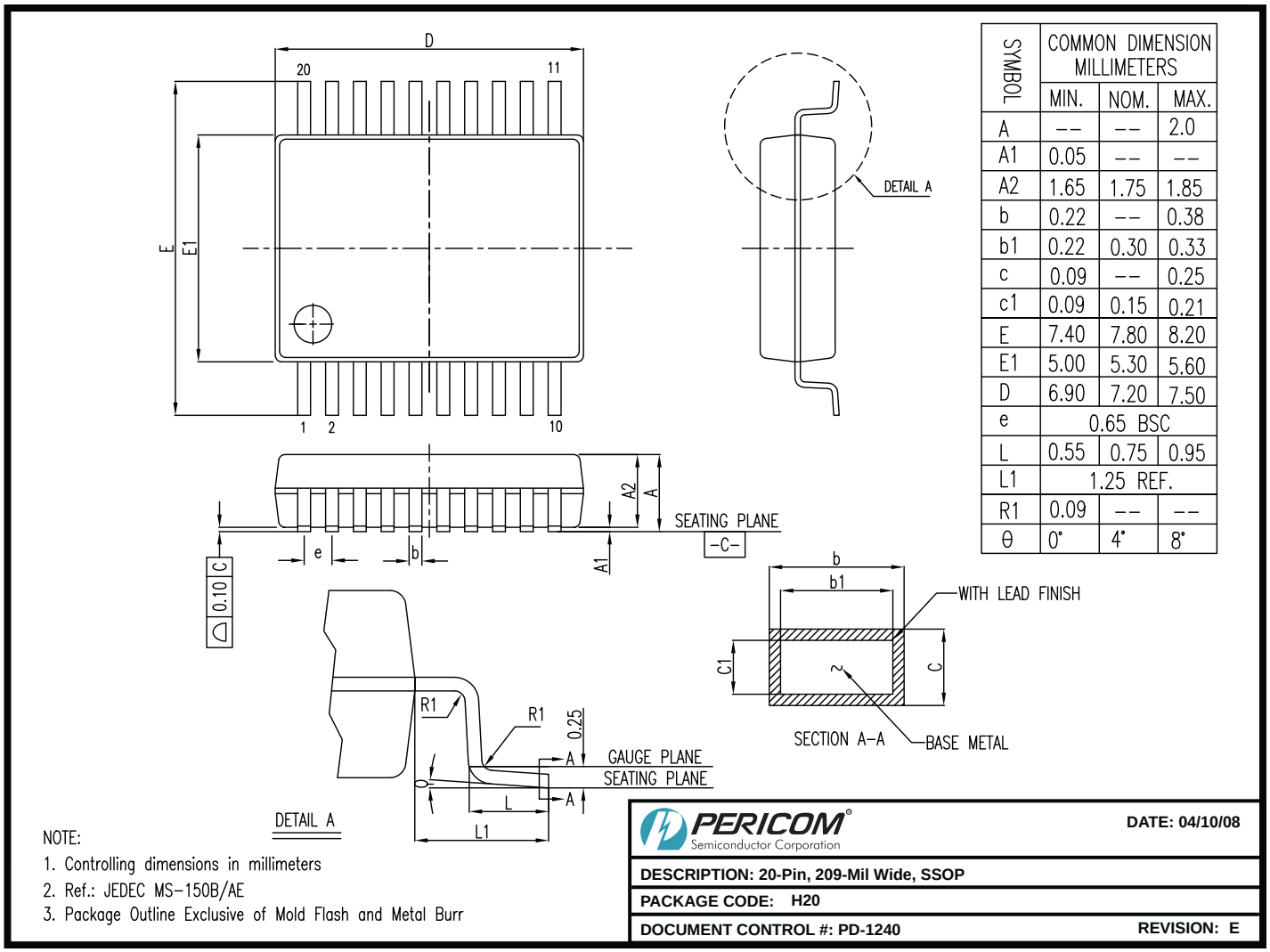
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Equalization						
T_J	Total Jitter	Measured at 3Gbps/500			0.37	UI
D_J	Deterministic Jitter	Measured at 3Gbps/500			0.19	UI
CML Transmitter Output (100-Ohm differential)						
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance		80	100	120	Ohm
$V_{TX-DIFFP-P}$	Differential Peak-to-peak Output Voltage	$V_{TX-DIFFP-P}$ = 2 * | V_{TX-D+} - V_{TX-D-} |	500		650	mV
V_{TX-DC}	Common-Mode Voltage(2,3)	| V_{TX-D+} + V_{TX-D-} | / 2	1.0		1.8	V
t_F, t_R	Transition Time	20% to 80% (1)			150	ps
t_F-t_R	Mis-match Transition Time	3G only; HFTP, MFTP			20	%
V_{amp_bal}	TX amplitude imbalance	3G only; HFTP, MFTP			10	%
T_{skew}	TX differential skew	1.5G and 3G; HFTP, MFTP			20	ps
V_{cm_ac}	TX AC common mode voltage	3G only; MFTP			50	mVpp
V_{cmOOB}	OOB common mode delta voltage				50	mV
$V_{diffOOB}$	OOB differential delta voltage				25	mV
t_{OOB}	Output OOB enable/disable time				5	nS
$V_{TX-Pre-Ratio-max}$	Max TX Pre-emphasis Level				4	dB
RL_{dd11_TX}	TX differential mode return loss	150MHz – 300MHz 300MHz – 600MHz 600MHz – 1.2GHz 1.2GHz – 2.4GHz 2.4GHz – 3.0GHz 3.0 GHz – 5.0GHz	14 8 6 6 3 1			dB
RL_{cc11_TX}	TX common mode return loss	150MHz – 300MHz 300MHz – 600MHz 600MHz – 1.2GHz 1.2GHz – 2.4GHz 2.4GHz – 3.0GHz 3.0 GHz – 5.0GHz	5 5 2 2 1 1			dB
RL_{dc11_TX}	TX impedance balance	150MHz – 300MHz 300MHz – 600MHz 600MHz – 1.2GHz 1.2GHz – 2.4GHz 2.4GHz – 3.0GHz 3.0 GHz – 5.0GHz	30 20 10 10 4 4			dB
LVCMOS Control Pins						
V_{IH}	Input High Voltage		0.65 × V_{DD}			V
V_{IL}	Input Low Voltage				0.35 × V_{DD}	
I_{IH}	Input High Current				5	µA
I_{IL}	Input Low Current				100	

Notes:
1. Using K28.7 (0011111000) pattern) .
2. The parameter is determined by device characterization, and is not production tested
3. Recommended AC output coupling capacitor is 4.7nF to 12nF at each output signal pin.

Figure 1. Test Condition Referenced in the Electrical Characteristic Table



Packaging Mechanical: 20-lead SSOP (H20)



SYMBOL	COMMON DIMENSION MILLIMETERS		
	MIN.	NOM.	MAX.
A	--	--	2.0
A1	0.05	--	--
A2	1.65	1.75	1.85
b	0.22	--	0.38
b1	0.22	0.30	0.33
c	0.09	--	0.25
c1	0.09	0.15	0.21
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
D	6.90	7.20	7.50
e	0.65 BSC		
L	0.55	0.75	0.95
L1	1.25 REF.		
R1	0.09	--	--
θ	0°	4°	8°

NOTE:
1. Controlling dimensions in millimeters
2. Ref.: JEDEC MS-150B/AE
3. Package Outline Exclusive of Mold Flash and Metal Burr

PERICOM Semiconductor Corporation — DATE: 04/10/08

DESCRIPTION: 20-Pin, 209-Mil Wide, SSOP

PACKAGE CODE: H20

DOCUMENT CONTROL #: PD-1240 — REVISION: E

08-0140

Ordering Information

Ordering Number	Package Code	Package Description
PI3EQX3811CHE	H	Pb-Free and Green 20-lead SSOP

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel