MC14536B

Programmable Timer

The MC14536B programmable timer is a 24–stage binary ripple counter with 16 stages selectable by a binary code. Provisions for an on–chip RC oscillator or an external clock are provided. An on–chip monostable circuit incorporating a pulse–type output has been included. By selecting the appropriate counter stage in conjunction with the appropriate input clock frequency, a variety of timing can be achieved.

- 24 Flip–Flop Stages — Will Count From 2^0 to 2^{24}
- Last 16 Stages Selectable By Four–Bit Select Code
- 8–Bypass Input Allows Bypassing of First Eight Stages
- Set and Reset Inputs
- Clock Inhibit and Oscillator Inhibit Inputs
- On–Chip RC Oscillator Provisions
- On–Chip Monostable Output Provisions
- Clock Conditioning Circuit Permits Operation With Very Long Rise and Fall Times
- Test Mode Allows Fast Test Sequence
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	–0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	–0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Operating Temperature Range	–55 to +125	°C
T_{stg}	Storage Temperature Range	–65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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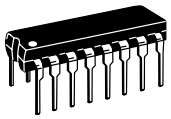
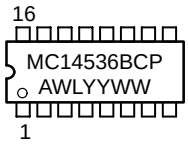
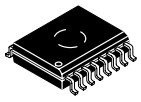
MARKING DIAGRAMS

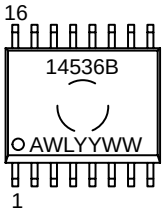


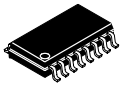
PDIP–16
P SUFFIX
CASE 648



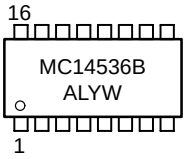


SOIC–16
DW SUFFIX
CASE 751G





SOEIAJ–16
F SUFFIX
CASE 966



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14536BCP	PDIP–16	2000/Box
MC14536BDW	SOIC–16	47/Rail
MC14536BDWR2	SOIC–16	1000/Tape & Reel
MC14536BF	SOEIAJ–16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

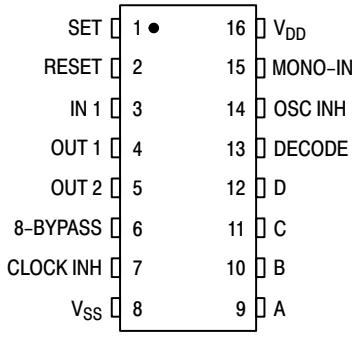


Figure 1. Pin Assignment

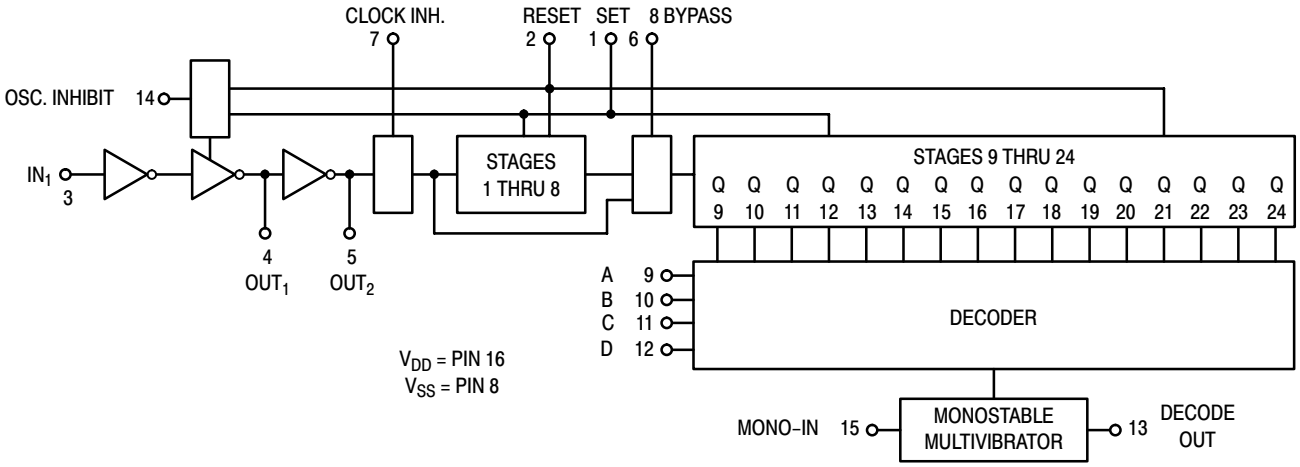


Figure 2. Block Diagram

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (Note 4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
“1” Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage “0” Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
“1” Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	– 1.2	—	– 1.0	– 1.7	—	– 0.7	—	
(V_{OH} = 4.6 Vdc) Pins 4 & 5		5.0	– 0.25	—	– 0.25	– 0.36	—	– 0.14	—	
(V_{OH} = 9.5 Vdc)		10	– 0.62	—	– 0.5	– 0.9	—	– 0.35	—	
(V_{OH} = 13.5 Vdc)		15	– 1.8	—	– 1.5	– 3.5	—	– 1.1	—	
(V_{OH} = 2.5 Vdc) Source		5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	mAdc
(V_{OH} = 4.6 Vdc) Pin 13		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
(V_{OH} = 9.5 Vdc)		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc)		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.010 0.020 0.030	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (Note 5., 6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (1.50 µA/kHz) f + I_{DD} I_T = (2.30 µA/kHz) f + I_{DD} I_T = (3.55 µA/kHz) f + I_{DD}							µAdc

4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

SWITCHING CHARACTERISTICS (Note 7.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ (Note 8.)	Max	Unit
Output Rise and Fall Time (Pin 13)	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time	t_{PLH},					ns
Clock to Q1, 8–Bypass (Pin 6) High	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 1715 ns		5.0	—	1800	3600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 617 ns		10	—	650	1300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 425 ns		15	—	450	1000	
Clock to Q1, 8–Bypass (Pin 6) Low	t_{PLH},					µs
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 3715 ns	t_{PHL}	5.0	—	3.8	7.6	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 1467 ns		10	—	1.5	3.0	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 1075 ns		15	—	1.1	2.3	
Clock to Q16	t_{PLH},					µs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 6915 ns	t_{PHL}	5.0	—	7.0	14	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 2967 ns		10	—	3.0	6.0	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 2175 ns		15	—	2.2	4.5	
Reset to Q_n	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 1415 ns		5.0	—	1500	3000	
t_{PHL} = (0.66 ns/pF) C_L + 567 ns		10	—	600	1200	
t_{PHL} = (0.5 ns/pF) C_L + 425 ns		15	—	450	900	
Clock Pulse Width	t_{WH}	5.0	600	300	—	ns
		10	200	100	—	
		15	170	85	—	
Clock Pulse Frequency	f_{cl}	5.0	—	1.2	0.4	MHz
(50% Duty Cycle)		10	—	3.0	1.5	
		15	—	5.0	2.0	
Clock Rise and Fall Time	t_{TLH},	5.0	No Limit			—
	t_{THL}	10				
		15				
Reset Pulse Width	t_{WH}	5.0	1000	500	—	ns
		10	400	200	—	
		15	300	150	—	

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

PIN DESCRIPTIONS

INPUTS

SET (Pin 1) — A high on Set asynchronously forces Decode Out to a high level. This is accomplished by setting an output conditioning latch to a high level while at the same time resetting the 24 flip–flop stages. After Set goes low (inactive), the occurrence of the first negative clock transition on IN_1 causes Decode Out to go low. The counter's flip–flop stages begin counting on the second negative clock transition of IN_1. When Set is high, the on–chip RC oscillator is disabled. This allows for very low–power standby operation.

RESET (Pin 2) — A high on Reset asynchronously forces Decode Out to a low level; all 24 flip–flop stages are also reset to a low level. Like the Set input, Reset disables the on–chip RC oscillator for standby operation.

IN_1 (Pin 3) — The device's internal counters advance on the negative–going edge of this input. IN_1 may be used as an external clock input or used in conjunction with OUT_1 and OUT_2 to form an RC oscillator. When an external clock is used, both OUT_1 and OUT_2 may be left unconnected or used to drive 1 LSTTL or several CMOS loads.

8–BYPASS (Pin 6) — A high on this input causes the first 8 flip–flop stages to be bypassed. This device essentially becomes a 16–stage counter with all 16 stages selectable. Selection is accomplished by the A, B, C, and D inputs. (See the truth tables.)

CLOCK INHIBIT (Pin 7) — A high on this input disconnects the first counter stage from the clocking source. This holds the present count and inhibits further counting. However, the clocking source may continue to run. Therefore, when Clock Inhibit is brought low, no oscillator start–up time is required. When Clock Inhibit is low, the counter will start counting on the occurrence of the first negative edge of the clocking source at IN_1.

OSC INHIBIT (Pin 14) — A high level on this pin stops the RC oscillator which allows for very low–power standby operation. May also be used, in conjunction with an external clock, with essentially the same results as the Clock Inhibit input.

MONO–IN (Pin 15) — Used as the timing pin for the on–chip monostable multivibrator. If the Mono–In input is connected to V_{SS}, the monostable circuit is disabled, and Decode Out is directly connected to the selected Q output. The monostable circuit is enabled if a resistor is connected between Mono–In and V_{DD}. This resistor and the device's internal capacitance will determine the minimum output pulse widths. With the addition of an external capacitor to V_{SS}, the pulse width range may be extended. For reliable operation the resistor value should be limited to the range of 5 kΩ to 100 kΩ and the capacitor value should be limited to a maximum of 1000 pf. (See figures 3, 4, 5, and 10).

A, B, C, D (Pins 9, 10, 11, 12) — These inputs select the flip–flop stage to be connected to Decode Out. (See the truth tables.)

OUTPUTS

OUT_1, OUT_2 (Pin 4, 5) — Outputs used in conjunction with IN_1 to form an RC oscillator. These outputs are buffered and may be used for 2^0 frequency division of an external clock.

DECODE OUT (Pin 13) — Output function depends on configuration. When the monostable circuit is disabled, this output is a 50% duty cycle square wave during free run.

TEST MODE

The test mode configuration divides the 24 flip–flop stages into three 8–stage sections to facilitate a fast test sequence. The test mode is enabled when 8–Bypass, Set and Reset are at a high level. (See Figure 8.)

TRUTH TABLES

Input					Stage Selected for Decode Out
8–Bypass	D	C	B	A	
0	0	0	0	0	9
0	0	0	0	1	10
0	0	0	1	0	11
0	0	0	1	1	12
0	0	1	0	0	13
0	0	1	0	1	14
0	0	1	1	0	15
0	0	1	1	1	16
0	1	0	0	0	17
0	1	0	0	1	18
0	1	0	1	0	19
0	1	0	1	1	20
0	1	1	0	0	21
0	1	1	0	1	22
0	1	1	1	0	23
0	1	1	1	1	24

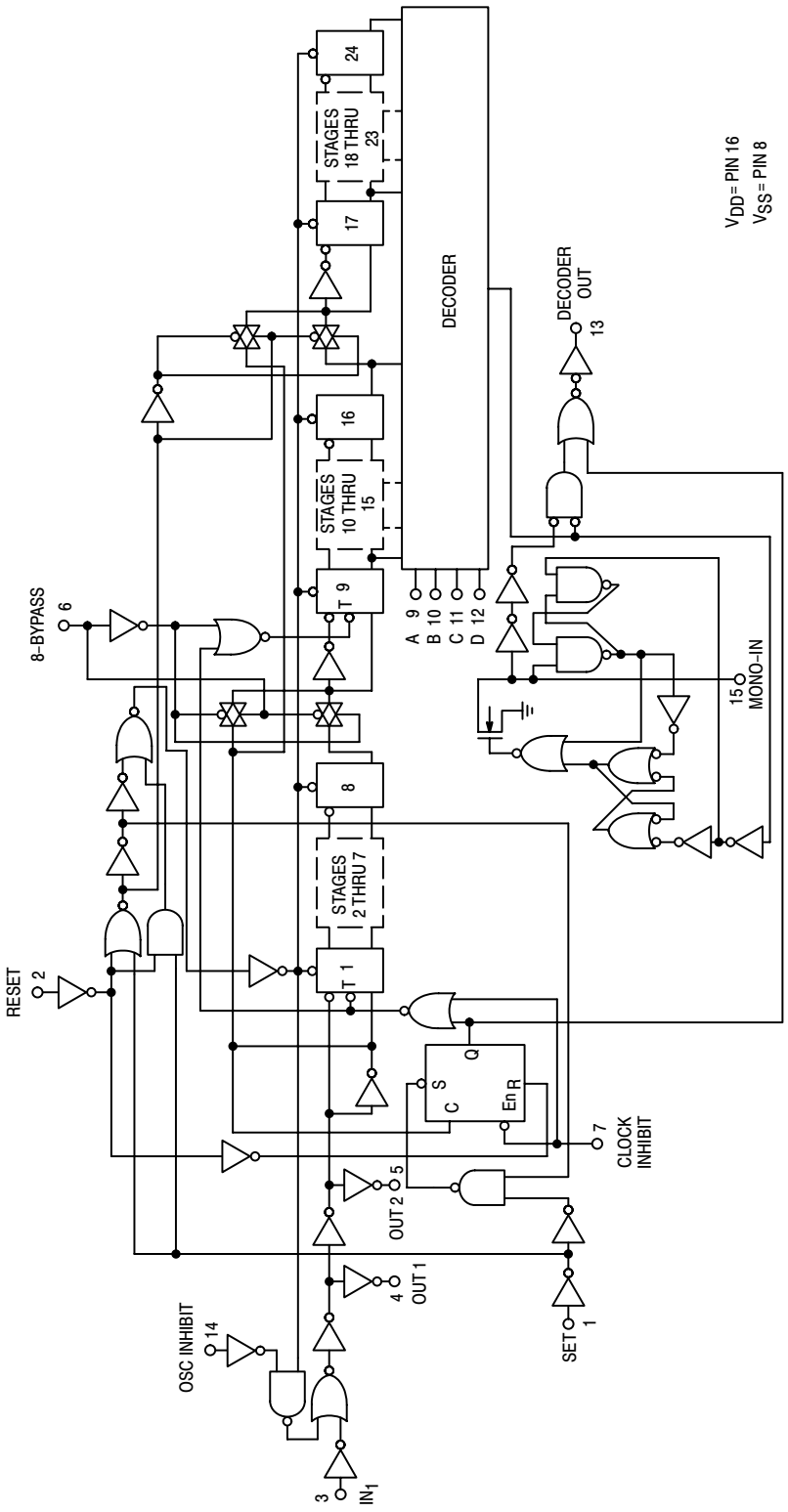
Input					Stage Selected for Decode Out
8–Bypass	D	C	B	A	
1	0	0	0	0	1
1	0	0	0	1	2
1	0	0	1	0	3
1	0	0	1	1	4
1	0	1	0	0	5
1	0	1	0	1	6
1	0	1	1	0	7
1	0	1	1	1	8
1	1	0	0	0	9
1	1	0	0	1	10
1	1	0	1	0	11
1	1	0	1	1	12
1	1	1	0	0	13
1	1	1	0	1	14
1	1	1	1	0	15
1	1	1	1	1	16

FUNCTION TABLE

In_1	Set	Reset	Clock Inh	OSC Inh	Out 1	Out 2	Decode Out
↗	0	0	0	0	↗	↘	No Change
↘	0	0	0	0	↘	↗	Advance to next state
X	1	0	0	0	0	1	1
X	0	1	0	0	0	1	0
X	0	0	1	0	—	—	No Change
X	0	0	0	1	0	1	No Change
0	0	0	0	X	0	1	No Change
1	0	0	0	↗	↘	↗	Advance to next state

X = Don’t Care

LOGIC DIAGRAM



TYPICAL RC OSCILLATOR CHARACTERISTICS

(For Circuit Diagram See Figure 11 In Application)

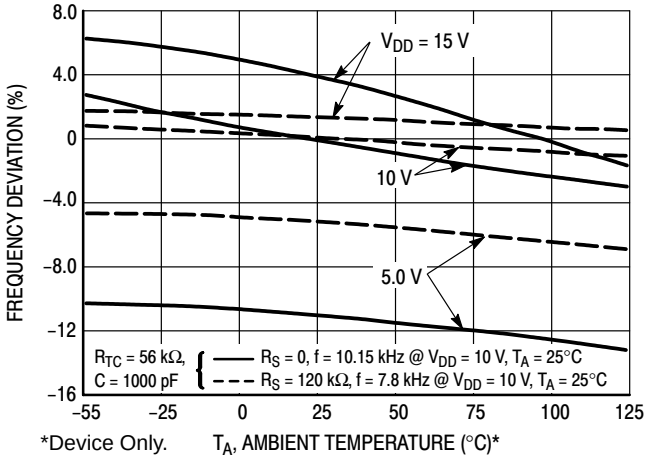


Figure 1. RC Oscillator Stability

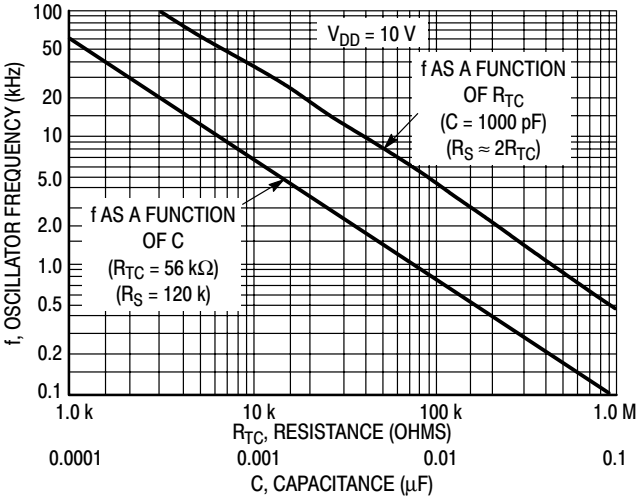


Figure 2. RC Oscillator Frequency as a Function of R_{TC} and C

MONOSTABLE CHARACTERISTICS

(For Circuit Diagram See Figure 10 In Application)

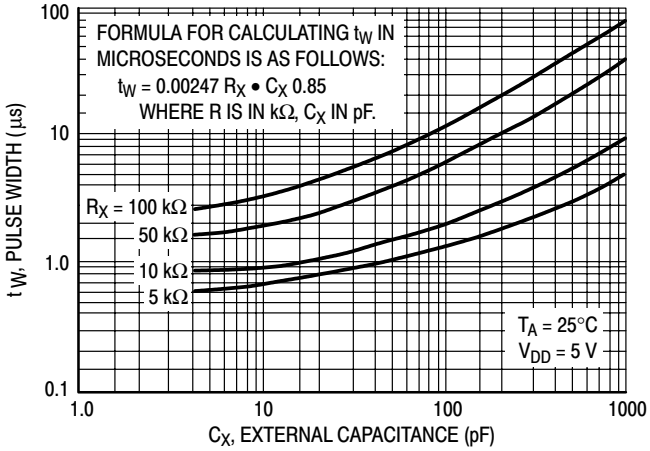


Figure 3. Typical C_X versus Pulse Width @ V_{DD} = 5.0 V

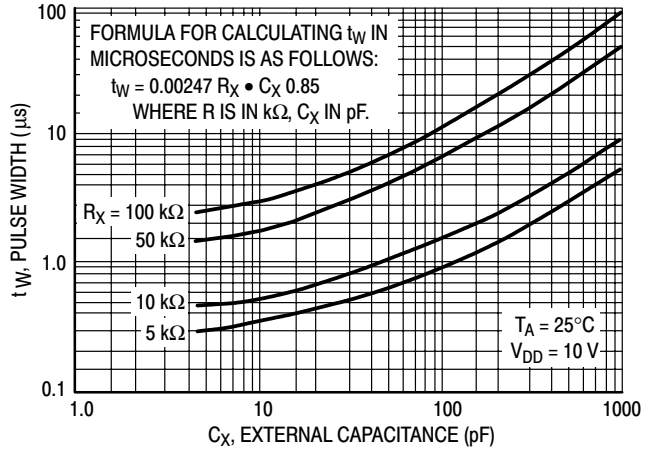


Figure 4. Typical C_X versus Pulse Width @ V_{DD} = 10 V

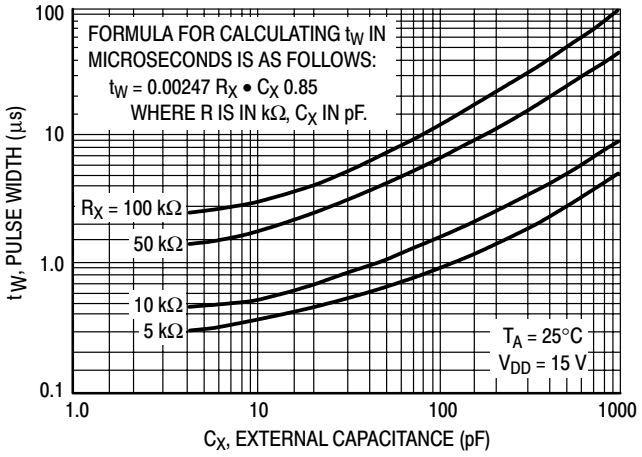


Figure 5. Typical C_X versus Pulse Width @ V_{DD} = 15 V

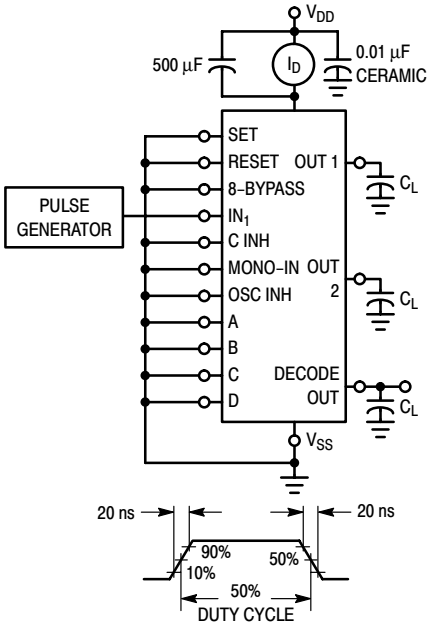


Figure 6. Power Dissipation Test Circuit and Waveform

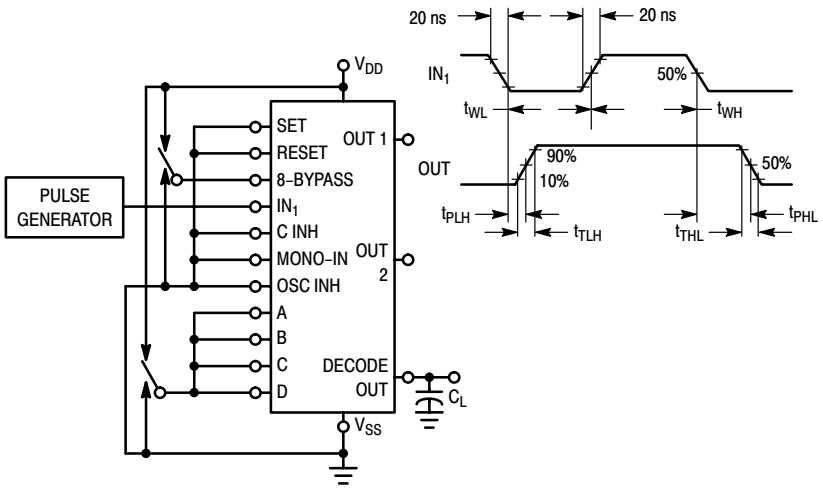


Figure 7. Switching Time Test Circuit and Waveforms

FUNCTIONAL TEST SEQUENCE

Test function (Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8–stage sections and 255 counts are loaded in each of the 8–stage sections in parallel. All flip–flops are now at a “1”. The counter is now returned to the normal 24–stages in series configuration. One more pulse is entered into In_1 which will cause the counter to ripple from an all “1” state to an all “0” state.

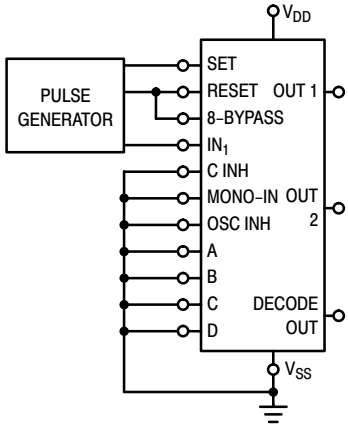
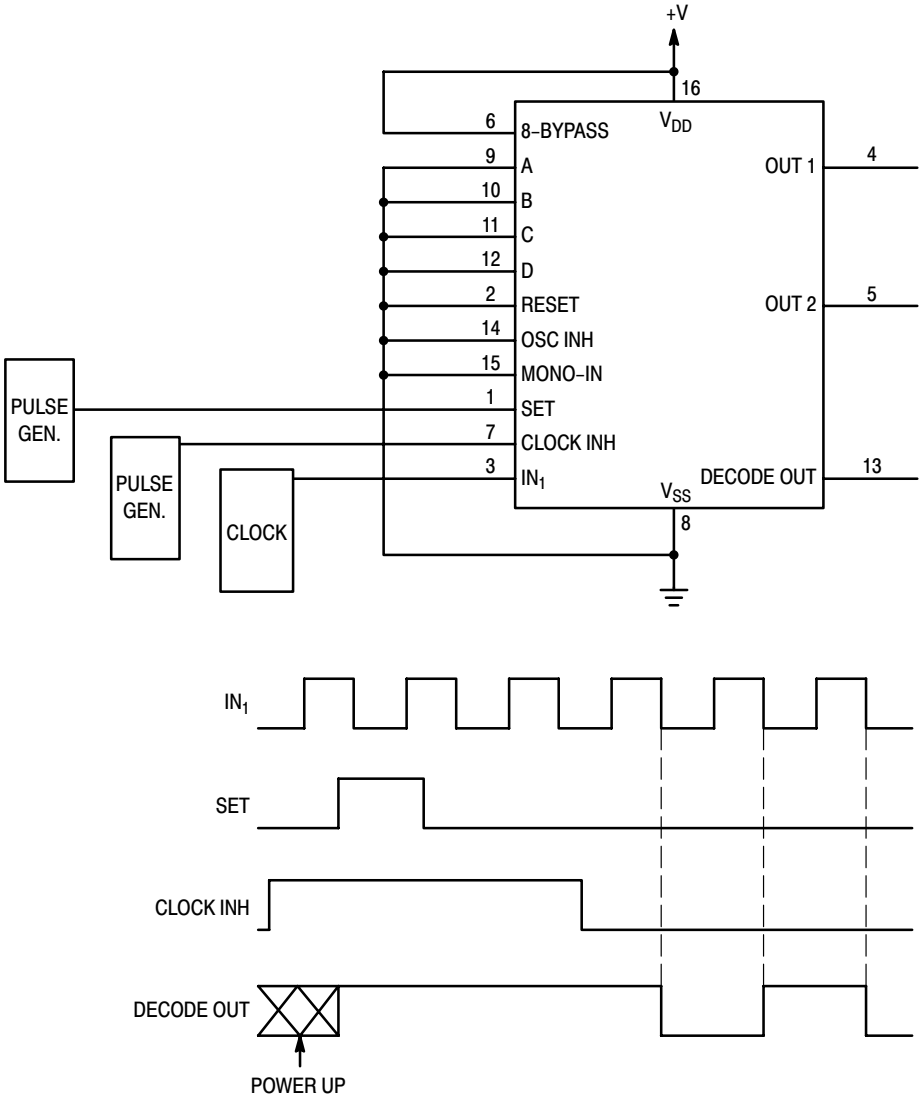


Figure 8. Functional Test Circuit

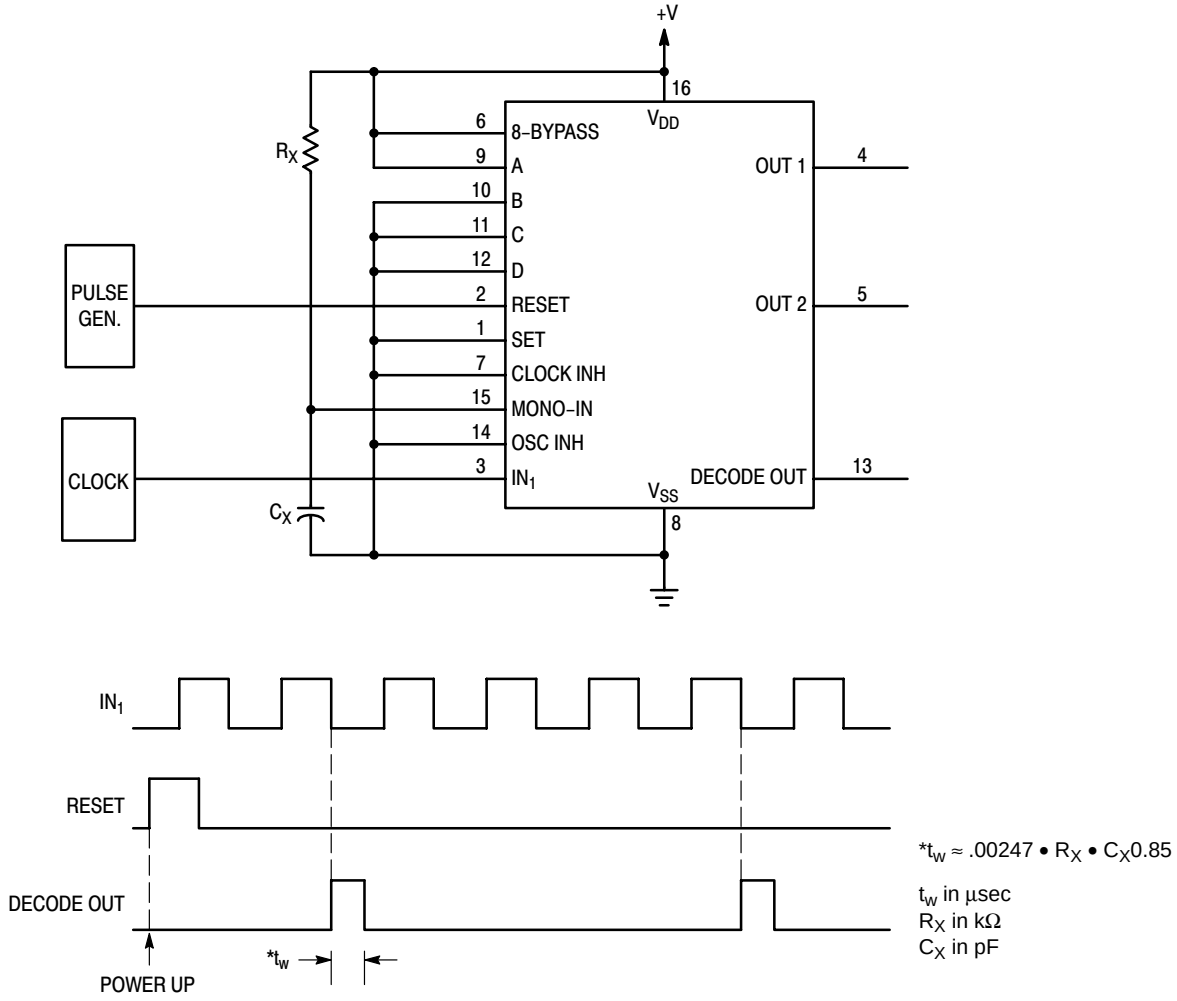
FUNCTIONAL TEST SEQUENCE

Inputs				Outputs	Comments
In_1	Set	Reset	8–Bypass	Decade Out Q1 thru Q24	All 24 stages are in Reset mode.
1	0	1	1	0	
1	1	1	1	0	Counter is in three 8 stage sections in parallel mode.
0	1	1	1	0	First “1” to “0” transition of clock.
1 0 — — —	1	1	1		255 “1” to “0” transitions are clocked in the counter.
0	1	1	1	1	The 255 “1” to “0” transition.
0	0	0	0	1	Counter converted back to 24 stages in series mode. Set and Reset must be connected together and simultaneously go from “1” to “0”.
1	0	0	0	1	In_1 Switches to a “1”.
0	0	0	0	0	Counter Ripples from an all “1” state to an all “0” state.



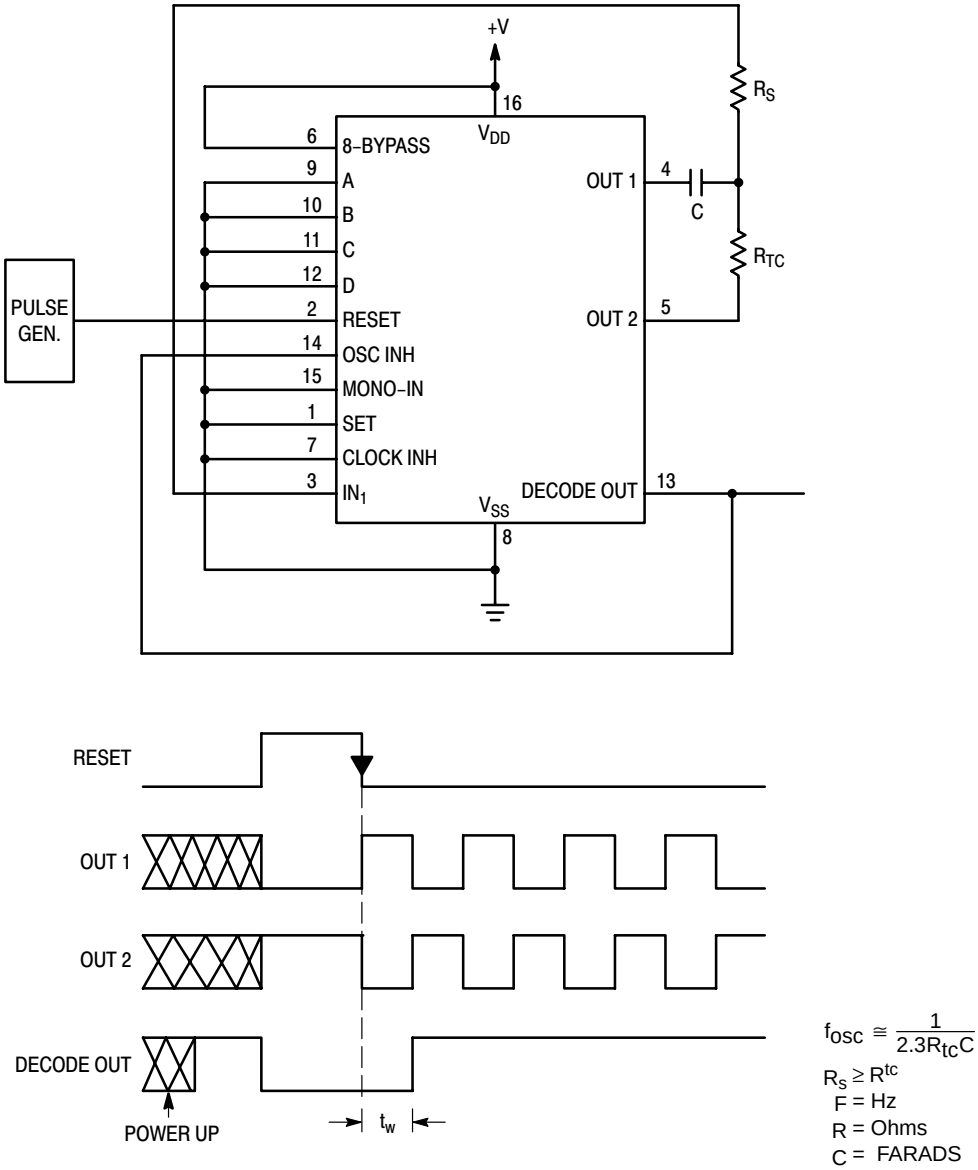
NOTE: When power is first applied to the device, DECODE OUT can be either at a high or low state. On the rising edge of a SET pulse the output goes high if initially at a low state. The output remains high if initially at a high state. Because CLOCK INH is held high, the clock source on the input pin has no effect on the output. Once CLOCK INH is taken low, the output goes low on the first negative clock transition. The output returns high depending on the 8–BY-PASS, A, B, C, and D inputs, and the clock input period. A 2^n frequency division (where n = the number of stages selected from the truth table) is obtainable at DECODE OUT. A 2^0–divided output of IN_1 can be obtained at OUT_1 and OUT_2.

Figure 9. Time Interval Configuration Using an External Clock, Set, and Clock Inhibit Functions (Divide–by–2 Configured)



NOTE: When Power is first applied to the device with the RESET input going high, DECODE OUT initializes low. Bringing the RESET input low enables the chip's internal counters. After RESET goes low, the $2^n/2$ negative transition of the clock input causes DECODE OUT to go high. Since the MONO–IN input is being used, the output becomes monostable. The pulse width of the output is dependent on the external timing components. The second and all subsequent pulses occur at 2^n x (the clock period) intervals where n = the number of stages selected from the truth table.

Figure 10. Time Interval Configuration Using an External Clock, Reset, and Output Monostable to Achieve a Pulse Output (Divide–by–4 Configured)

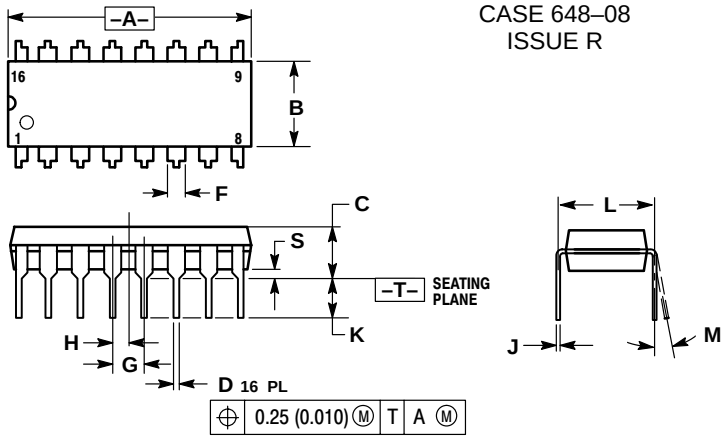


NOTE: This circuit is designed to use the on–chip oscillation function. The oscillator frequency is determined by the external R and C components. When power is first applied to the device, DECODE OUT initializes to a high state. Because this output is tied directly to the OSC INH input, the oscillator is disabled. This puts the device in a low–current standby condition. The rising edge of the RESET pulse will cause the output to go low. This in turn causes OSC INH to go low. However, while RESET is high, the oscillator is still disabled (i.e.: standby condition). After RESET goes low, the output remains low for $2^n/2$ of the oscillator's period. After the part times out, the output again goes high.

Figure 11. Time Interval Configuration Using On–Chip RC Oscillator and Reset Input to Initiate Time Interval (Divide–by–2 Configured)

PACKAGE DIMENSIONS

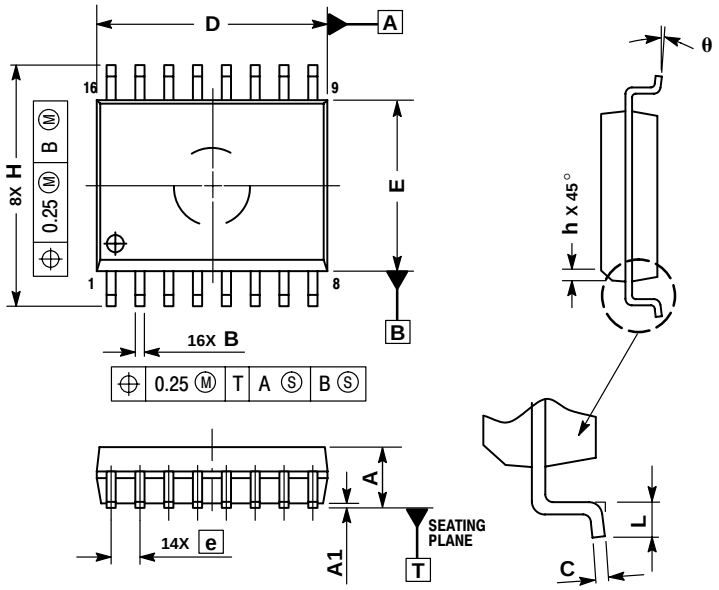
PDIP–16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SOIC–16
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751G–03
ISSUE B

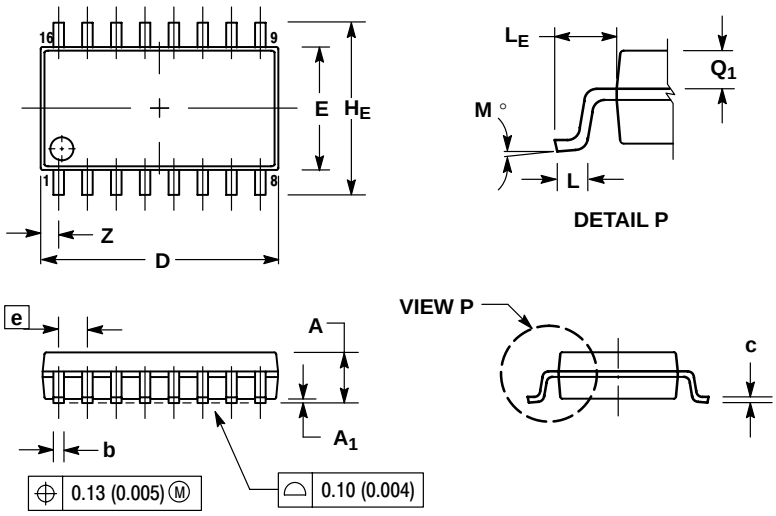


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

PACKAGE DIMENSIONS

SOEIAJ–16
F SUFFIX
PLASTIC EIAJ SOIC PACKAGE
CASE 966–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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