40V, Low Quiescent Current, 150mA Linear Regulator for Automotive Applications

ISL78301

The ISL78301 is a high voltage, low quiescent current linear regulator ideally suited for “always-on” and “keep alive” automotive applications. The ISL78301 operates from an input voltage of +6V to +40V under normal operating conditions and operates down to +3V under a cold crank. It consumes only 18µA of quiescent current at no load on the adjustable version.

The ISL78301 is available in a fixed 3.3V, 5V and adjustable output voltage (2.5V to 12V) options. It features an EN pin that can be used to put the device into a low-quiescent current shutdown mode where it draws only 2µA of supply current. The device features over-temperature shutdown and current limit protection.

The ISL78301 is both AEC-Q100 qualified and fully TS16949 compliant. It is rated over the -40°C to +125°C automotive temperature range and is available in a 14 Ld HTSSOP with an exposed pad package.

Applications

- Automotive
- Industrial
- Telecommunications

Features

- Optimized for “Always-on” Automotive Applications
- 18µA Typical Quiescent Current
- Guaranteed 150mA Output Current
- Operates Through Cold Crank Down to 3V
- 40V Tolerant Logic Level (TTL/CMOS) Enable Input
- 2µA of Typical Shutdown Current
- Low Dropout Voltage of 295mV at 150mA
- Fixed +3.3V, +5.0V and Adjustable Output Voltage Options
- Stable Operation with 10µF Output Capacitor
- Thermal Shutdown and Current Limit Protection
- -40°C to +125°C Operating Temperature Range
- Thermally Enhanced 14 Ld Exposed Pad HTSSOP Package
- AEC-Q100 Qualified
- 5kV ESD HBM Rated
- Pb-Free (RoHS Compliant)

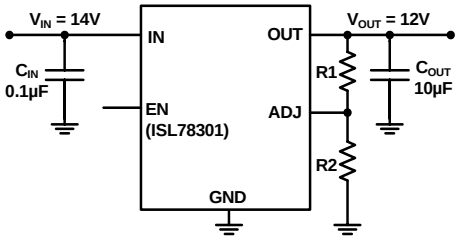


FIGURE 1. TYPICAL APPLICATION - ADJ VERSION

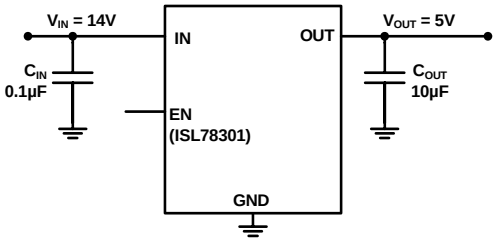


FIGURE 2. TYPICAL APPLICATION - FIXED VERSION

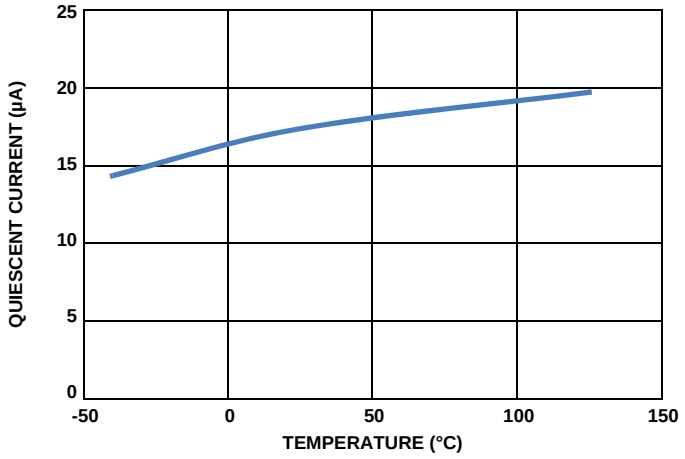
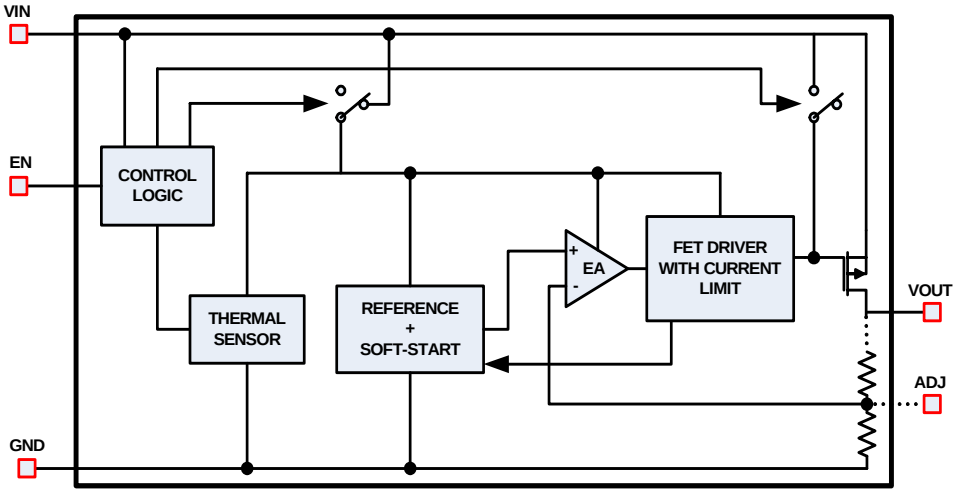


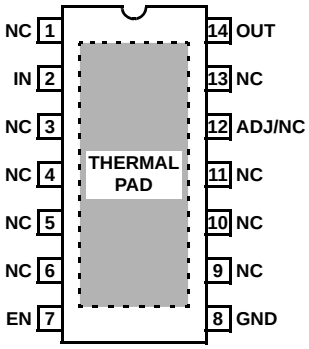
FIGURE 3. QUIESCENT CURRENT vs LOAD CURRENT (ADJ VERSION AT UNITY GAIN) V_{IN} = 14V

Block Diagram



Pin Configuration

ISL78301
(14 LD HTSSOP)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1, 3, 4, 5, 6, 9, 10, 11, 13	NC	Pins have internal termination and can be left unconnected. Connection to ground is optional.
2	IN	Input voltage pin. A minimum 0.1µF ceramic capacitor is required for proper operation.
7	EN	Enable pin. High on this pin enables the device.
8	GND	Ground pin.
12	ADJ/NC	In the adjustable output voltage option, this pin is connected to the external feedback resistor divider which sets the LDO output voltage. In the 3.3V and 5V options, this pin is not used and can be connected to ground.
14	OUT	Regulated output voltage. A 10µF ceramic capacitor is required for stability.
	EPAD	It is recommended to solder the EPAD to the ground plane.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	ENABLE PIN	OUTPUT VOLTAGE (V)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL78301FVEAZ	78301 FVEAZ	-40 to +125	Yes	3.3	14 Ld HTSSOP	M14.173B
ISL78301FVEBZ	78301 FVEBZ	-40 to +125	Yes	5.0	14 Ld HTSSOP	M14.173B
ISL78301FVECZ	78301 FVECZ	-40 to +125	Yes	ADJ	14 Ld HTSSOP	M14.173B

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL78301. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

Supply Voltage, VCC . . . . . +45V
IN pin to GND Voltage. . . . . GND - 0.3V to VCC
OUT pin to GND Voltage . . . . . GND - 0.3V to 16V
ADJ pin to GND Voltage . . . . . GND - 0.3V to 3V
EN pin to GND Voltage . . . . . GND - 0.3V to VCC
Output Short-circuit Duration . . . . . Indefinite
ESD Rating
Human Body Model (Tested per JESD22-A114E). 5kV
Machine Model (Tested per JESD-A115-A) 200V
Charge Device Model (Tested per JESD22-C101C). 2.2kV
Latch Up (Tested per JESD78B; Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
14 Ld HTSSOP Package (Notes 4, 5).	37	5

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +175°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature Range . . . . . -40°C to +125°C
IN pin to GND Voltage. . . . . +3V to +40V
OUT pin to GND Voltage . . . . . +2.5V to +12V
EN pin to GND Voltage . . . . . 0V to +40V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, unless otherwise noted. V_{IN} = 14V, I_{OUT} = 1mA, C_{IN} = 0.1µF, C_{OUT} = 10µF, $T_A = T_J$ = -40°C to +125°C, unless otherwise noted. Typical specifications are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN (Note 8)	TYP	MAX (Note 8)	UNIT
Input Voltage Range	V_{IN}			**6**		**40**	V
		Cold Crank condition		**3**		**40**	V
Guaranteed Output Current	I_{OUT}	$V_{IN} = V_{OUT} + VDO$		**150**			mA
Output Voltage	V_{OUT}	EN = High V_{IN} = 14V I_{OUT} = 0.1mA to 150mA	3.3V Version	**3.267**	3.3	**3.333**	V
			5V Version	**4.950**	5	**5.050**	V
			ADJ pin voltage	**1.211**	1.223	**1.235**	V
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	3V ≤ V_{IN} ≤ 40V I_{OUT} = 1mA			0.04	**0.15**	%
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	$V_{IN} = V_{OUT} + V_{DO}$ I_{OUT} = 100µA to 150mA			0.3	**0.6**	%
Dropout Voltage (Note 6)	ΔV_{DO}	I_{OUT} = 1mA, V_{OUT} = 3.3V			7	**33**	mV
		I_{OUT} = 150mA, V_{OUT} = 3.3V			380	**525**	mV
		I_{OUT} = 1mA, V_{OUT} = 5V			7	**33**	mV
		I_{OUT} = 150mA, V_{OUT} = 5V			295	**460**	mV
Shutdown Current	I_{SHDN}	EN = LOW			2	**3.64**	µA
Quiescent Current	I_Q	EN = High V_{IN} = 14V	I_{OUT} = 0mA, ADJ Version, $V_{OUT} = V_{ADJ}$		18	**24**	µA
			I_{OUT} = 1mA, ADJ Version, $V_{OUT} = V_{ADJ}$		22	**42**	µA
			I_{OUT} = 10mA, ADJ Version, $V_{OUT} = V_{ADJ}$		34	**60**	µA
			I_{OUT} =150mA, ADJ Version, $V_{OUT} = V_{ADJ}$		90	**125**	µA
			I_{OUT} = 0, 3.3V and 5.0V Versions		22	**28**	µA
			I_{OUT} = 1mA, 3.3V and 5.0V Versions		27	**45**	µA
			I_{OUT} = 10mA, 3.3V and 5.0V Versions		39	**65**	µA
			I_{OUT} = 150mA, 3.3V and 5.0V Versions		96	**142**	µA

Electrical Specifications Recommended Operating Conditions, unless otherwise noted. V_{IN} = 14V, I_{OUT} = 1mA, C_{IN} = 0.1µF, C_{OUT} = 10µF, $T_A = T_J$ = -40°C to +125°C, unless otherwise noted. Typical specifications are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
Power Supply Rejection Ratio	PSRR	f = 100Hz; V_{IN_RIPPLE} = 500mV_{P-P}; Load = 150mA, 3.3V and 5V Versions		55		dB
		f = 100Hz; V_{IN_RIPPLE} = 500mV_{P-P}; Load = 150mA, ADJ Version, $V_{OUT} = V_{ADJ}$		66		
EN FUNCTION						
EN Threshold Voltage	V_{EN_H}	V_{OUT} = Off to On			**1.485**	V
	V_{EN_L}	V_{OUT} = On to Off	**0.975**			V
EN Pin Current	I_{EN}	V_{OUT} = 0V		0.026		µA
EN to Regulation Time (Note 7)	t_{EN}			1.65	**1.93**	ms
PROTECTION FEATURES						
Output Current Limit	I_{LIMIT}	V_{OUT} = 0V	**175**	410		mA
Thermal Shutdown	T_{SHDN}	Junction Temperature Rising		+165		°C
Thermal Shutdown Hysteresis	T_{HYST}			+20		°C

NOTES:

6. Dropout voltage is defined as (V_{IN} - V_{OUT}) when V_{OUT} is 2% below the value of V_{OUT} when $V_{IN} = V_{OUT}$ + 3V.
7. Enable to Regulation is the time the output takes to reach 95% of its final value with V_{IN} = 14V and EN is taken from V_{IL} to V_{IH} in 5ns. For the adjustable versions, the output voltage is set at 5V.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

V_{IN} = 14V, I_{OUT} = 1mA, V_{OUT} = 5V, T_J = +25°C unless otherwise specified.

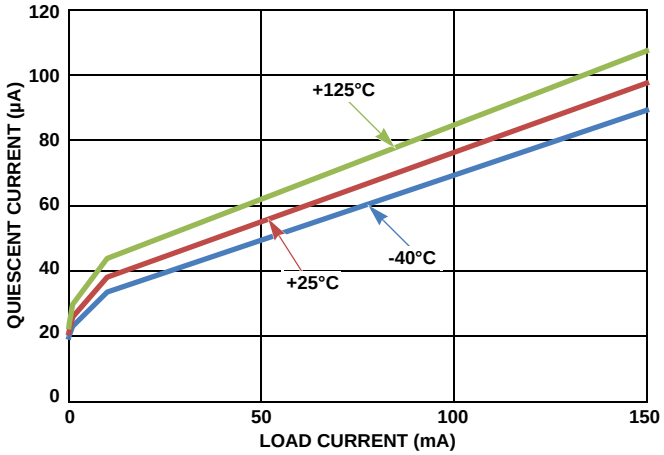


FIGURE 4. QUIESCENT CURRENT vs LOAD CURRENT

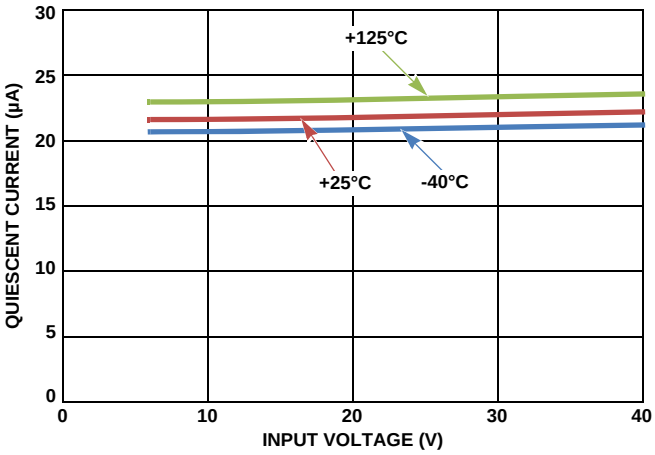


FIGURE 5. QUIESCENT CURRENT vs INPUT VOLTAGE (NO LOAD)

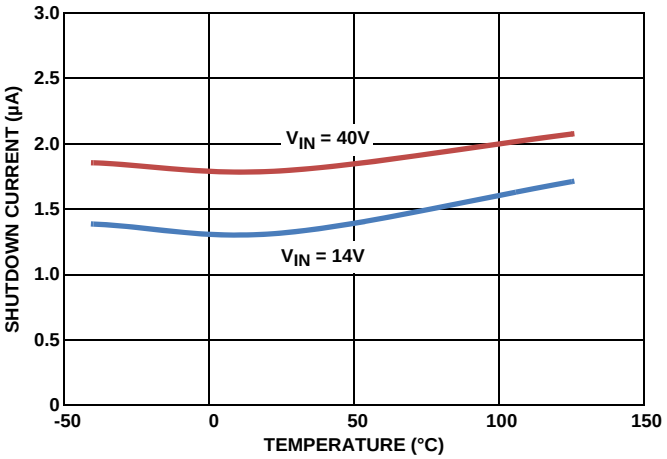


FIGURE 6. SHUTDOWN CURRENT vs TEMPERATURE (EN = 0)

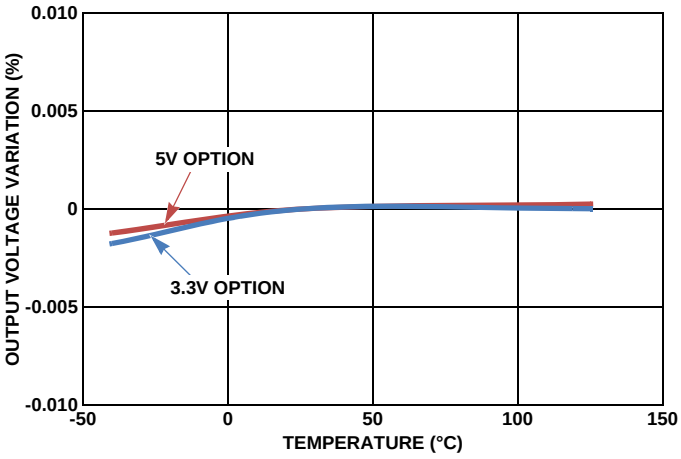


FIGURE 7. OUTPUT VOLTAGE vs TEMPERATURE (LOAD = 50mA)

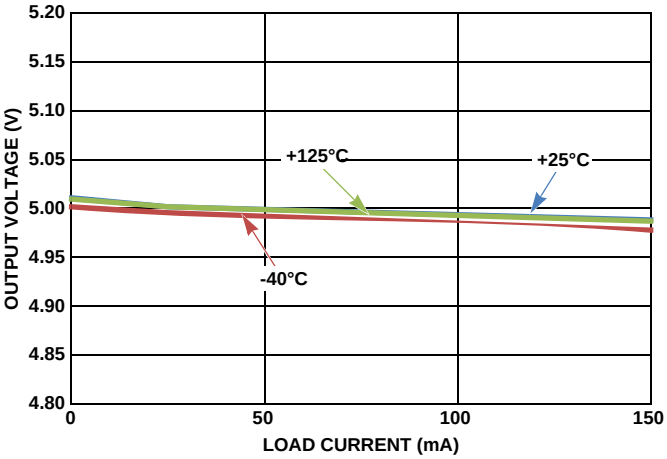


FIGURE 8. OUTPUT VOLTAGE vs LOAD CURRENT

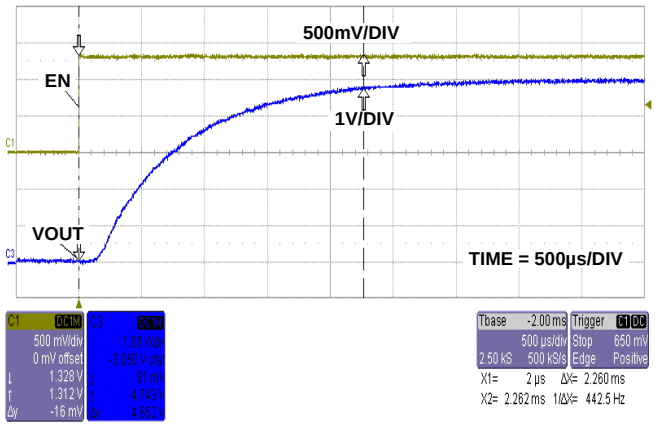


FIGURE 9. START-UP WAVEFORM

Typical Performance Curves

V_{IN} = 14V, I_{OUT} = 1mA, V_{OUT} = 5V, T_J = +25°C unless otherwise specified. **(Continued)**

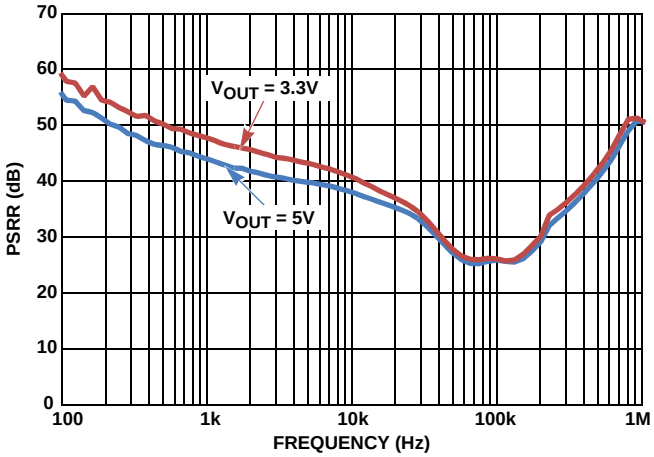


FIGURE 10. POWER SUPPLY REJECTION RATIO (LOAD = 150mA)

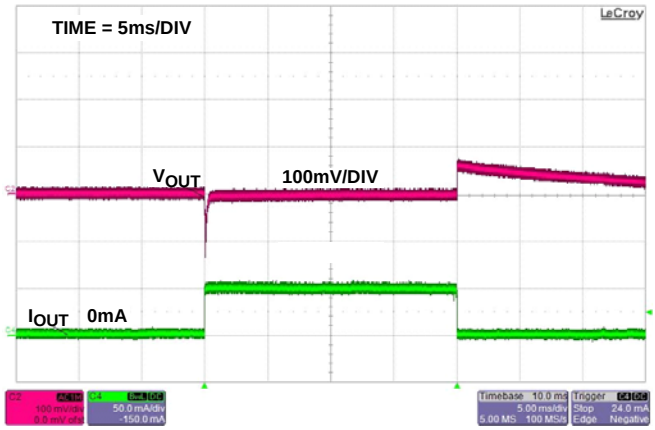


FIGURE 11. LOAD TRANSIENT RESPONSE

Functional Description

Functional Overview

The ISL78301 is a high performance, high voltage, low-dropout regulator (LDO) with 150mA sourcing capability. The part is qualified to operate over the -40°C to +125°C automotive temperature range. Featuring ultra-low quiescent current, it makes an ideal choice for “always-on” automotive applications. It works well under a “load dump condition” where the input voltage could rise up to 40V. The LDO continues to operate down to 3V under a “cold-crank” condition. The device also features current limit and thermal shutdown protection.

Enable Control

The ISL78301 has an enable pin which turns the device on when pulled high. When EN is low, the IC goes into shutdown mode and draws less than 2µA.

Current Limit Protection

The ISL78301 has internal current limiting functionality to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current largely independent of the output voltage. If the short or overload is removed from V_{OUT}, the output returns to normal voltage regulation mode.

Thermal Fault Protection

In the event that the die temperature exceeds a typical value of +165°C, the output of the LDO will shut down until the die temperature cools down to a typical +145°C. The level of power dissipated, combined with the ambient temperature and the thermal impedance of the package, determines if the junction temperature exceeds the thermal shutdown temperature. See the “Power Dissipation” section for more details.

Application Information

Input and Output Capacitors

A minimum 0.1µF ceramic capacitor is recommended at the input for proper operation. For the output, a ceramic capacitor with a capacitance of 10µF is recommended for the ISL78301 to maintain stability. The ground connection of the output capacitor should be routed directly to the GND pin of the device and also placed close to the IC.

Output Voltage Setting

For the adjustable version of the ISL78301, the output voltage is programmed using an external resistor divider as shown in Figure 12.

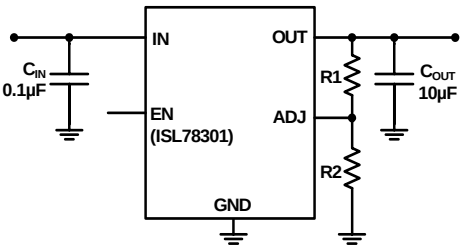


FIGURE 12. ADJUSTABLE VERSION

The output voltage is calculated using Equation 1:

$$V_{OUT} = 1.223V \times \left(\frac{R_1}{R_2} + 1\right) \quad \text{(EQ. 1)}$$

Power Dissipation

The junction temperature must not exceed the range specified in “Recommended Operating Conditions” on page 4. The power dissipation can be calculated using Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad \text{(EQ. 2)}$$

The maximum allowable junction temperature, $T_{J(MAX)}$ and the maximum expected ambient temperature, $T_{A(MAX)}$ will determine the maximum allowable junction temperature rise (ΔT_J), as shown in Equation 3:

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)} \quad \text{(EQ. 3)}$$

To calculate the maximum ambient operating temperature, use the junction-to-ambient thermal resistance (θ_{JA}) as shown in Equation 4:

$$T_{J(MAX)} = P_{D(MAX)} \times \theta_{JA} + T_A \quad \text{(EQ. 4)}$$

Board Layout Recommendations

A good PCB layout is important to achieve expected performance. Consideration should be taken when placing the components and routing the trace to minimize the ground impedance and keep the parasitic inductance low. The input and output capacitors should have a good ground connection and be placed as close to the IC as possible. The feedback trace in the adjustable version should be away from other noisy traces.

The 14 Ld HTSSOP package uses the copper area on the PCB as a heat-sink. The EPAD of this package must be soldered to the copper plane (GND plane) for effective heat dissipation. Figure 13 shows a curve for θ_{JA} of the package for different copper area sizes.

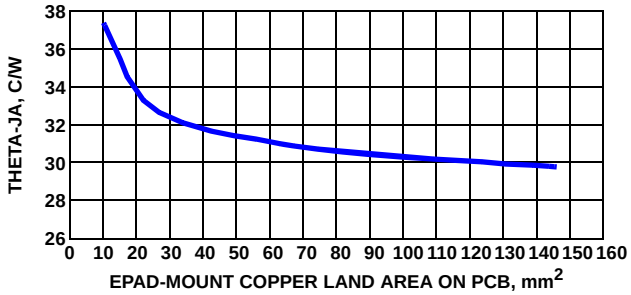


FIGURE 13. θ_{JA} vs EPAD-MOUNT COPPER LAND AREA ON PCB

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
10/21/11	FN6705.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL78301

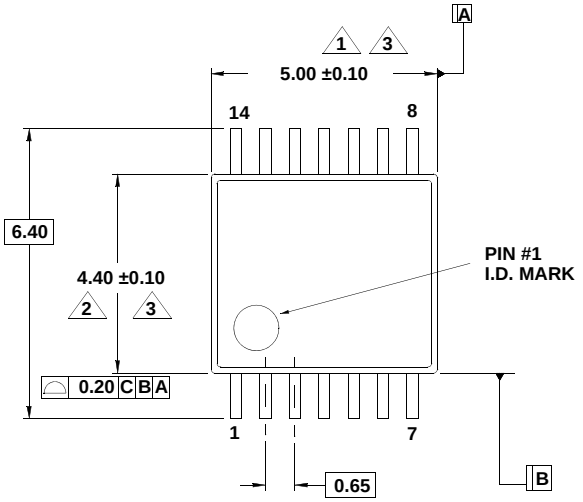
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

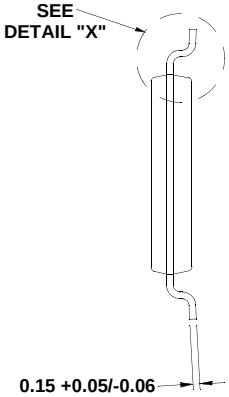
Package Outline Drawing

M14.173B

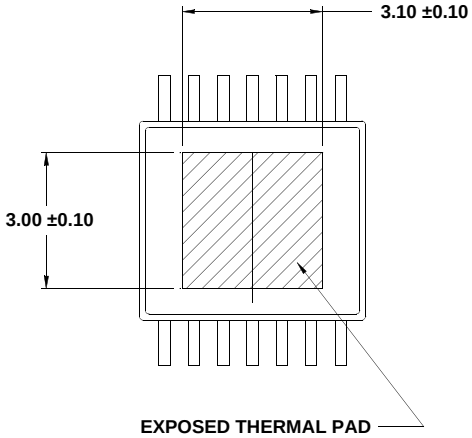
14 LEAD HEAT-SINK THIN SHRINK SMALL OUTLINE PACKAGE (HTSSOP)
Rev 1, 1/10



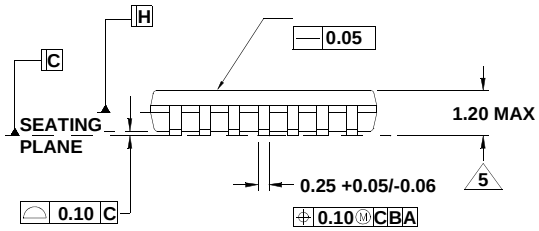
TOP VIEW



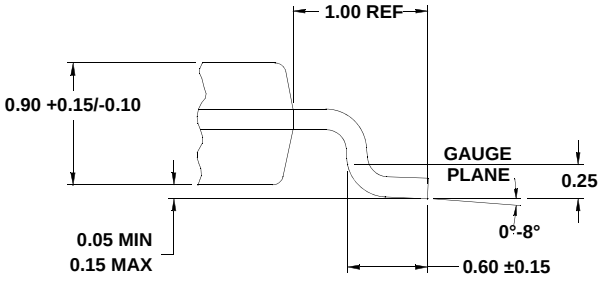
END VIEW



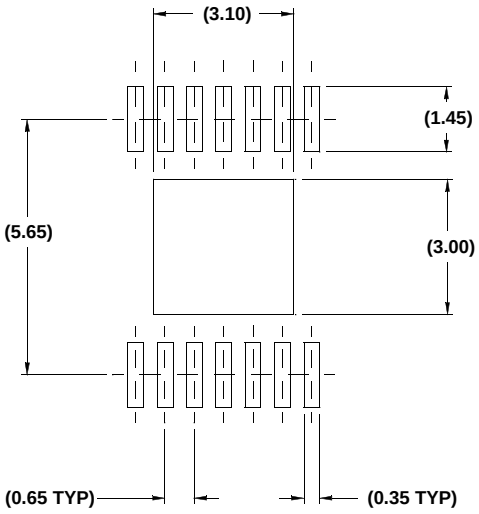
BOTTOM VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion.
   Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition.
   Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153, variation ABT-1.