

HITACHI

Hitachi Displays, Ltd.

Date: November 28, 2008

TECHNICAL DATA

TX05D125VM0AAA

CONTENTS

No.	Item	Sheet No.	Page
1	COVER	3284PS 2601- TX05D125VM0AAA	1-1/1
2	RECORD OF REVISIONS	3284PS 2602- TX05D125VM0AAA	2-1/1
3	GENERAL DATA	3284PS 2603- TX05D125VM0AAA	3-1/1
4	ABSOLUTE MAXIMUM RATINGS	3284PS 2604- TX05D125VM0AAA	4-1/1
5	ELECTRICAL CHARACTERISTICS	3284PS 2605- TX05D125VM0AAA	5-1/1
6	OPTICAL CHARACTERISTICS	3284PS 2606- TX05D125VM0AAA	6-1/2 - 6-2/2
7	BLOCK DIAGRAM	3284PS 2607- TX05D125VM0AAA	7-1/1
8	INTERFACE	3284PS 2608- TX05D125VM0AAA	8-1/9 - 8-9/9
9	DIMENSIONAL OUTLINE	3284PS 2609- TX05D125VM0AAA	9-1/1

Hitachi Displays, Ltd.	Sh. No.	3284PS 2601- TX05D125VM0AAA	Page	1-1/1
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RECORD OF REVISIONS

Date	Sheet No.	Summary

3. GENERAL DATA

(1) Product Name	TX05D125VM0AAA
(2) Module Dimensions	46.0 (W) mm x 63.05 (H) mm x 1.9 (t) mm
(3) Active Area Dimensions	40.8 (W) mm x 30.6 (H) mm
(4) Pixel Pitch	0.1275 (W) mm x 0.1275 (H) mm
(5) Resolution	320 x 3 (R,G,B)(W) x 240(H) dots
(6) Color Pixel Arrangement	RGB Vertical Stripe
(7) Display Mode	Transmissive Type, Normally Black Mode, In-Plane Sw itching Mode
(8) Number of Colors	65,536 Colors / 262,144 Colors
(9) View ing Direction	-
(10) Backlight	Light Emitting Diode (LED), FourLEDs are parallel connection Backlight current : 20 mA/LED (typ)
(11) Weight	6.5 g (typ)
(12) Pow er Supply Voltage	VDD= 2.8 V (typ)
(13) Interface I/O pow er supply Note (1)	IOVCC = 1.8 V to VDD($1.8\text{ V} \leq \text{IOVCC} \leq \text{VDD}$) The same voltage as "H" level of a customer's interface signal must be supplied to IOVCC.
(14) LCD Driver IC	S6D0171X01 (Source, Gate and Pow er IC)
(15) Interface	8-bit/16-bit CPU Interface (80 systems)

Note (1) IOVCC is the reference voltage for adjusting the I/O signal level of S6D0171X01.
IOVCC voltage must be determined according to a customer's system.

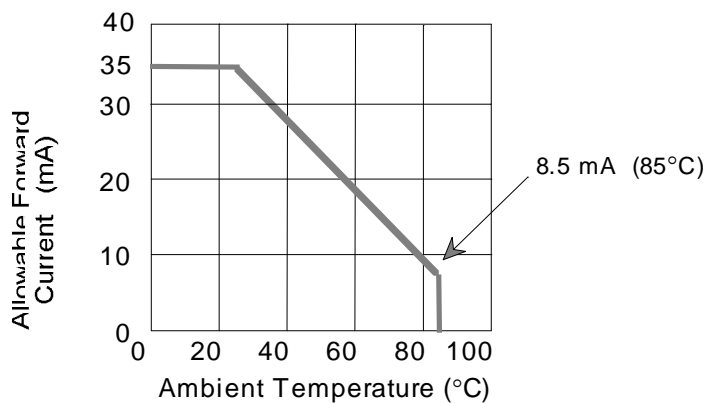
4. ABSOLUTE MAXIMUM RATINGS

4. 1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS OF LCD

V_{SS} = 0 V, T_a = 25°C

Item	Symbol	Min	Max	Unit	Note
Power Supply for Interface	IOVCC	-0.5	3.6	V	(1), (5)
Power Supply for Analog & Logic	VDD	-0.5	4.2	V	(1)
Input Voltage	V _i	-0.5	IOVCC+0.5	V	(2)
Input Current	i _i	0	100	mA	
LED Reverse Voltage	V _R	-	5	V	
LED Forward Current	I _{LED}	-	Note (3)	mA	per LED
Static Electricity	-	-	±2	kV	(4)

- Notes (1) Keep all Voltages no lower than GND.
 (2) Applies to the RESET, CS/, RS, WR/, RD/, D0 to D15 pins, IF
 (3) Ambient Temperature vs. Allowable Forward Current



- (4) 100pF-1.5 kohm, 25°C-70%RH
 Static electricity discharge is to be aimed at the center of the active area.
 (5) IOVCC ≤ VDD

4. 2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

Item	Operating		Storage		Remarks
	Min	Max	Min	Max	
Ambient Temperature	-20°C	70°C	-30°C	80°C	Note (2)
Humidity	Note (1)		Note (1)		No condensation
Corrosive Gas	Not Acceptable		Not Acceptable		

- Notes (1) T_a ≤ 40°C 85%RH max.
 T_a > 40°C Absolute humidity must be lower than the humidity of 85%RH at 40°C.
 (2) Background color slightly changes depending on ambient temperature and viewing angle.

5. ELECTRICAL CHARACTERISTICS

LCD Module

VSS = 0 V, Ta = 25 °C

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Power Supply Voltage for Logic and Analog	VDD	-	2.5	2.8	3.1	V	-
Power Supply Voltage for I/O interface	IOVCC	-	1.75	1.8	3.1	V	-
Input Voltage for Logic Circuits	Vi	"H" level	0.75xIOVCC	-	IOVCC	V	(1),(2)
		"L" level	0.0	-	0.25xIOVCC		
Output Voltage for Logic Circuits	Vo	"H" level	0.75xIOVCC	-	-	V	(1),(2)
		"L" level	-	-	0.25xIOVCC		
Input/Output Leak Current	ILi	-	-1.0		1.0	μA	(3)
Power Supply Current	IDD	All White	-	5.7	8.6	mA	(4)
		8-color partial	-	0.5	1.9	mA	(5)
Frame Frequency	fFLM	-	55	65	75	Hz	(6)
LED Forward Voltage	VLED	-	2.8	3.2	3.6	V	(7)
LED Forward Current	ILED	-	-	20	Note (9)	mA	(7)
LED Reverse Current	IR	-	-	-	50	μA	(7)

Notes (1) $1.8V \leq IOVCC \leq VDD$ (IOVCC = 1.8 V to 2.8V)

(2) Input : RESET, CS/, RS, WR/, RD/, IF, D15 to D0
Output : VSYNC-O, MID

(3) Excepted the current of out driving MOS.

(4) IOVCC=1.8V,VDD=2.8 V, fFLM = 65 Hz, Line inversion mode.

(5) IOVCC=1.8V,VDD=2.8 V, fFLM = 65 Hz, 8-color mode, Frame inversion mode.
Refer to Fig.1 Partial Pattern.

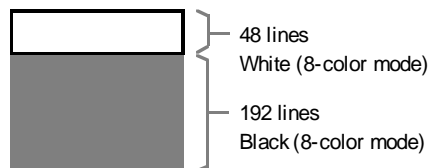


Fig.1 Partial Pattern

(6) Operation Mode: Refer to Item 8.5.1, State (b).

(7) Shows the value per LED.

(8) The operating current of LED should be determined within the maximum rating of the temperature environmental condition.

6. OPTICAL CHARACTERISTICS

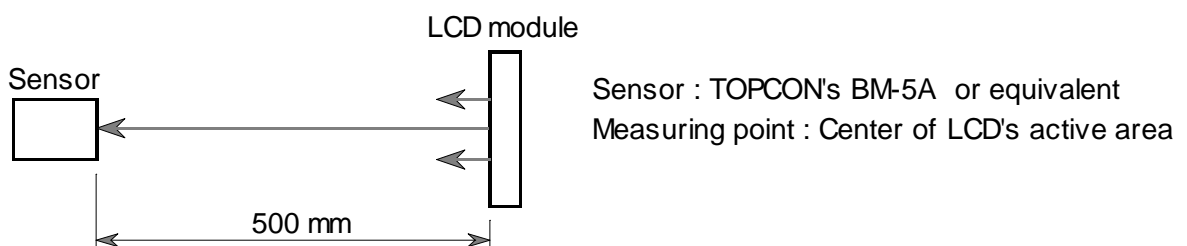
LCD (BACKLIGHT ON)

Item	Symbol	Condition	Min	Typ	Max	Unit	Note	
Brightness	B	$\phi=0^\circ, \theta=0^\circ$	-	250	-	cd/m ²	(1), (2)	
Brightness Uniformity	-	$\phi=0^\circ, \theta=0^\circ$	-	80	-	%	(2), (3), (5)	
Viewing Angle	$\phi_1+\phi_2$	$\theta=0^\circ, K\geq 10$	-	170	-	deg	(4), (6), (7)	
		$\theta=90^\circ, K\geq 10$	-	170	-			
Contrast Ratio	K	$\phi=0^\circ, \theta=0^\circ$	-	400	-	-	(6)	
Response Time	tr+tf	$\phi=0^\circ, \theta=0^\circ$	-	40	-	ms	(8)	
Color Tone (Primary Color)	Red	x	$\phi=0^\circ, \theta=0^\circ$	-	-	-	-	-
		y		-	-	-		
	Green	x		-	-	-		
		y		-	-	-		
	Blue	x		-	-	-		
		y		-	-	-		
	White	x		-	(0.29)	-		
		y		-	(0.31)	-		
NTSC Ratio	-	-	-	60	-	%	-	

Measurement Conditions

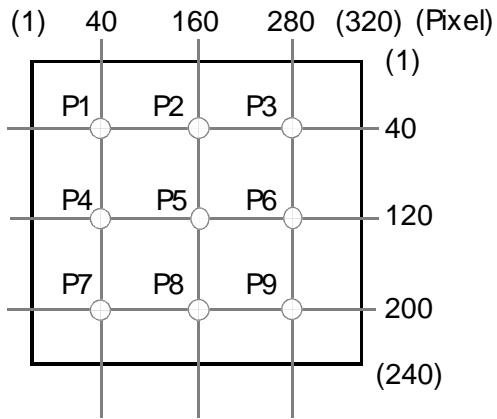
Measurement environment : Dark room
 Ambient temperature : Ta = 25°C
 Sequence : Refer to Item 8.5.2.
 Power supply voltage : VDD = 2.8V, IOVCC = 1.8 V
 Backlight current : ILED = 20 mA

Note (1) Definition of Brightness "B"

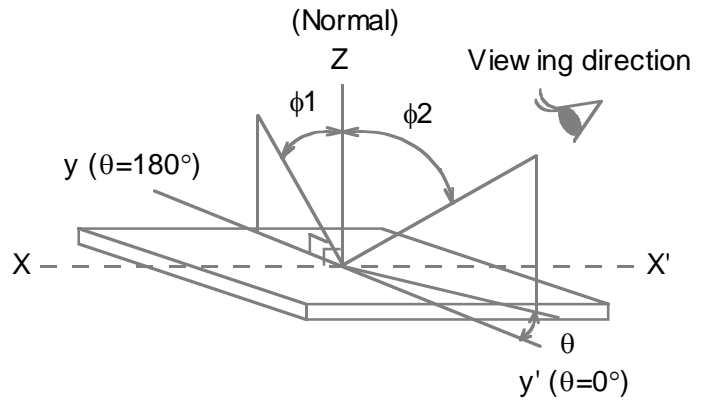


(2) Display image for measurement: All white

Notes (3) Measurement point



(4) Definitions of θ and ϕ



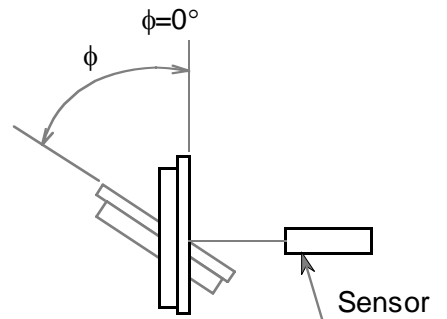
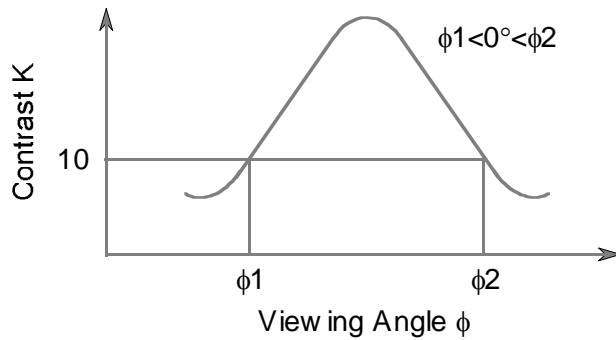
(5) Definition of Brightness Uniformity

$$\text{Brightness Uniformity} = \frac{\text{Brightness (min)}}{\text{Brightness (max)}} \times 100 (\%)$$

(6) Definition of Contrast "K"

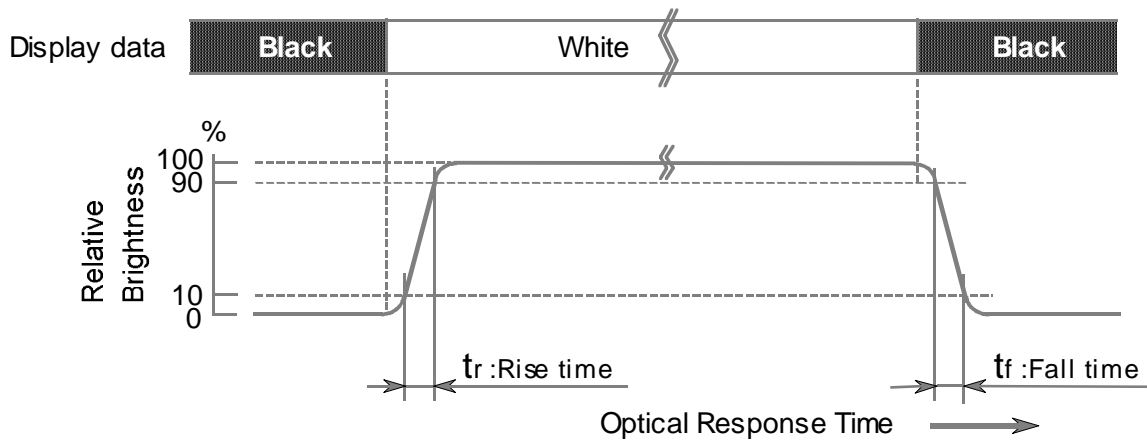
$$K = \frac{\text{Brightness when displaying White raster}}{\text{Brightness when displaying Black raster}}$$

(7) Definition of View ing Angle ϕ_1 and ϕ_2

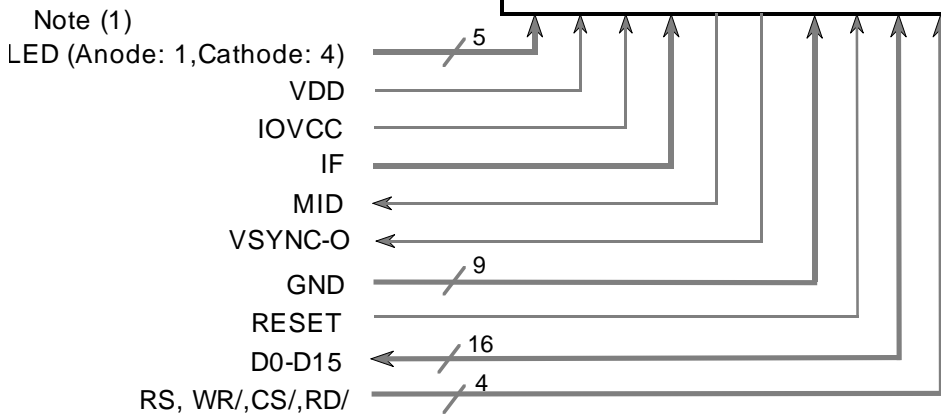
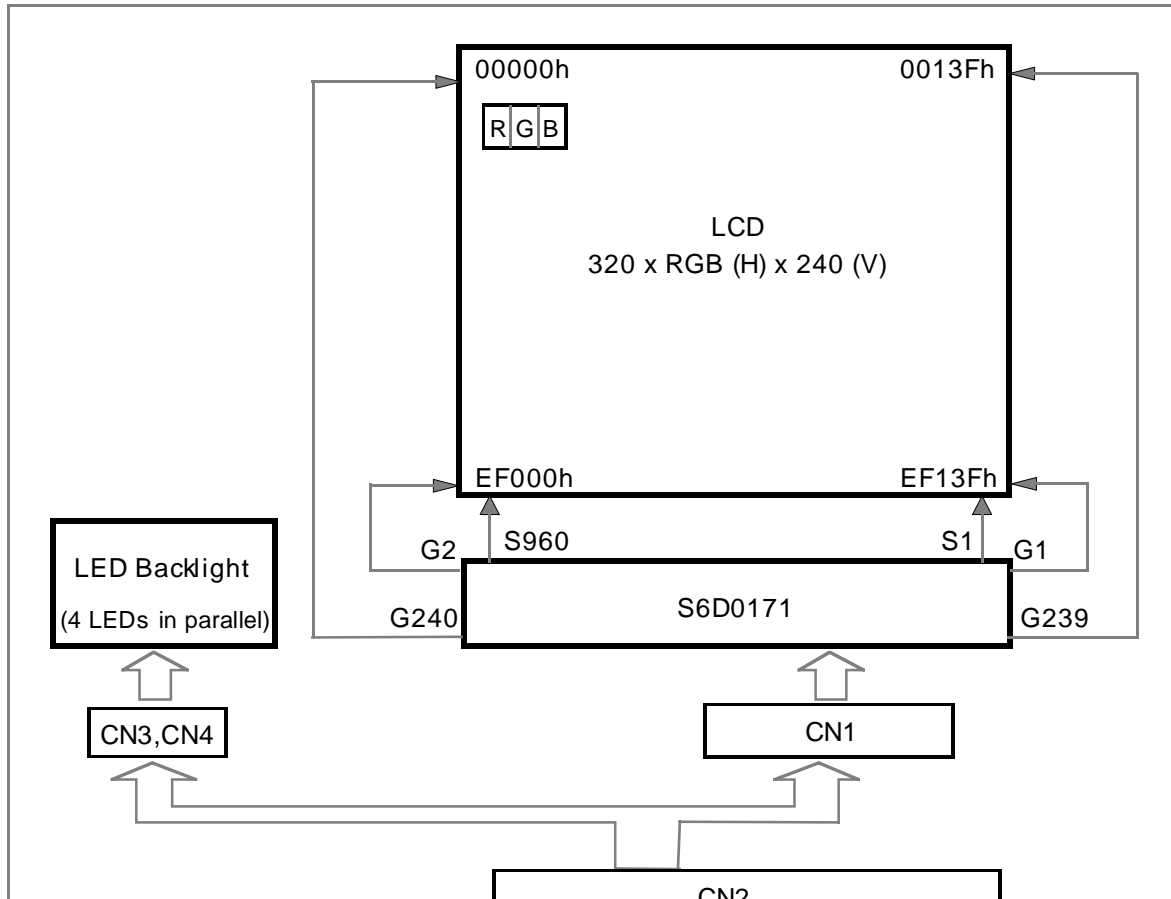


Sensor : TOPCON's BM-5A or equivalent

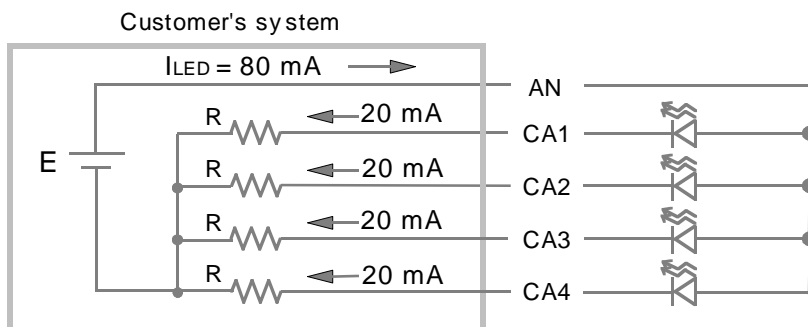
(8) Definition of Optical Response Time



7. BLOCK DIAGRAM



Note (1) Please connect the resistor (R = 200 ohm) for current control between LED (cathode) and GND in the customer's system.



8. INTERFACE

8.1 INTERNAL PIN CONNECTION

Pin No.	Signal	I/O	Function	Driver's Signal Name
1	GND	-	Ground	GND
2	LED C1	-	Ground for LED	-
3	LED C4	-	Ground for LED	-
4	LED A	-	Power Supply for LED	-
5	GND	-	Ground	GND
6	RESET	I	Reset	RESX
7	GND	-	Ground	GND
8	D15	I/O	Data Bus (Instruction & Display Data)	D15
9	D13	I/O	Data Bus (Instruction & Display Data)	D13
10	D11	I/O	Data Bus (Instruction & Display Data)	D11
11	D9	I/O	Data Bus (Instruction & Display Data)	D9
12	D7	I/O	Data Bus (Instruction & Display Data)	D7
13	D5	I/O	Data Bus (Instruction & Display Data)	D5
14	D3	I/O	Data Bus (Instruction & Display Data)	D3
15	D1	I/O	Data Bus (Instruction & Display Data)	D1
16	RD/	I	Read Strobe	RDX
17	RS	I	Register Select	DCX
18	VSYNC-O	O	Frame Head Pulse Signal	TE
19	IOVCC	-	Power Supply for Interface	VDDI
20	GND	-	Ground	GND
21	GND	-	Ground	GND
22	VDD	-	Power Supply for Logic and Analog	VDD
23	MID	O	Maker ID (Low ; GND level)	-
24	CS/	I	Chip Select	CSX
25	WR/	I	Write Strobe	WRX
26	D0	I/O	Data Bus (Instruction & Display Data)	D0
27	D2	I/O	Data Bus (Instruction & Display Data)	D2
28	D4	I/O	Data Bus (Instruction & Display Data)	D4
29	D6	I/O	Data Bus (Instruction & Display Data)	D6
30	D8	I/O	Data Bus (Instruction & Display Data)	D8
31	D10	I/O	Data Bus (Instruction & Display Data)	D10
32	D12	I/O	Data Bus (Instruction & Display Data)	D12
33	D14	I/O	Data Bus (Instruction & Display Data)	D14
34	GND	-	Ground	GND
35	GND	-	Ground	GND
36	IF	I	Interface mode Select	BUSSEL1
37	GND	-	Ground	GND
38	LED C3	-	Ground for LED	-
39	LED C2	-	Ground for LED	-
40	GND	-	Ground	GND

Suitable Connector: AXK8L40125(MATSUSHITA)

8.2 CPU INTERFACE MODE SETTING

8.2.1 SELECT CPU INTERFACE MODE

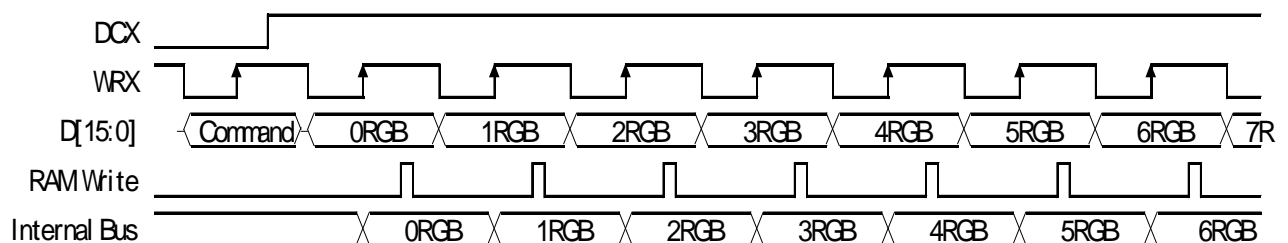
Mode Select IF	System Interface	DB Pin	RAM Write Data	Colors	Note
1	16-bit Interface	D15-D0	Single transfer (16 bits)	65k	
0	8-bit Interface	D7-D0	2 transfers (1st: 8 bits, 2nd: 8 bits)	65k	(1)
			3 transfers (1st: 6 bits, 2nd: 6 bits, 3rd: 6 bits)	262k	(1)

Note (1) The unused DB pins must be fixed to the GND level.

8.2.2 DATA FORMAT OF CPU INTERFACE

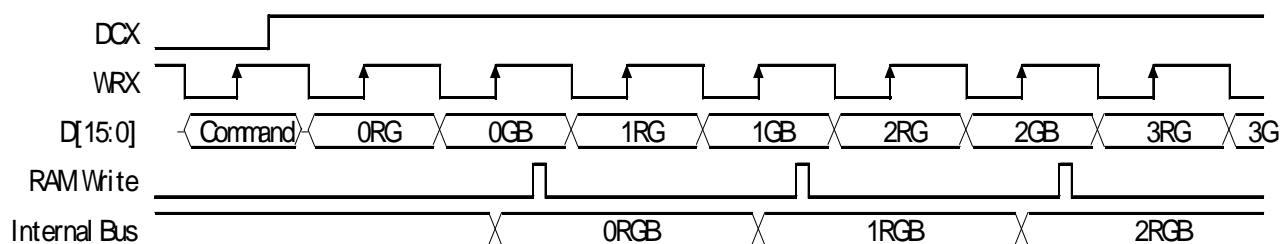
16-bit Interface mode

Cycle Count	0	1	2	...	n+1
DCX	0	1	1	...	1
D15	X	0DR4	1DR4	...	nDR4
D14	X	0DR3	1DR3	...	nDR3
D13	X	0DR2	1DR2	...	nDR2
D12	X	0DR1	1DR1	...	nDR1
D11	X	0DR0	1DR0	...	nDR0
D10	X	0DG5	1DG5	...	nDG5
D9	X	0DG4	1DG4	...	nDG4
D8	X	0DG3	1DG3	...	nDG3
D7	CD7	0DG2	1DG2	...	nDG2
D6	CD6	0DG1	1DG1	...	nDG1
D5	CD5	0DG0	1DG0	...	nDG0
D4	CD4	0DB4	1DB4	...	nDB4
D3	CD3	0DB3	1DB3	...	nDB3
D2	CD2	0DB2	1DB2	...	nDB2
D1	CD1	0DB1	1DB1	...	nDB1
D0	CD0	0DB0	1DB0	...	nDB0



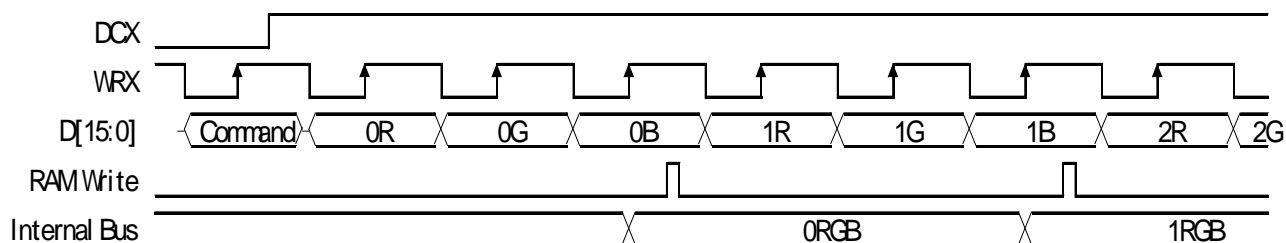
8-bit interface mode
2 transfer mode

Cycle Count	0	1	2	3	4	...	2n+1	2n+2
DCX	0	1	1	1	1	...	1	1
D7	CD7	0DR4	0DG2	1DR4	1DG2	...	nDR4	nDG2
D6	CD6	0DR3	0DG1	1DR3	1DG1	...	nDR3	nDG1
D5	CD5	0DR2	0DG0	1DR2	1DG0	...	nDR2	nDG0
D4	CD4	0DR1	0DB4	1DR1	1DB4	...	nDR1	nDB4
D3	CD3	0DR0	0DB3	1DR0	1DB3	...	nDR0	nDB3
D2	CD2	0DG5	0DB2	1DG5	1DB2	...	nDG5	nDB2
D1	CD1	0DG4	0DB1	1DG4	1DB1	...	nDG4	nDB1
D0	CD0	0DG3	0DB0	1DG3	1DB0	...	nDG3	nDB0



3 transfer mode

Cycle Count	0	1	2	3	...	2n+1	2n+2	2n+2
DCX	0	1	1	1	...	1	1	1
D7	CD7	0DR5	0DG5	0DB5	...	nDR5	nDG5	nDB5
D6	CD6	0DR4	0DG4	0DB4	...	nDR4	nDG4	nDB4
D5	CD5	0DR3	0DG3	0DB3	...	nDR3	nDG3	nDB3
D4	CD4	0DR2	0DG2	0DB2	...	nDR2	nDG2	nDB2
D3	CD3	0DR1	0DG1	0DB1	...	nDR1	nDG1	nDB1
D2	CD2	0DR0	0DG0	0DB0	...	nDR0	nDG0	nDB0
D1	CD1	X	X	X	...	X	X	X
D0	CD0	X	X	X	...	X	X	X



8.3 GRAM ADDRESS MAP

MADCTL(36h)=D8

Y	X	1			2			3			4			-----	317			318			319			320		
		S960	S959	S958	S957	S956	S955	S954	S953	S952	S951	S950	S949	-----	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
1	G240	"00000"H	"00001"H	"00002"H	"00003"H	-----	"0013C"H	"0013D"H	"0013E"H	"0013F"H																
2	G239	"01000"H	"01001"H	"01002"H	"01003"H	-----	"0113C"H	"0113D"H	"0113E"H	"0113F"H																
3	G238	"02000"H	"02001"H	"02002"H	"02003"H	-----	"0213C"H	"0213D"H	"0213E"H	"0213F"H																
4	G237	"03000"H	"03001"H	"03002"H	"03003"H	-----	"0313C"H	"0313D"H	"0313E"H	"0313F"H																
5	G236	"04000"H	"04001"H	"04002"H	"04003"H	-----	"0413C"H	"0413D"H	"0413E"H	"0413F"H																
6	G235	"05000"H	"05001"H	"05002"H	"05003"H	-----	"0513C"H	"0513D"H	"0513E"H	"0513F"H																
235	G6	"EA000"H	"EA001"H	"EA002"H	"EA003"H	-----	"EA13C"H	"EA13D"H	"EA13E"H	"EA13F"H																
236	G5	"EB000"H	"EB001"H	"EB002"H	"EB003"H	-----	"EB13C"H	"EB13D"H	"EB13E"H	"EB13F"H																
237	G4	"EC000"H	"EC001"H	"EC002"H	"EC003"H	-----	"EC13C"H	"EC13D"H	"EC13E"H	"EC13F"H																
238	G3	"ED000"H	"ED001"H	"ED002"H	"ED003"H	-----	"ED13C"H	"ED13D"H	"ED13E"H	"ED13F"H																
239	G2	"EE000"H	"EE001"H	"EE002"H	"EE003"H	-----	"EE13C"H	"EE13D"H	"EE13E"H	"EE13F"H																
240	G1	"EF000"H	"EF001"H	"EF002"H	"EF003"H	-----	"EF13C"H	"EF13D"H	"EF13E"H	"EF13F"H																

8.4 INTERFACE TIMING

8.4.1 Bus Timing Characteristics

Item	Symbol	Unit	Timing Diagram	Min	Typ	Max
CSX-WRX,RDX time	tCW8	ns	Fig. 1	8	-	-
CSX-E time	tCH8	ns	Fig. 1	8	-	-
Address hold time	tAH8	ns	Fig. 1	8	-	-
Address setup time	tAW8	ns	Fig. 1	8	-	-
Write cycle time	tCYC8	ns	Fig. 1	74	-	-
Control pulse H width time	tCCHW8	ns	Fig. 1	21	-	-
Control pulse L width time	tCCLW8	ns	Fig. 1	21	-	-
Read cycle time (ID)	tCYC28	ns	Fig. 1	147	-	-
Control pulse H width time (ID)	tCCHR8	ns	Fig. 1	79	-	-
Control pulse L width time (ID)	tCCLR8	ns	Fig. 1	37	-	-
Read cycle time (FM)	tCYC28	ns	Fig. 1	231	-	-
Control pulse H width time (FM)	tCCHR8	ns	Fig. 1	137	-	-
Control pulse L width time (FM)	tCCLR8	ns	Fig. 1	63	-	-
Data setup time	tDS8	ns	Fig. 1	8	-	-
Data hold time	tDH8	ns	Fig. 1	8	-	-
Read access time (ID)	tACC8	ns	Fig. 1	-	-	32
Read access time (FM)	tACC8	ns	Fig. 1	-	-	58
Output disable time	tOH8	ns	Fig. 1	25	-	74

8.4.2 Reset Timing Characteristics

Item	Symbol	Unit	Timing Diagram	Min	Typ	Max
Reset pulse width	tRW	μs	Fig. 2	10	-	-
Reset cancel time	tRT	ms	Fig. 2	6	-	-
Negative ignored pulse width	tNNS	μs	Fig. 2	-	-	4
Positive ignored pulse width	tPNS	ns	Fig. 2	-	-	19

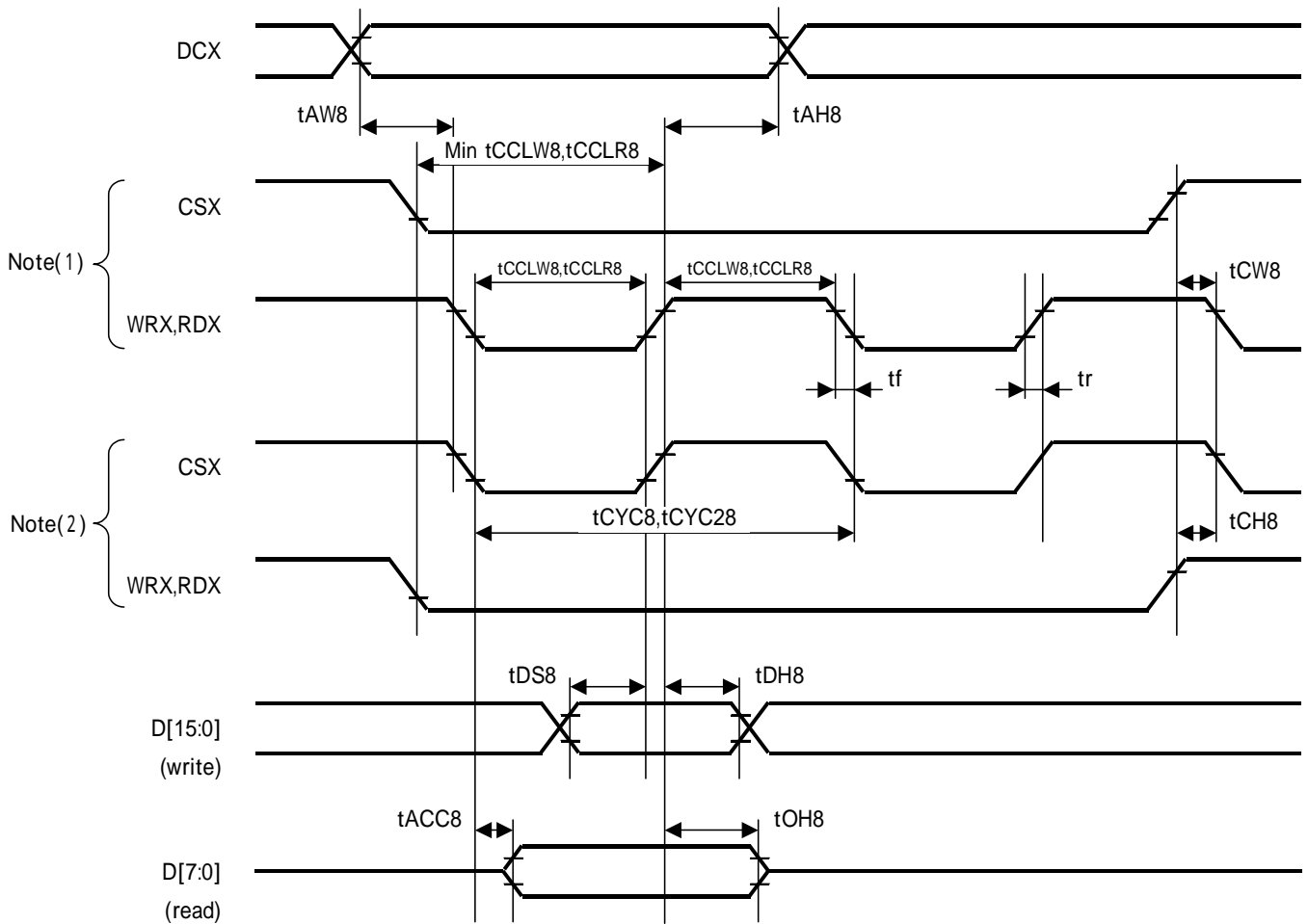


Fig.1 Bus Timing

Note(1) Access at WRX and RDX when CSX is "L".

Note (2) Access at CSX when WRX and RDX are "L".

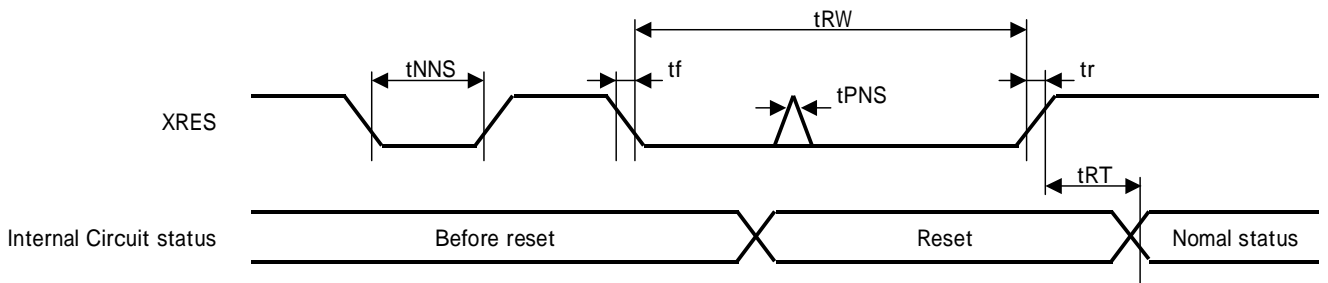
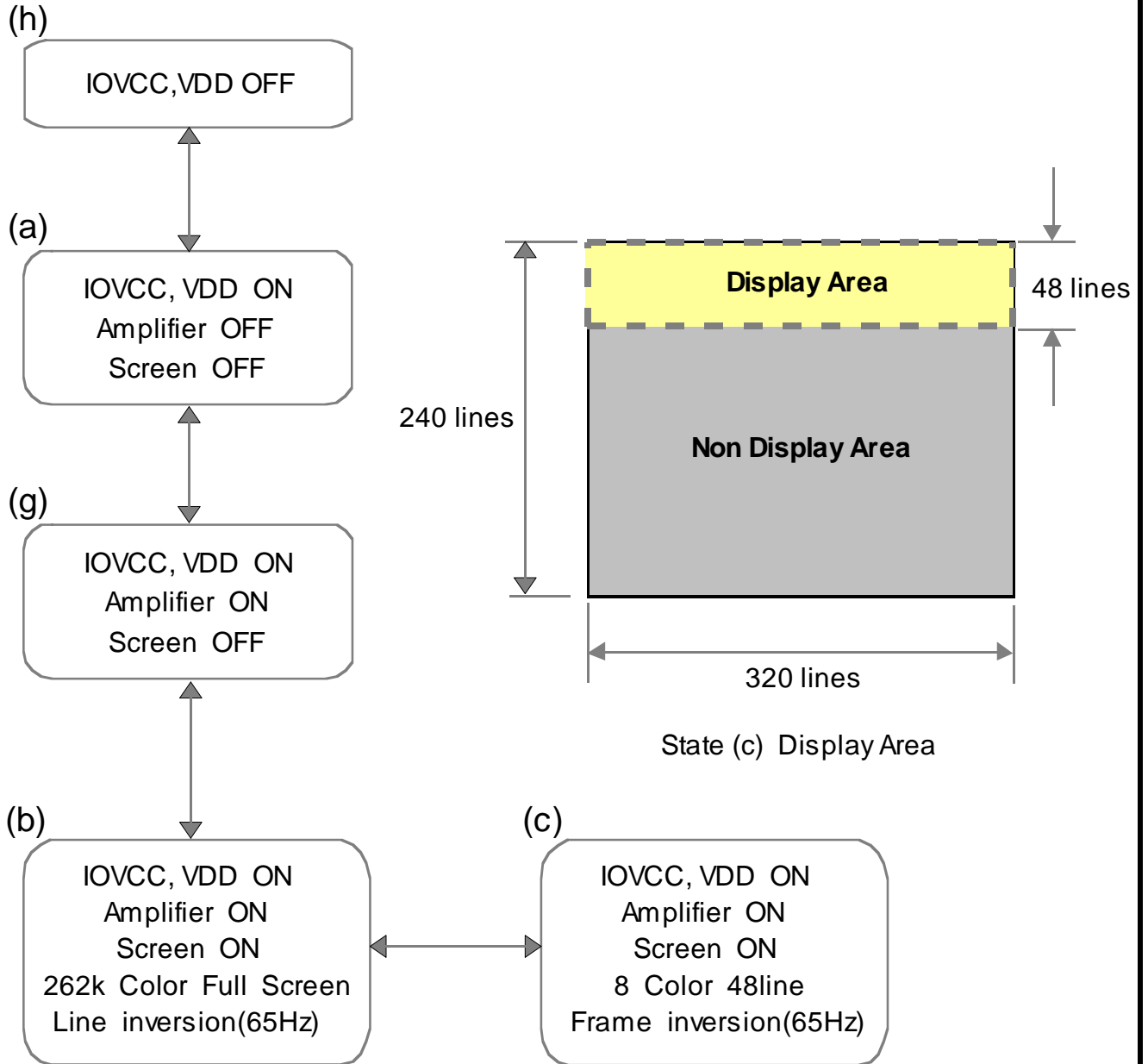


Fig.2 Reset Timing

8.5 REGISTER SETTING

8.5.1 STATE TRANSITION DIAGRAM OF OPERATION MODE



8.5.2 SEQUENCE

		State (a) -> (g)		Previous data				Previous data	
1	Command level 2	0xB0						0xE2	
2	NHW	p1	0x003C		0x002E	87		p1	0x0010
3	PHW	p2	0x003C		0x0041	88		p2	0x0000
4	IHW	p3	0x003C		0x0041	89		p3	0x0000
5	PIHW	p4	0x003C		0x0041	90		p4	0x000F
6	NVBP	p5	0x0008			91		p5	0x001B
7	PVBP	p6	0x0008			92		p6	0x0023
8	IVBP	p7	0x0008			93		p7	0x0025
9	PIVBP	p8	0x0008			94		p8	0x002D
10	NVFP	p9	0x0008			95		p9	0x0037
11	PVFP	p10	0x0008			96		p10	0x0038
12	IVFP	p11	0x0008			97		p11	0x003F
13	PIVFP	p12	0x0008			98		p12	0x0047
14	240line	p13	0x003C			99		p13	0x0039
15	Driving method	p14	0x0020		0x0000	100		0xE3	
16		p15	0x0008		0x0000	101		p1	0x0000
17	SDT	p16	0x0000			102		p2	0x0010
18	NO	p17	0x0001			103		p3	0x0000
19	262k color , NB mode	p18	0x001C			104		p4	0x000F
20	SEQ1(12ms)	p19	0x0006			105		p5	0x001B
21	SEQ2,3(12ms)	p20	0x0066			106		p6	0x0023
22	SEQ4,5(12ms)	p21	0x0066			107		p7	0x0025
23	POWER CONTROL	0xB1				108		p8	0x002D
24	NDC, NBT	p1	0x0014			109		p9	0x0037
25	NSAP, NVC	p2	0x0038			110		p10	0x0038
26		p3	0x0000			111		p11	0x003F
27	NGVDD	p4	0x0019			112		p12	0x0047
28	NVDMH	p5	0x0057			113		p13	0x0039
29	NVCOMA	p6	0x001F			114		0xE4	
30	charge recycling 1	p7	0x0000			115		p1	0x0000
31	charge recycling 2	p8	0x0080			116		p2	0x0010
32	PDC, PBT	p9	0x0014			117		p3	0x0000
33	PSAP, PVC	p10	0x0038			118		p4	0x000F
34		p11	0x0080			119		p5	0x001B
35	PGVDD	p12	0x0019			120		p6	0x0023
36	PVCMH	p13	0x0057			121		p7	0x0025
37	PVCOMA	p14	0x001F			122		p8	0x002D
38	charge recycling 1	p15	0x0000			123		p9	0x0037
39	charge recycling 2	p16	0x0080			124		p10	0x0038
40	IDC, IBT	p17	0x0014			125		p11	0x003F
41	IVC	p18	0x0008			126		p12	0x0047
42	IGVDD	p19	0x0019			127		p13	0x0039
43	IVCMH	p20	0x0057			128		0xE5	
44	IVCOMA	p21	0x001F			129		p1	0x0000
45	charge recycling 1	p22	0x0000			130		p2	0x0010
46	charge recycling 2	p23	0x0000			131		p3	0x0000
47	PIDC, PIBT	p24	0x0034			132		p4	0x000F
48	PIVC	p25	0x0008			133		p5	0x001B
49	PIGVDD	p26	0x0019			134		p6	0x0023
50	PIVCMH	p27	0x0057			135		p7	0x0025
51	PIVCOMA	p28	0x001F			136		p8	0x002D
52	charge recycling 1	p29	0x0000			137		p9	0x0037
53	charge recycling 2	p30	0x0000			138		p10	0x0038
54		0xD2				139		p11	0x003F
55		p1	0x0001			140		p12	0x0047
56		0xD3				141		p13	0x0039
57		p1	0x0000			142		0x2D	
58		p2	0x0057			143	RGBSET Setting	0x35	
59	Gamma setting	0xE0				144	Tearing effect output on	p1	0x0000
60		p1	0x0010			145		0x36	
61		p2	0x0000			146		p1	0x00D8
62		p3	0x0000			147		0x3A	
63		p4	0x000F			148	Color mode Setting	p1	0x0006
64		p5	0x001B			149	262k color	0xC2	
65		p6	0x0023			150	IF mode	p1	0x0000
66		p7	0x0025			151		0x2A	
67		p8	0x002D			152	CASET(320RGB)	p1	0x0000
68		p9	0x0037			153		p2	0x0000
69		p10	0x0038			154		p3	0x0001
70		p11	0x003F			155		p4	0x003F
71		p12	0x0047			156		0x2B	
72		p13	0x0039			157	PASET(240line)	p1	0x0000
73		0xE1				158		p2	0x0000
74		p1	0x0010			159		p3	0x0000
75		p2	0x0000			160		p4	0x00EF
76		p3	0x0000			161		0x30	
77		p4	0x000F			162	Partial setting(48line)	p1	0x0000
78		p5	0x001B			163		p2	0x0000
79		p6	0x0023			164		p3	0x0000
80		p7	0x0025			165		p4	0x002F
81		p8	0x002D			166			
82		p9	0x0037						
83		p10	0x0038						
84		p11	0x003F						
85		p12	0x0047						
86		p13	0x0039						

State (h) -> (a)		
		Previous data
1		RESET*="L"
2	POWER ON	VDDI,VDD on
3		wait 1 ms
4	RESET	RESET*="H"
5		wait 10 ms

State (g) -> (a)		
		Previous data
1	SLEEP IN	0x10

State (a) -> (h)		
		Previous data
1	POWER OFF	VDDI,VDD OFF

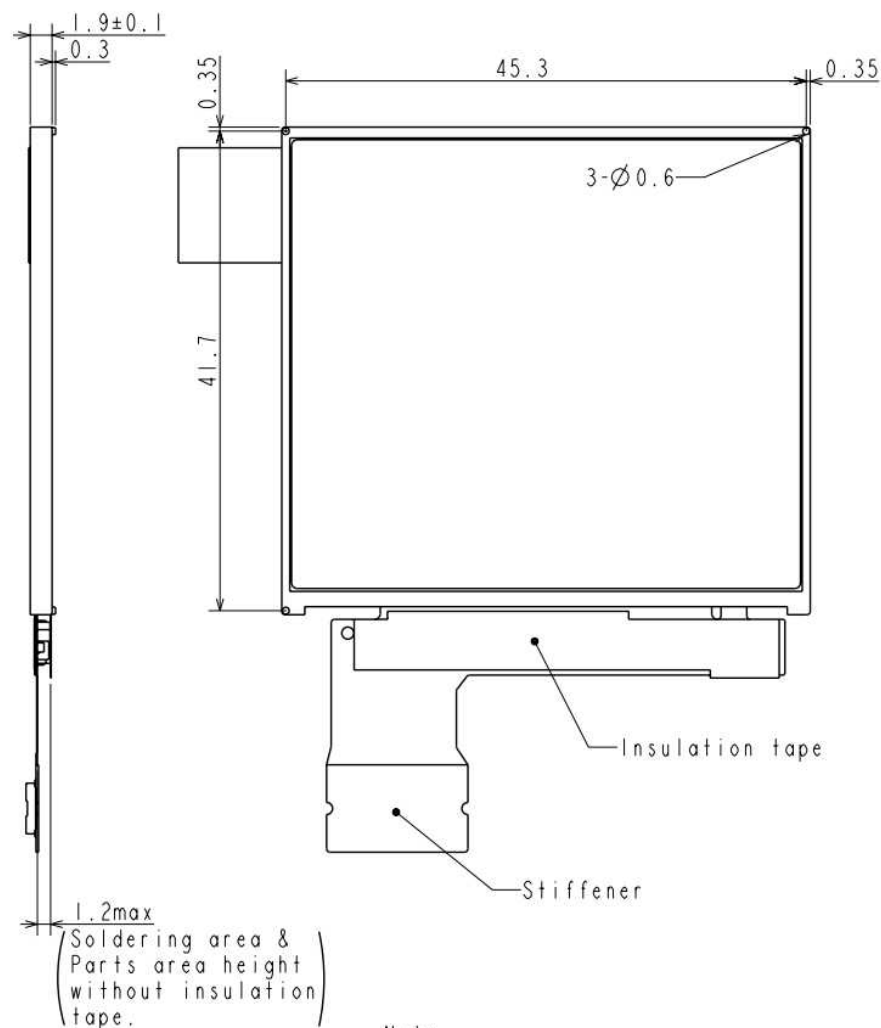
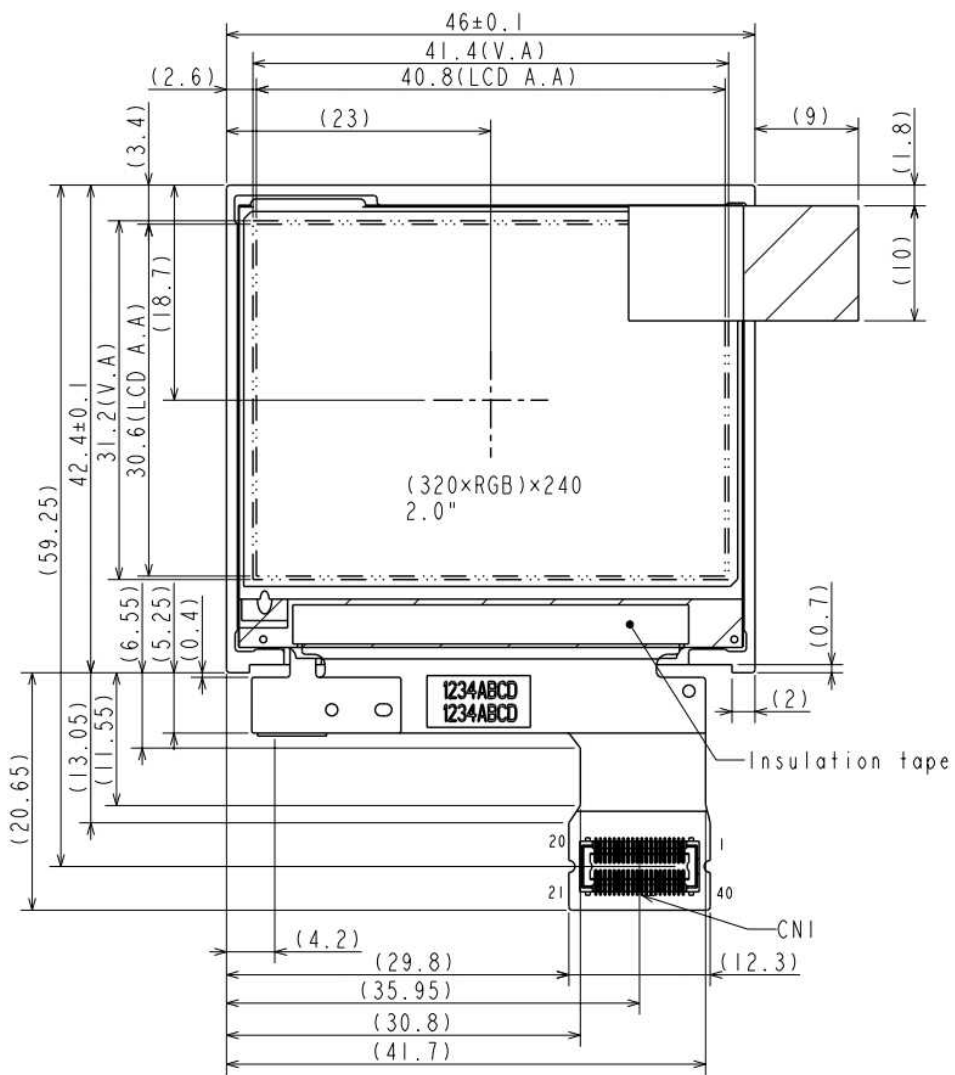
State (g) -> (b)		
		Previous data
1	GRAM write	0x2C
2		Display data write
		Image size 320x240
3	SLEEP OUT	0x11
4		wait 60ms
5	Normal display	0x13
6	Display On	0x29

State (b) -> (g)		
		Previous data
1	Display OFF	0x28

State (b) -> (c)		
		Previous data
1	Partial display	0x12
2	GRAM write	0x2C
3		Display data write
		Image size 320x48
4	Idle mode on	0x39

State (c) -> (b)		
		Previous data
1	Idle mode off	0x38
2	GRAM write	0x2C
3		Display data write
		Image size 320x240
4	Normal display	0x13

9. Dimensional outline



No.	SIGNAL
1	GND
2	LED C1
3	LED C4
4	LED A
5	GND
6	RESET
7	GND
8	D15
9	D13
10	D11
11	D9
12	D7
13	D5
14	D3
15	D1
16	RD/
17	RS
18	VSYNC-0
19	10VCC(1.8V)
20	GND
21	GND
22	VDD(2.8V)
23	MakerID(GND Level)
24	CS/
25	WR/
26	D0
27	D2
28	D4
29	D6
30	D8
31	D10
32	D12
33	D14
34	GND
35	GND
36	IF(IM) Note(4)
37	GND
38	LED C3
39	LED C2
40	GND

Note
 (1) The unspecified tolerance: ±0.2
 (2) CNI: AXK7L40227(Matsushita)
 (3) VDD(analog)=2.8V, 10VCC(logic)=1.8~2.8V
 (4) Select CPU interface mode
 Low: 8bit interface
 High: 16bit interface

Scale: NTS
 Unit: mm