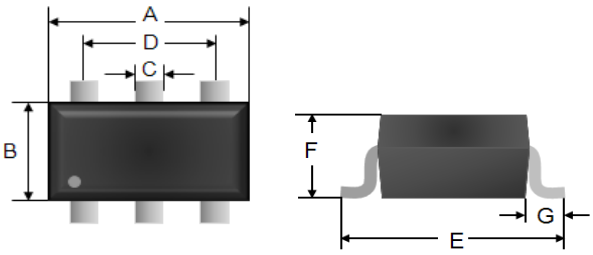
TAIWAN SEMICONDUCTOR

TESDS5V0ALC
Steering Diode Structure ESD Protection Array

Small Signal Diode

SOT-26



Dimensions	Unit (mm)		Unit (inch)	
	Min	Max	Min	Max
A	2.80	3.00	0.110	0.118
B	1.50	1.70	0.059	0.067
C	0.30	0.50	0.012	0.020
D	1.80	2.00	0.071	0.079
E	2.65	2.95	0.104	0.112
F	1.05	1.15	0.041	0.045
G	0.575 REF		0.022 REF	

Features

- ✧Meet IEC61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
- ✧Meet IEC61000-4-4 (EFT) rating. 40A (5/50ήs)
- ✧Meet IEC61000-4-5 (Lightning) rating. 24A (8/20μs)
- ✧Protects four high speed I/O lines
- ✧Working Voltage : 5V
- ✧Pb free version, RoHS compliant, and Halogen free

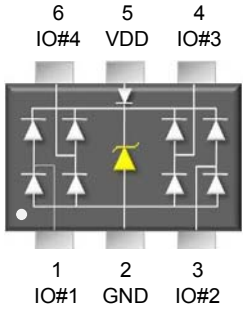
Mechanical Data

- ✧Case : SOT-26 standard package, molded plastic
- ✧Terminal: Matte tin plated, lead free, solderable per MIL-STD-202, Method 202 guaranteed
- ✧High temperature soldering guaranteed: 260°C/10s
- ✧Molding Compound Flammability Rating : UL 94V-O
- ✧Weight :16 mg (approximately)
- ✧Marking Code : Y B05

Applications

- ✧USB Power & Data Line Protection
- ✧Notebooks, Desktops, Servers and Video Graphics Cards
- ✧Monitors and Flat Panel Displays
- ✧Portable Instrumentation
- ✧Set Top Box

Pin Configutation



Ordering Information

Part No.	Package	Packing	Packing Code	Marking
TESDS5V0ALC	SOT-26	3K / 7" Reel	RFG	Y B05

Maximum Ratings and Electrical Characteristics

Rating at 25°C ambient temperature unless otherwise specified.

Maximum Ratings

Type Number	Symbol	Value	Units
Peak Pulse Power (tp=8/20μs waveform)	P_{PP}	200	W
Peak Pulse Current (tp = 8/20μs)	I_{PP}	5	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±27 ±16	KV
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to + 150	°C

Electrical Characteristics

Type Number		Symbol	Min	Max	Units
Reverse Stand-Off Voltage		V_{RWM}	-	5	V
Reverse Breakdown Voltag	I_R= 1mA	$V_{(BR)}$	6.5	-	V
Reverse Leakage Current	V_R= 5V	I_R	-	0.1	uA
Clamping Voltage	I_{PP}= 1A	Vc	-	9.8	V
	I_{PP}= 3A		-	17	
Junction Capacitance	V_R=0V, f=1.0MHz	C_J	0.7 (Typ.)		pF

Small Signal Diode

Rating and Characteristic Curves

FIG 1 Non-Repetitive Peak Pulse Power vs. Pulse Time

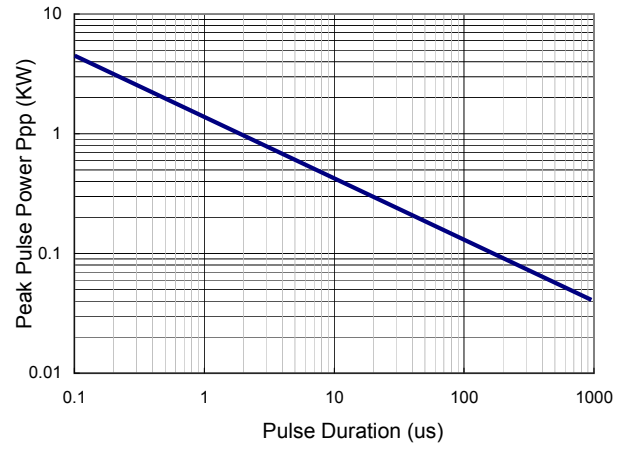


FIG 2 Pulse Waveform

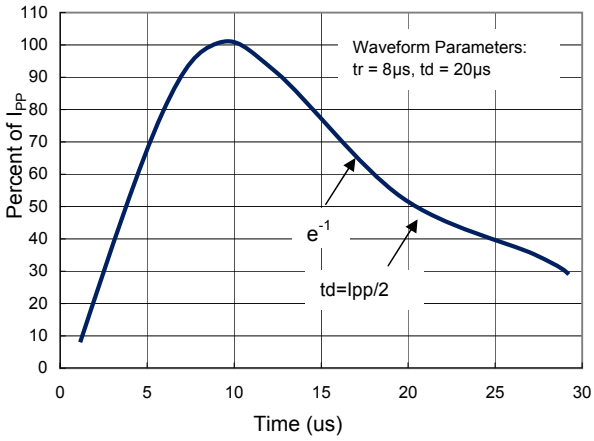


FIG 3 Admissible Power Dissipation Curve

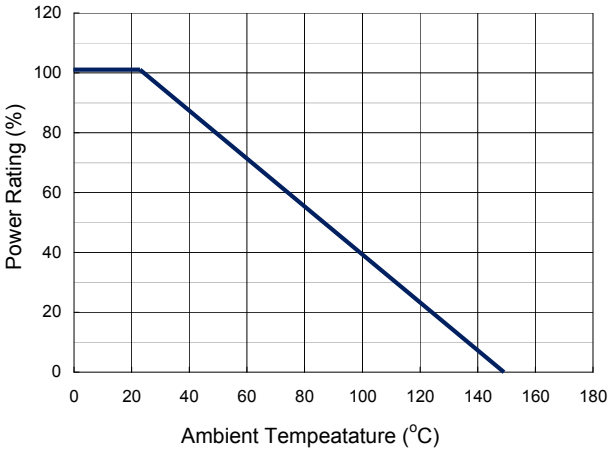


FIG 4 Typical Junction Capacitance

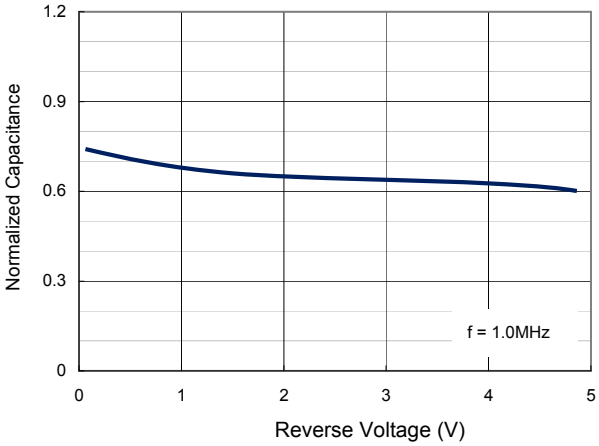
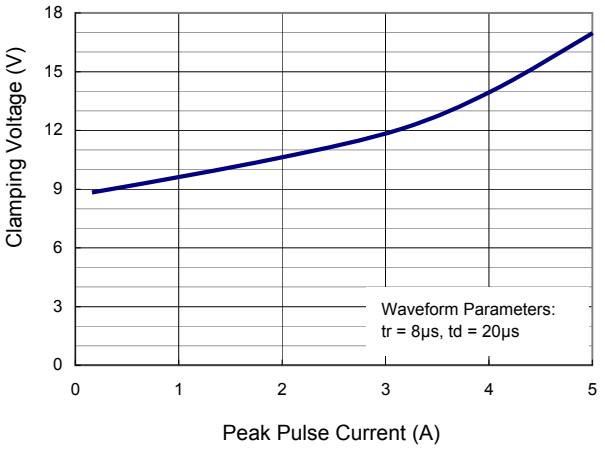


FIG 5 Clamping Voltage vs. Peak Pulse Current



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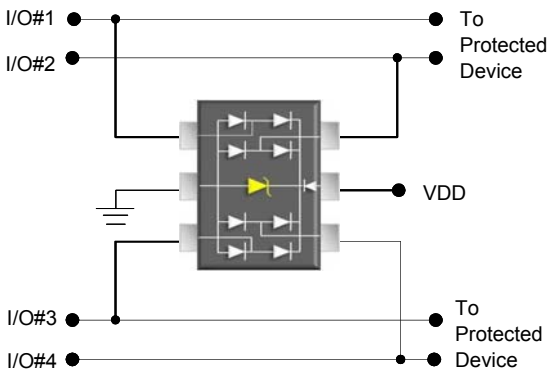
Applications Information

✧Designed to protect protect high speed data interfaces
✧Designed to protect four data lines from transient over-voltages by clamping them to a fixed reference
✧Designed to protect protect sensitive components which are connected to data and transmission lines from overvoltage caused by electrostatic discharge (ESD), electrical fast transients (EFT), and lightning.
✧TESDS5V0ALC incorporates eight surge rated, low capacitance steering diodes and a TVS diode in a single package
✧During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground
✧The internal TVS diode prevents over-voltage on the power line, protecting any downstream components

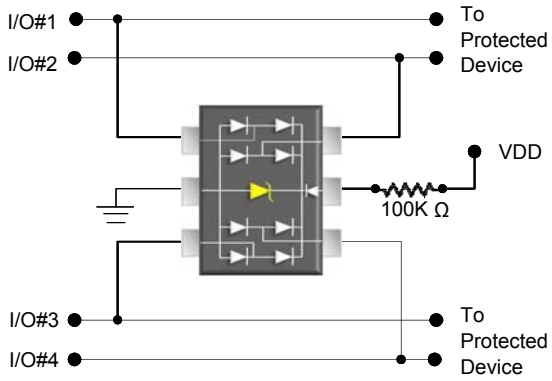
Circuit Board Layout Recommendations

✧To protect data lines and the power line, connect pin 5 directly to the VDD. In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail.
✧The TESDS5V0ALC can be isolated from the power supply by adding a series resistor between pin 5 and VDD. A value of 100kΩ is recommended. The internal TVS and steering diodes remain biased, providing the advantage of lower capacitance.

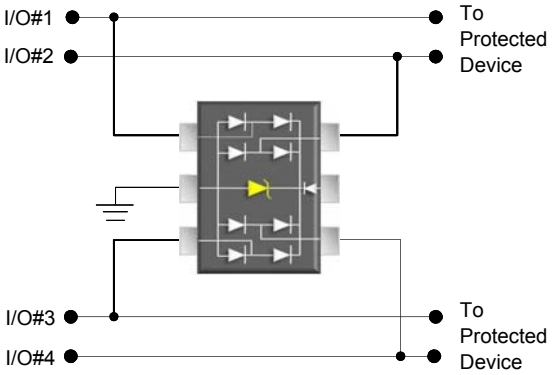
²In applications where no positive supply reference is available, or complete supply isolation is desired, the internal TVS may be used as the reference. In this case, pin 5 is not connected. The steering diodes will begin to conduct when the voltage



✧Data Line and Power Supply Protection Using Vcc as reference



✧Data Line Protection with Bias and Power Supply Isolatior



✧Data Line Protection Using Internal TVS Diode as Reference

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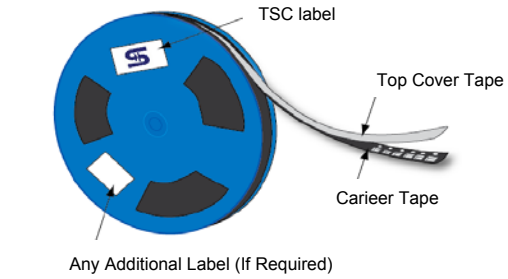
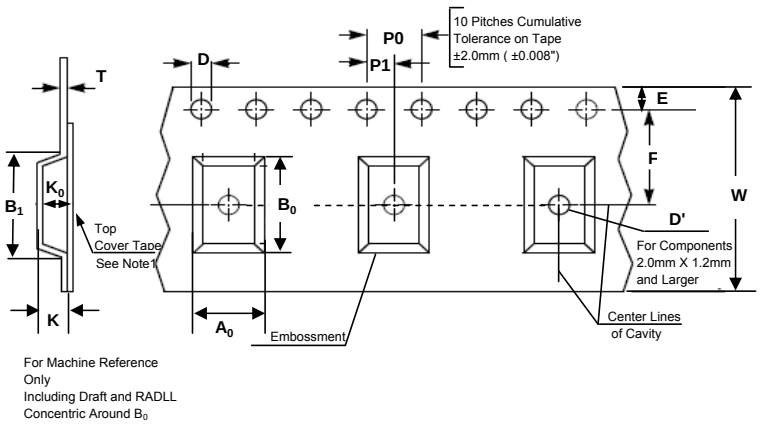
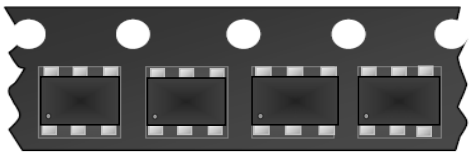
Tape & Reel specification

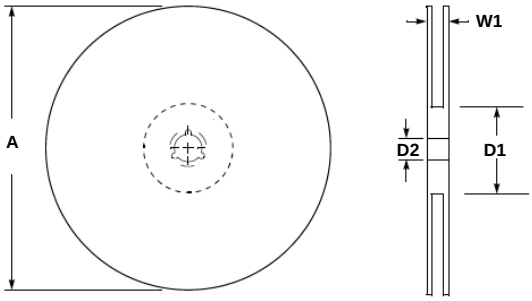


Item	Symbol	Dimension (mm)
Carrier depth	K	1.22 Max.
Sprocket hole	D	1.50 +0.10
Reel outside diameter	A	180 ± 1
Reel inner diameter	D1	50 Min.
Feed hole width	D2	13.0 ± 0.5
Sprocke hole position	E	1.75 ±0.10
Sprocke hole pitch	P0	4.00 ±0.10
Embossment center	P1	2.00 ±0.10
Overall tape thickness	T	0.6 Max.
Tape width	W	8.30 Max.
Reel width	W1	14.4 Max.

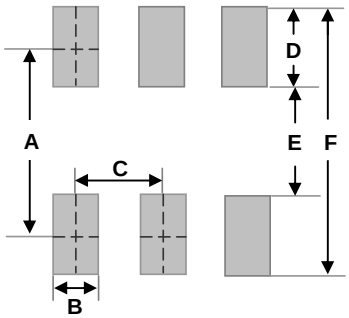




Direction of Feed



Suggested PAD Layout



Dimensions	Unit (inch)	Unit (mm)
A	0.098	2.50
B	0.024	0.60
C	0.037	0.95
D	0.043	1.10
E	0.055	1.40
F	0.142	3.60

Note 1: A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min. to 0.5 mm max. The component cannot rote more than 10° within the determined cavity.

Note 2: If B_1 exceeds 4.2 mm(0.165") for 8 mm embossed tape, the tape may not feed through all tape feeders.

Note 3: The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary despending on application.