



SANYO Semiconductors

DATA SHEET

LA75694M — Monolithic Linear IC For Use in TV/VTR Applications IF Signal Processing (VIF/SIF for Hi-Fi)

Overview

The LA75694M is a PAL/NTSC split Support VIF/SIF for Hi-Fi signal-processing IC that makes the minimum number of adjustments possible. The system is designed so that VCO adjustment makes AFT adjustment unnecessary, thus simplifying the adjustment steps in endproduct manufacturing. PLL detection is adopted in the FM detector, allowing the LA75694M to support multichannel detection for the audio signal. In addition, it also incorporates a buzz canceller that suppresses Nyquist buzz for improved audio quality.

Functions

- VIF Block: VIF Amplifier, Buzz Canceller, BNC, PLL Detector, IF AGC, RF AGC, AFT, Equalizer Amplifier
- 1st SIF Block: 1st SIF Amplifier, 1st SIF Detector, AGC
- SIF Block: HPF, MIX, 500kOSC

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		6	V
Circuit voltage	V ₁₃ , V ₁₇		V _{CC}	V
Circuit current	I ₆		-3	mA
	I ₁₀		-10	mA
Allowable power dissipation	Pd max	Ta ≤ 50°C, Independent IC	420	mW
		Mounted on a board. *	720	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-55 to +150	°C

* When mounted on a 65×72×1.6mm³ paper phenol board.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V _{CC}		5	V
Operating voltage	V _{CC} op		4.5 to 5.5	V

■ Any and all SANYO Semiconductor products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO Semiconductor representative nearest you before using any SANYO Semiconductor products described or contained herein in such applications.

■ SANYO Semiconductor assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor products described or contained herein.

SANYO Semiconductor Co., Ltd.

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

LA75694M

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $f_p = 45.75\text{MHz}$

VIF Block

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current	I_5		38	45	51.8	mA
Maximum RF AGC voltage	V_{14H}		$V_{CC}-0.5$	V_{CC}		V
Minimum RF AGC voltage	V_{14L}			0	0.5	V
Input sensitivity	V_i	S1 = OFF	27	33	39	dB μ V
AGC range	GR		53	58		dB
Maximum allowable input	V_i max		90	96		dB μ V
No-signal video output voltage	V_6		2.1	2.4	2.7	V
Sync. signal tip voltage	V_6 tip		0.7	1.0	1.3	V
Video output level	V_O		0.95	1.1	1.25	Vp-p
Black noise threshold voltage	V_{BTH}		0.5	0.8	1.1	V
Black noise clamp voltage	V_{BCL}		1.2	1.5	1.8	V
Video S/N	S/N		48	52		dB
C-S best	IC-S		38	43		dB
Frequency characteristics	f_c	6MHz	-3	-1.5		dB
Differential gain	DG			3	6.5	%
Differential phase	DP			3	5	$^\circ\text{C}$
No-signal AFT voltage	V_{13}		2.0	2.5	3.0	V
Maximum AFT voltage	V_{13H}		4.0	4.4	5.0	V
Minimum AFT voltage	V_{13L}		0	0.18	1.0	V
AFT detection sensitivity	S_f		14	21	28	mV/kHz
VIF input resistance	R_i	45.75MHz		1.5		k Ω
VIF input capacitance	C_i	45.75MHz		3		pF
APC pull-in range (U)	fpu		0.7	1.5		MHz
APC pull-in range (L)	fpl			-2.0	-1.4	MHz
AFT tolerance frequency 1	ΔF_{a1}		-200	0	200	kHz
VCO1 maximum variable range (U)	dfu		1.0	1.5		MHz
VCO1 maximum variable range (L)	dfl			-2.0	-1.4	MHz
VCO control sensitivity	β		1.2	3.2	5.0	kHz/mV
Synchronization ratio	V_S		25.0	28.5	31.5	%

1st SIF Block

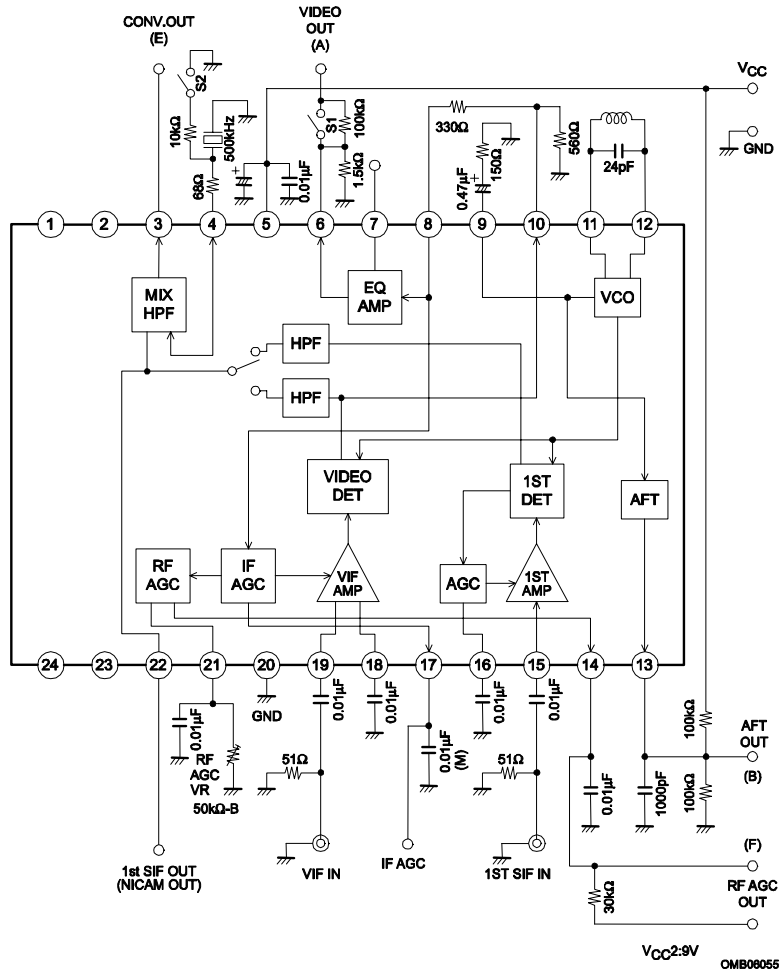
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Conversion gain	V_G		27	33	39	dB
4.5MHz output level	S_O		53	115	180	mVrms
1st SIF maximum input	S_i max		8	16		mVrms
1st SIF input resistance	R_i (SIF)	41.25MHz		2		k Ω
1st SIF input capacitance	C_i (SIF)	41.25MHz		3		pF

SIF Converter

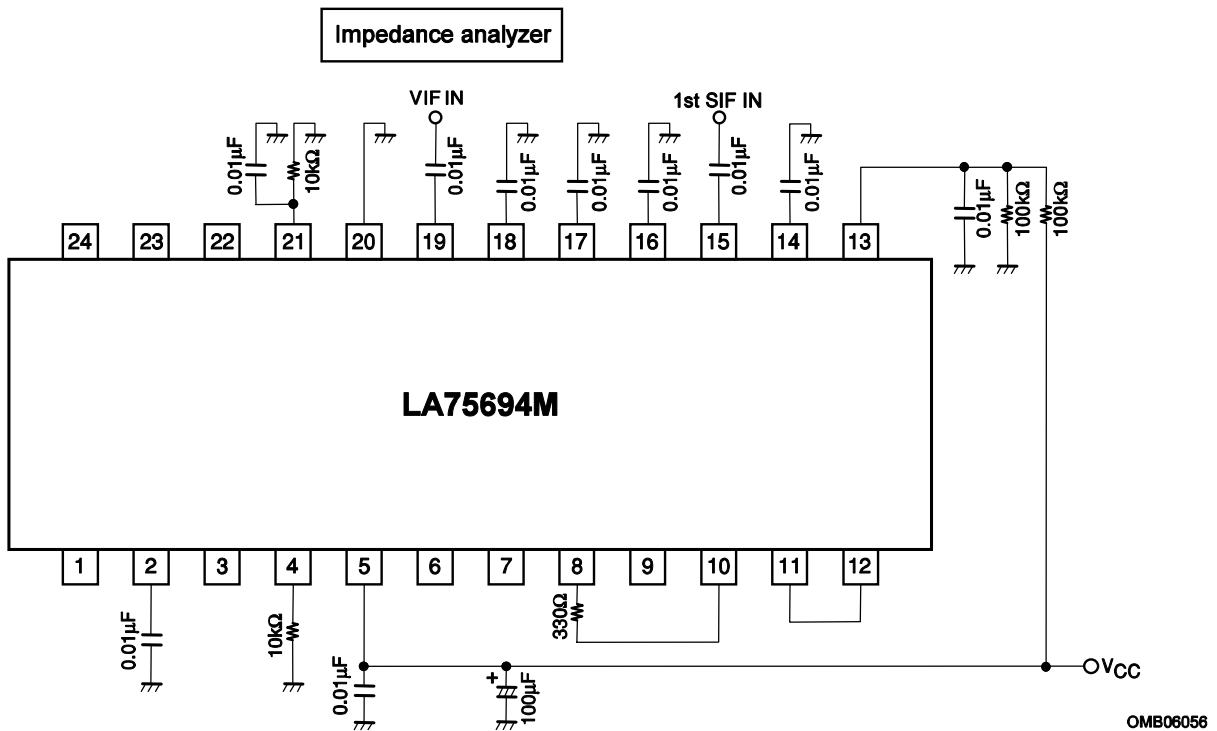
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Conversion gain	V_G (SIF)		8	11	14	dB
Maximum output level	V max		103	109	115	dB μ V
Carrier suppression ratio	V_{GR} (4.5)		15	21		dB
Oscillator level	V_{OSC}		35	70		mVp-p
OSC leakage	OSC leak		14	25		dB
Oscillator stop current	I_4				300	μA

LA75694M

Block Diagram and AC Characteristics Test Circuit



Input Impedance Test Circuit



Test Conditions**V1. Circuit current [I₅]**

- (1) Internal AGC
- (2) Input a 45.75MHz 10mV_{rms} continuous wave to the VIF input pin.
- (3) RF AGC V_r MAX
- (4) Connect an ammeter to the V_{CC} and measure the incoming current.

V2.V3. Maximum RF AGC voltage, Minimum RF AGC voltage [V_{14H}, V_{14L}]

- (1) Internal AGC
- (2) Input a 45.75MHz 10mV_{rms} continuous wave to the VIF input pin.
- (3) Adjust the RF AGC V_r (resistor value max.) and measure the maximum RF AGC voltage. F
- (4) Adjust the RF AGC V_r (resistor value min.) and measure the minimum RF AGC voltage. F

V4. Input sensitivity [V_i]

- (1) Internal AGC
- (2) f_p = 45.75MHz 400Hz 40% AM (VIF input)
- (3) Turn off the S1 and put 100kΩ through.
- (4) VIF input level at which the 400Hz detection output level at test point A becomes 0.35V_{p-p}.

V5. AGC range [GR]

- (1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
- (2) In the same manner as for the V4 (input sensitivity), measure the VIF input level at which the detection output level becomes 0.35V_{p-p}. V_{il}

(3) $GR = 20 \log \frac{V_{il}}{V_i} \text{ dB}$

V6. Maximum allowable input [V_i max]

- (1) Internal AGC
- (2) f_p = 45.75MHz 15kHz 78% AM (VIF input)
- (3) VIF input level at which the detection output level at test point A is video output (V_O) ±1dB.

V7. No-signal video output voltage [V₆]

- (1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
- (2) Measure the DC voltage of VIDEO output (A).

V8. Sync. signal tip voltage [V_{6tip}]

- (1) Internal AGC
- (2) Input a 45.75MHz 10mV_{rms} continuous wave to the VIF input pin.
- (3) Measure the DC voltage of VIDEO output (A).

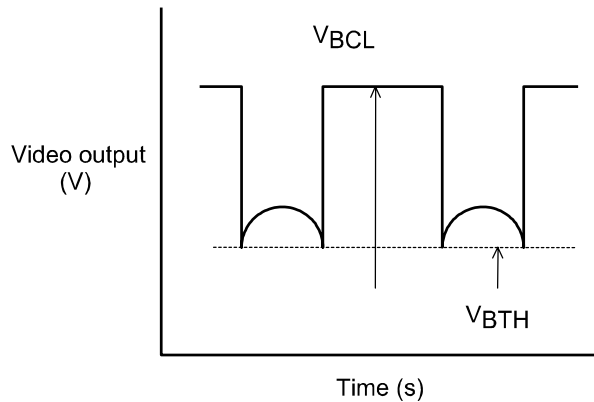
V9. Video output level [V_O]

- (1) Internal AGC
- (2) f_p = 45.75MHz 15kHz 78% AM V_i = 10mV_{rms} (VIF input)
- (3) Measure the peak value of the detection output level at test point A. (V_{p-p})

LA75694M

V10.V11. Black noise threshold level and clamp voltage [V_{BTH}, V_{BCL}]

- (1) Apply DC voltage to the external AGC, IF AGC (pin 17) and adjust the voltage.
- (2) $f_p = 45.75\text{MHz}$ 400Hz 40% AM 10mVrms (VIF input)
- (3) Adjust the IF AGC (pin 17) voltage to operate the noise canceller.
Measure the V_{BTH}, V_{BCL} at test point A.



OMG06012

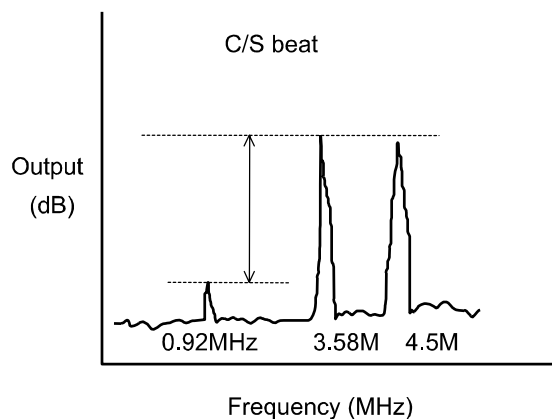
V12. Video S/N [S/N]

- (1) Internal AGC
- (2) $f_p = 45.75\text{MHz}$ CW = 10mVrms (VIF input)
- (3) Measure the noise voltage at test point A in RMS volts through a 10kHz to 4MHz band-pass filter.
..... Noise voltage (N)

$$(4) S/N = 20 \log \frac{\text{Video portion (Vp-p)}}{\text{Noise voltage (Vrms)}} = 20 \log \frac{1.12\text{Vp-p}}{\text{Noise voltage (Vrms)}} \text{ (dB)}$$

V13. C/S beat [I-C-S]

- (1) Apply DC voltage to the external AGC IF AGC (pin 17) and adjust the voltage.
- (2) $f_p = 45.75\text{MHz}$ CW; 10mVrms
 $f_c = 42.17\text{MHz}$ CW; 10mVrms – 10dB
 $f_s = 41.25\text{MHz}$ CW; 10mVrms – 10dB
- (3) Adjust the IF AGC (pin 17) voltage so that the output level at test point A becomes 0.72Vp-p.
- (4) Measure the difference between the levels for 3.58MHz and 0.92MHz components at test point A.



OMG06011

LA75694M

V14. Frequency characteristics [fc]

- (1) Apply DC voltage to the external AGC IF AGC (pin 17) and adjust the voltage.
- (2) SG1 : 45.75MHz continuous wave 10mVrms
SG2 : 45.65MHz to 39.75MHz continuous wave 2mVrms
Add the SG1 and SG2 signals using a T pat and adjust each SG signal level so that the above-mentioned levels are reached and input the added signals to the VIF IN.
- (3) First set the SG2 frequency to 45.65MHz, and then adjust the IF AGC voltage (V17) so that the output level at test point A becomes 0.5Vp-p. V1
- (4) Set the SG2 frequency to 39.75MHz and measure the output level. V2
- (5) Calculate as follows :

$$fc = 20 \log \frac{V2}{V1} \text{ (dB)}$$

V15.V16. Differential gain, differential phase [DG, DP]

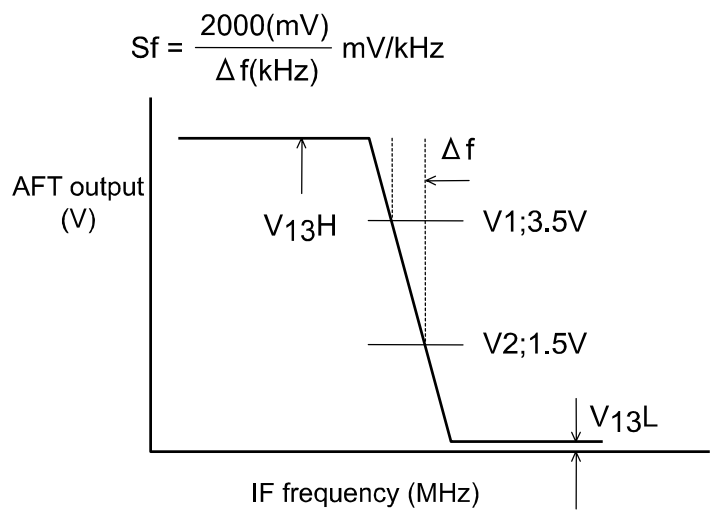
- (1) Internal AGC
- (2) fp = 45.75MHz APL50% 87.5% modulation video signal Vi = 10mVrms
- (3) Measure the DG and DP at test point A.

V17. No-signal AFT voltage [V13]

- (1) Internal AGC
- (2) Measure the DC voltage at the AFT output (B).

V18.V19.V20. Maximum, minimum AFT output voltage, AFT detection sensitivity [V13H, V13L, Sf]

- (1) Internal AGC
- (2) fp = 45.75MHz ±1.5MHz Sweep = 10mVrms (VIF input)
- (3) Maximum voltage : V13H, minimum voltage : V13L.
- (4) Measure the frequency deviation at which the voltage at test point B changes from V1 to V2. Δf



V21.V22. VIF input resistance, Input capacitance [Ri, Ci]

- (1) Referring to the Input Impedance Test Circuit, measure Ri and Ci with an impedance analyzer.

V23.V24. APC pull-in range [fpu, fpl]

- (1) Internal AGC
- (2) $f_p = 39\text{MHz}$ to 51MHz continuous wave; 10mVrms
- (3) Adjust the SG signal frequency to be higher than $f_p = 45.75\text{MHz}$ to bring the PLL to unlocked state.
Note : The PLL is assumed to be in unlocked state when a beat signal appears at test point A.
- (4) When the SG signal frequency is lowered, the PLL is brought to locked state again. f_1
- (5) Lower the SG signal frequency to bring the PLL to unlock state.
- (6) When the SG signal frequency is raised, the PLL is brought to locked state again. f_2
- (7) Calculate as follows :

$$f_{pu} = f_1 - 45.75\text{MHz}$$

$$f_{pl} = f_2 - 45.75\text{MHz}$$

V25. AFT tolerance frequency 1 [ΔFa_1]

- (1) Internal AGC
- (2) SG1 : 43.75MHz to 47.75MHz variable continuous wave 10mVrms
- (3) Adjust the SG1 signal frequency so that the AFT output DC voltage (test point B) becomes 2.5V ; that SG1 signal frequency is f_1 .
- (4) External AGC (Adjust the V17.)
- (5) Apply 5V to the IF AGC (pin 17) and then pick up the VCO oscillation frequency from GND, etc.; and measure the frequency f_2
- (6) Calculate as follows :
AFT tolerance frequency : $\Delta Fa_1 = f_2 - f_1$ (kHz)

V26.V27. VCO maximum variable range (U, L) [dfu, dfl]

- (1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
- (2) Pick up the VCO oscillation frequency from the VIDEO output (A), GND, etc. and adjust the VCO coil so that the frequency becomes 45.75MHz .
- (3) f_l is taken as the frequency when 1V is applied to the APC pin (pin 9).
In the same manner, f_u is taken as the frequency when 5V is applied to the APC pin (pin 9).

$$df_u = f_l - 45.75\text{MHz}$$

$$df_l = f_l - 45.75\text{MHz}$$

V28. VCO control sensitivity [β]

- (1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
- (2) Pick up the VCO oscillation frequency from the VIDEO output (A), GND, etc. and adjust the VCO coil so that the frequency becomes 45.75MHz .
- (4) f_1 is taken as the frequency when 3.0V is applied to the APC pin (pin 9).
In the same manner, f_2 is taken as the frequency when 3.4V is applied to the APC pin (pin 9).

$$\beta = \frac{f_2 - f_1}{400} \text{ (kHz/mV)}$$

V29. Synchronization ratio [V_S]

- (1) Internal AGC
- (2) $f_p = 45.75\text{MHz}$ 87.5% 10STEP B/W
 $V_i = 10\text{mVrms}$
- (3) Measure the output amplitude at the measuring point A. V_{video}
- (4) Measure the pedestal voltage (DC) at the measuring point A. V_{ped}

$$V_S = (V_{\text{ped}} - V_{\text{Gtip}}) / V_{\text{video}} \times 100 \text{ (\%)}$$

F1. 1st SIF conversion gain [VG]

- (1) Internal AGC
- (2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; 500μV (1st SIF input) V1
- (3) Detection output level at test point C (Vrms) V2 (4.5MHz)
- (4) $VG = 20\log \frac{V2}{V1} \text{ dB}$

F2. 4.5MHz output level [SO]

- (1) Internal AGC
- (2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; 10mV (1st SIF input) V1
- (3) Detection output level at test point C (4.5MHz) SO (mVrms)

F3. 1st SIF maximum input [Si max]

- (1) Internal AGC
- (2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; variable (1st SIF input)
- (3) Input level at which the detection output at test point C (4.5MHz) becomes SO ±2dB. Si max

F4.F5. 1st SIF input resistance, Input capacitance [Ri (SIF), Ci (SIF)]

- (1) Using an input analyzer, measure Ri and Ci in the input impedance measuring circuit.

C1. Converter conversion gain [VG (SIF)]

- (1) Internal AGC
- (2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; 316μV (1st SIF input)
- (3) Measure the 6MHz component at test point E (MIX output) V1
- (4) Measure the 4.5MHz component at test point F (NICAM output). V2
- (5) $VG(SIF) = 20\log \frac{V1}{V2} \text{ dB}$

C2. SIF converter maximum output level [V max]

- (1) Internal AGC
- (2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; 10mV (1st SIF input)
- (3) Measure the 6MHz component at test point E (MIX output). V max (dBμV)

C3. Carrier suppression ratio [VGR (4.5)]

- (1) Internal AGC
- (2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; 316μV (1st SIF input)
- (3) Measure the 6MHz component at test point E (MIX output). V6 (dBμV)
- (4) Measure the 4.5MHz component at test point E (MIX output). V4.5 (dBμV)
- (5) Perform the following calculation.
Carrier suppression ratio VGR (4.5) (dB) = V6 – V4.5

C5. OSC leakage [OSC leak]

- (1) Internal AGC
- (2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; 316μV (1st SIF input)
- (3) Measure the 6MHz component at test point E (MIX output). V6 (dBμV)
- (4) Measure the 500kHz component at test point E (MIX output). V0.5 (dBμV)
- (5) Perform the following calculation.
Carrier suppression ratio OSC leak (dB) = V6 – V0.5

LA75694M

- Note 1) Unless otherwise specified for VIF test, apply the V_{CC} voltage to the IF AGC and adjust the VCO coil so that oscillation occurs at 45.75MHz.
- 2) Unless otherwise specified, the SW1 must be ON.

- Specifications of any and all SANYO Semiconductor products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- SANYO Semiconductor Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Semiconductor Co., Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO Semiconductor believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of April, 2006. Specifications and information herein are subject to change without notice.