



UR6515A

LINEAR INTEGRATED CIRCUIT

3A DDR BUS TERMINATION REGULATOR

DESCRIPTION

The **UR6515A** is a linear regulator providing up to 3A transient peak current sourcing and sinking capability for DDR SDRAM bus terminator applications while regulating an output voltage to within 40mV. It contains a high speed operational amplifier which provides fast load transient response and only requires 10uF of ceramic output capacitance.

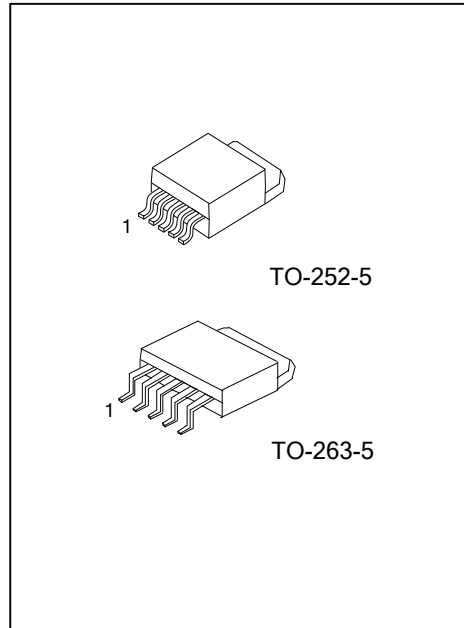
The **UR6515A** output termination voltage tracks the reference voltage applied at V_{REF} pin. A resistor divider connected to V_{IN} , GND and V_{REF} pins is used to force the reference voltage to V_{REF} pin. Additional features include current limiting protection and thermal shutdown protection.

FEATURES

- *DDR1/ DDR2 termination voltage applications
- *Low output voltage offset within 20mV
- *Source and sink 3A peak current
- *Adjustable output voltage by external resistors
- *Integrated power MOS devices
- *Suspend to RAM(STR) functionality
- *Current Limiting Protection
- *Thermal Shutdown Protection
- *Cost-effective and easy to use

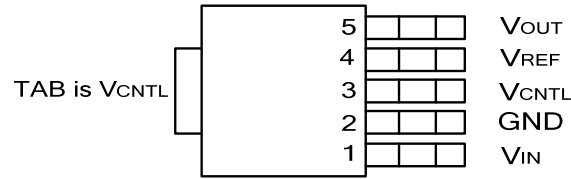
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UR6515L-TN5-R	UR6515G-TN5-R	TO-252-5	Tape Reel
UR6515L-TQ5-R	UR6515G-TQ5-R	TO-263-5	Tape Reel
UR6515L-TQ5-T	UR6515G-TQ5-T	TO-263-5	Tube



<p>UR6515AL-TN5-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Lead Plating</p>	<p>(1) R: Tape Reel, T:Tube</p> <p>(2) TN5: TO-252-5, TQ5: TO-263-5</p> <p>(3) G: Halogen Free, L: Lead Free</p>
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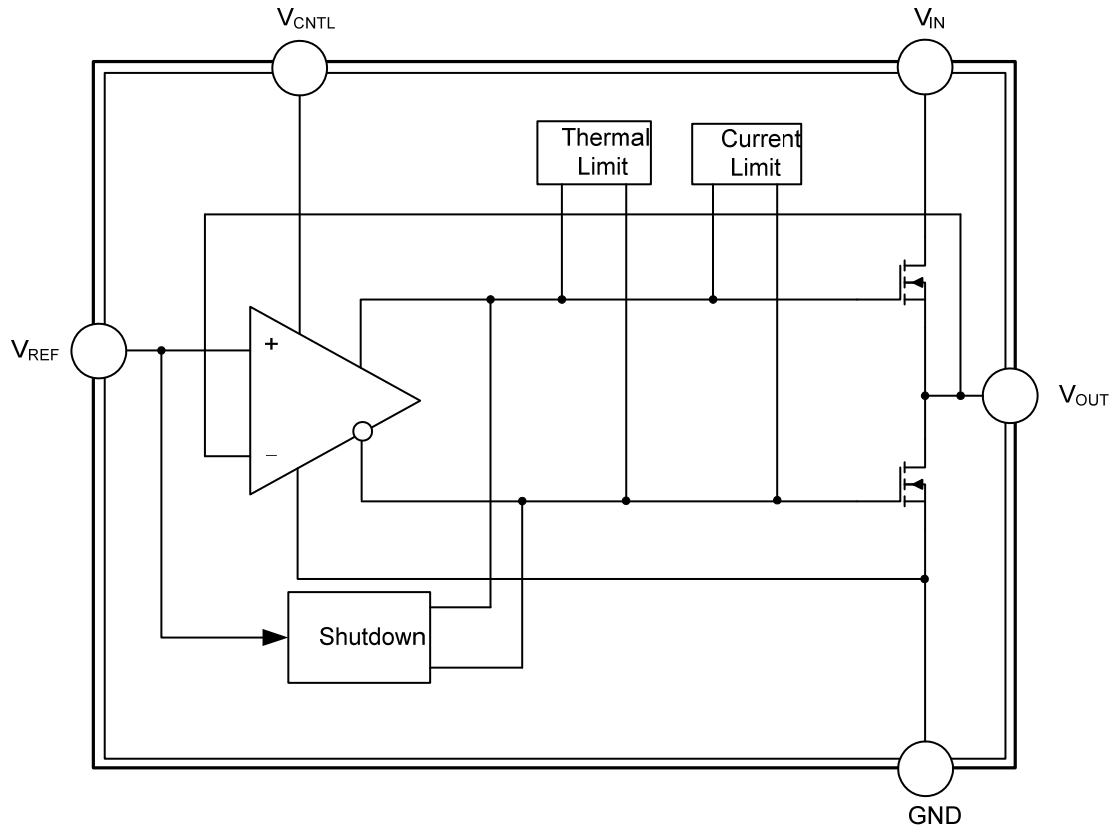
■ PIN CONFIGURATIONS



■ PIN DESCRIPTION

PIN NAME	PIN TYPE	PIN DESCRIPTION
VIN	I	Power supply pin for the VOUT output
GND	O	Ground pin
VCNTL	I	Power supply pin for the internal control circuits
VREF	I	Reference voltage input and active-low shutdown control pin
VOUT	O	Output voltage pin

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
V _{CNTL} Control Voltage	V _{CNTL}	7	V
V _{IN} Supply Voltage	V _{IN}	7	V
Power Dissipation (Ta=25°C)	TO-252-5	1.471	W
	TO-263-5	1.923	
Junction Temperature	T _J	125	°C
Storage Temperature	T _{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient (Note 1)	TO-252-5	68	°C/W
	TO-263-5	52	
Junction to Case	TO-252-5	8	°C/W
	TO-263-5	7.7	

Note: 1. θ_{JA} is measured in the natural convection at Ta = 25°C on a high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard

■ RECOMMENDED OPERATING CONDITIONS (Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
V _{CNTL} Control Voltage	V _{CNTL}	5 or 3 ± 5%	V
V _{IN} Supply Voltage	V _{IN}	2.5~1.5 ± 3%	V
V _{REF} Input Voltage	V _{REF}	1.25~0.75 ± 3%	V
Junction Temperature	T _J	-40~+125	°C

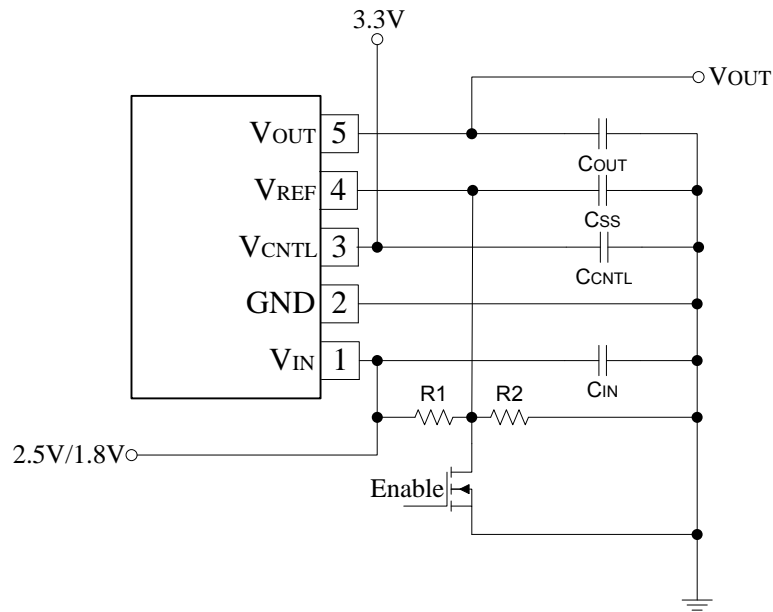
Notes: 1. All voltage values are with respect to the network ground terminal unless otherwise noted.
2. The V_{OUT} tracks the V_{REF} with additional voltage offset and load regulation.

■ ELECTRICAL CHARACTERISTICS (Ta=25°C, unless otherwise specified)

(V_{IN}=2.5V/1.8V, V_{CNTL}=3.3V, V_{REF}=1.25V/0.9V, C_{OUT} = 10μF (Ceramic))

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENT						
Operation Current of V _{CNTL}	I _{CNTL}	I _{OUT} = 0A		1	2.5	mA
Standby Current	I _{STB}	V _{REF} < 0.2V, R _{LOAD} = 180Ω		50	90	μA
OUTPUT VOLTAGE (DDR/DDR II/DDR III)						
Output Voltage Offset (V _{REF} -V _{OUT})	V _{OS}	I _{OUT} = 0A	-20		20	mV
Load Regulation(DDR1/2)	ΔV _{LOAD}	I _{OUT} = ±1.5A		0.8/1.2	2/3	%
PROTECTION						
Current Limit	I _{LIMIT}	V _{IN} = 2.5V/1.8V	3			A
Thermal Shutdown Temperature	T _{SD}	V _{CNTL} = 3.3V~5V	125	150		°C
Thermal Shutdown Hysteresis	ΔT _{SD}	V _{CNTL} = 3.3V~5V		50		°C
V_{REF} Shutdown						
Shutdown Threshold	V _{IH}	Enable	0.8			V
	V _{IL}	Shutdown			0.2	V

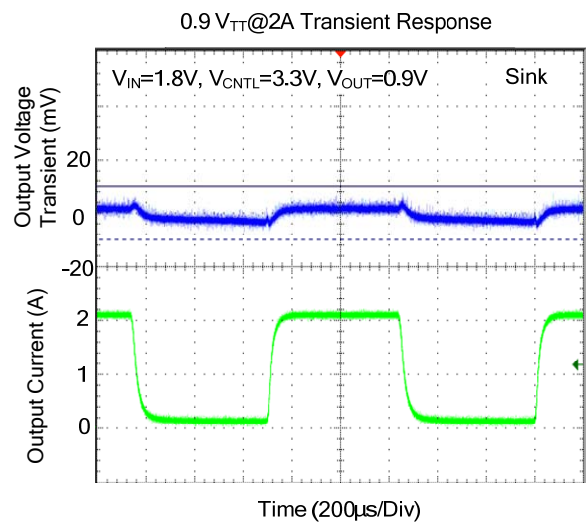
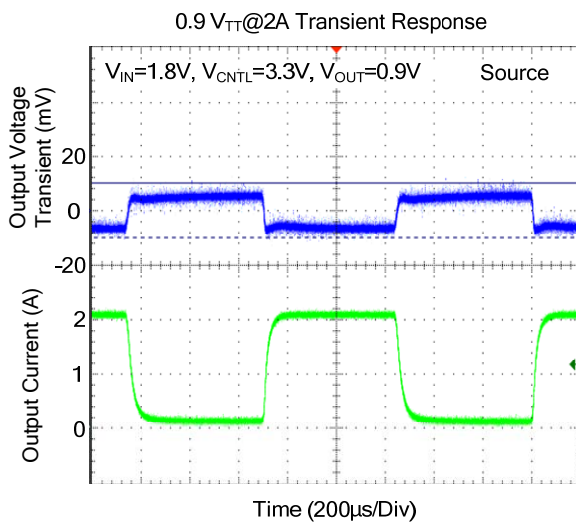
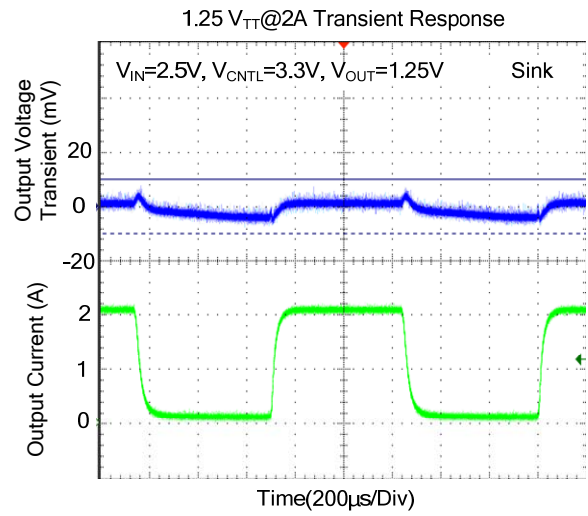
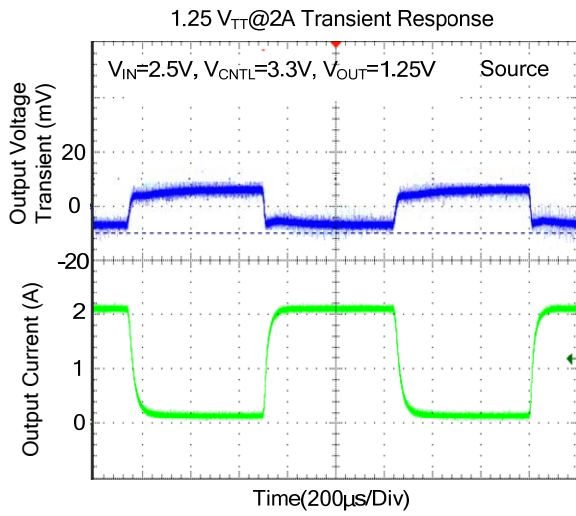
■ TYPICAL APPLICATIONS CIRCUITS



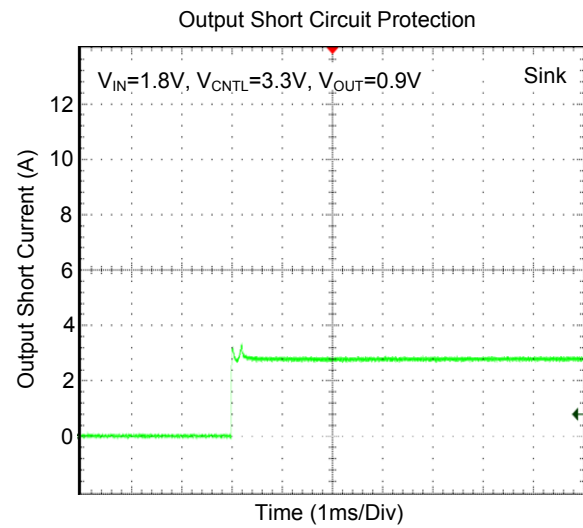
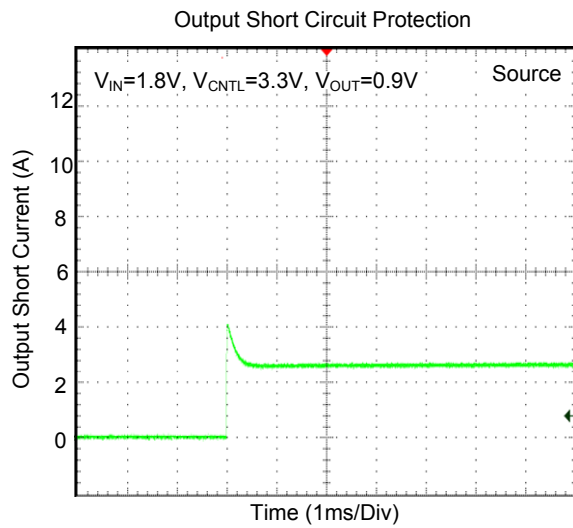
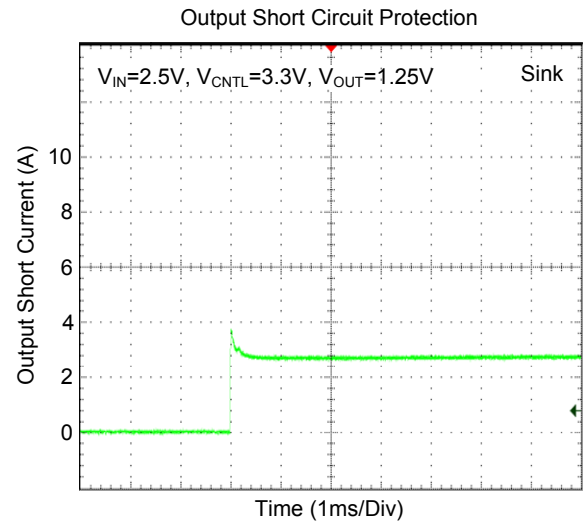
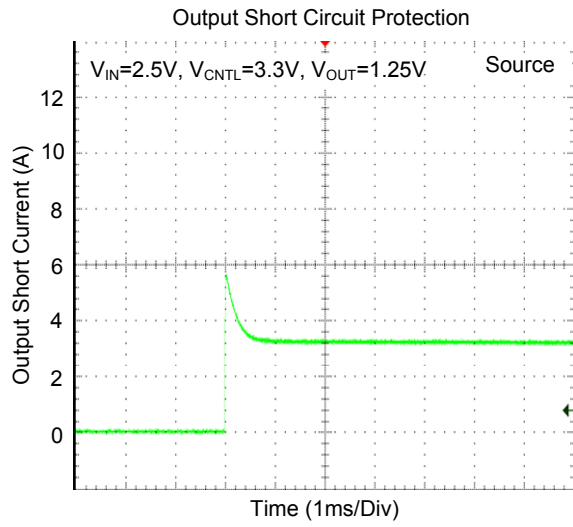
$R1=R2=100K\Omega$, $C_{OUT}=10\mu F(\text{Ceramic})+1000\mu F$ under the worst case testing condition
 $C_{SS}=1\mu F$, $C_{IN}=470\mu F(\text{Low ESR})$, $C_{CNTL}=47\mu F$

$$V_{REF} = \frac{R_2}{R_1 + R_2} V_{IN}(V), V_{OUT} \text{ track } V_{REF}$$

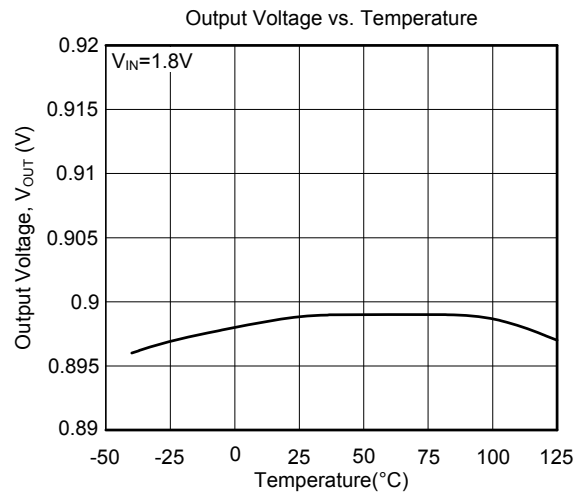
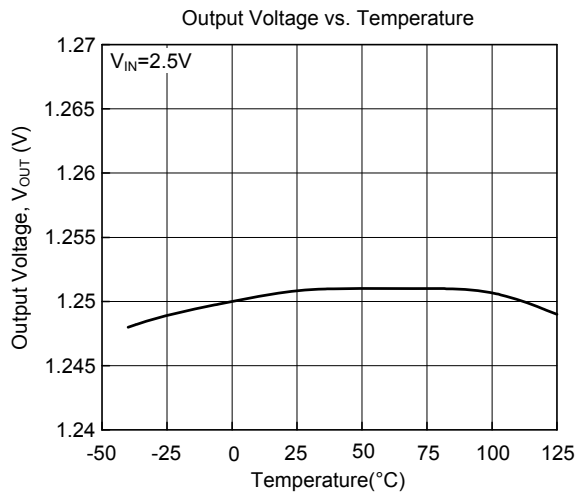
■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS(Cont.)



■ TYPICAL CHARACTERISTICS(Cont.)



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