CY62128EV30 MoBL®

1 Mbit (128K x 8) Static RAM

Features

- Very high speed: 45 ns
- Temperature ranges–
  - — Industrial: –40°C to +85°C
  - — Automotive-A: –40°C to +85°C
  - — Automotive-E: –40°C to +125°C
- Wide voltage range: 2.20V – 3.60V
- Pin compatible with CY62128DV30
- Ultra low standby power
  - — Typical standby current: 1 μA
  - — Maximum standby current: 4 μA
- Ultra low active power
  - — Typical active current: 1.3 mA @ f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2 and $\overline{OE}$ features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Offered in Pb-free 32-pin SOIC, 32-pin TSOP I, and 32-pin STSOP packages

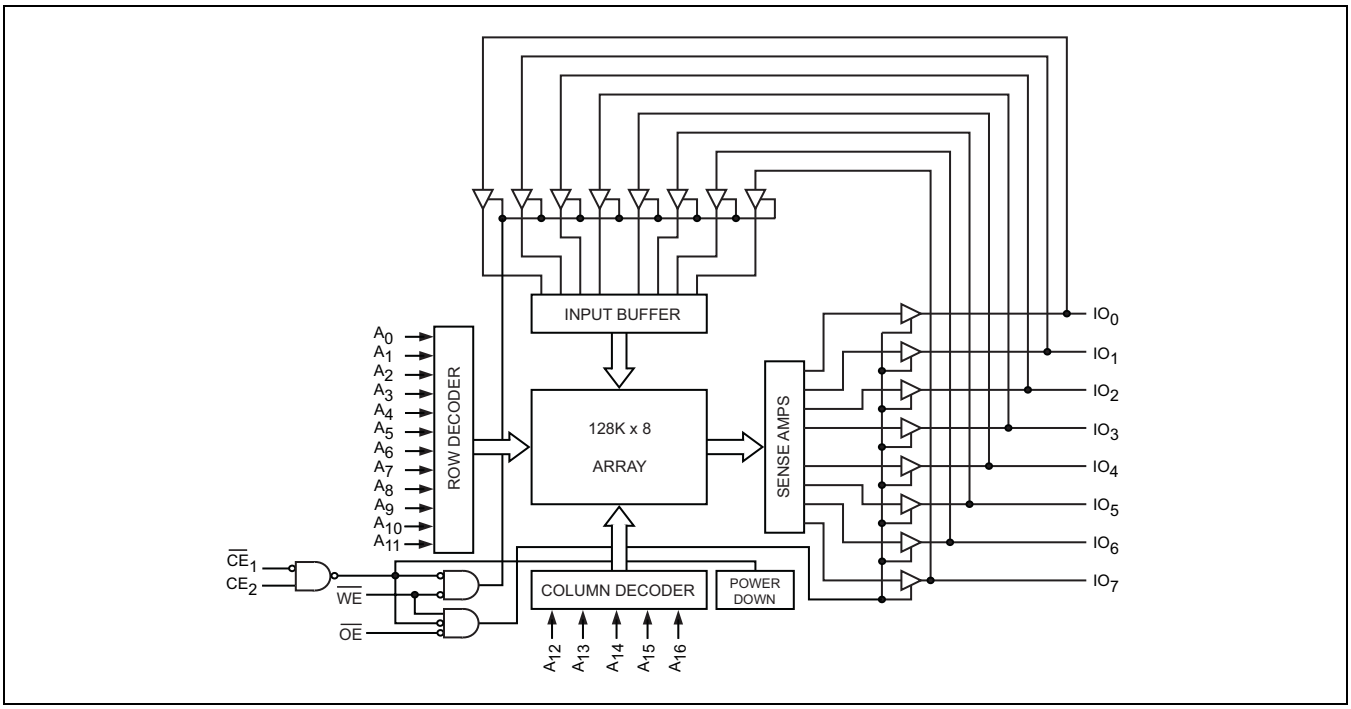
Functional Description[1]

The CY62128EV30 is a high performance CMOS static RAM module organized as 128K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW). The eight input and output pins (IO_0 through IO_7) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or a write operation is in progress ($\overline{CE}_1$ LOW and CE_2 HIGH and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight IO pins is then written into the location specified on the Address pin (A_0 through A_{16}).

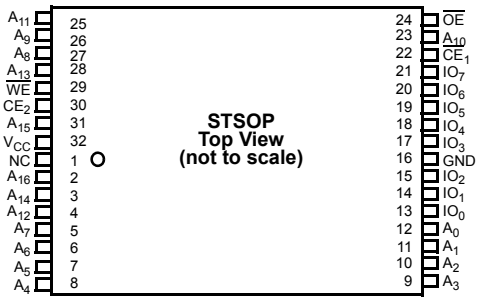
To read from the device, take Chip Enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the IO pins.

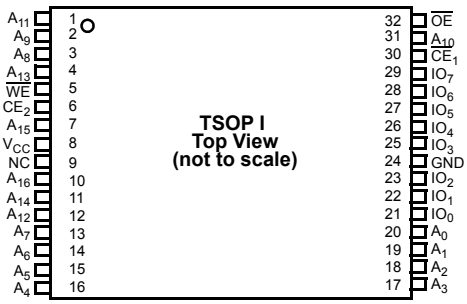
Logic Block Diagram

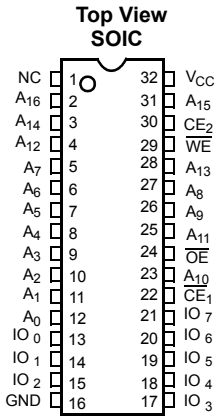


Note
1. For best practice recommendations, refer to the Cypress application note *"System Design Guidelines"* at http://www.cypress.com.

Pin Configuration[2]







Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ[3]	Max		Typ[3]	Max	Typ[3]	Max	Typ[3]	Max
CY62128EV30LL	Ind'l/Auto-A	2.2	3.0	3.6	45	1.3	2.0	11	16	1	4
CY62128EV30LL	Auto-E	2.2	3.0	3.6	55	1.3	4.0	11	35	1	30

Notes:
2. NC pins are not connected on the die.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25°C$.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... 55°C to +125°C

Supply Voltage to Ground Potential ..... –0.3V to $V_{CC(max)}$ + 0.3V

DC Voltage Applied to Outputs in High-Z State[4, 5] ..... –0.3V to $V_{CC(max)}$ + 0.3V

DC Input Voltage[4,5] ..... –0.3V to $V_{CC(max)}$ + 0.3V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (MIL-STD-883, Method 3015)

Latch up Current ..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[6]
CY62128EV30LL	Ind'l/Auto-A	–40°C to +85°C	2.2V to 3.6V
	Auto-E	–40°C to +125°C	

Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	45 ns (Ind'l/Auto-A)			55 ns (Auto-E)			Unit
			Min	Typ[3]	Max	Min	Typ[3]	Max	
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	2.0			2.0			V
		I_{OH} = –1.0 mA, $V_{CC} \geq$ 2.70V	2.4			2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA			0.4			0.4	V
		I_{OL} = 2.1 mA, $V_{CC} \geq$ 2.70V			0.4			0.4	V
V_{IH}	Input HIGH Voltage	V_{CC} = 2.2V to 2.7V	1.8		V_{CC} + 0.3V	1.8		V_{CC} + 0.3V	V
		V_{CC}= 2.7V to 3.6V	2.2		V_{CC} + 0.3V	2.2		V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage	V_{CC} = 2.2V to 2.7V	–0.3		0.6	–0.3		0.6	V
		V_{CC}= 2.7V to 3.6V	–0.3		0.8	–0.3		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	–1		+1	–4		+4	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	–1		+1	–4		+4	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{max} = 1/t_{RC}, V_{CC} = V_{CCmax}, I_{OUT} = 0 mA CMOS levels		11	16		11	35	mA
		f = 1 MHz		1.3	2.0		1.3	4.0	mA
I_{SB1}	Automatic CE Power down Current — CMOS Inputs	$\overline{CE}_1 \geq V_{CC}$–0.2V, CE_2 < 0.2V $V_{IN} \geq V_{CC}$–0.2V, $V_{IN} \leq$ 0.2V) f = f_{max} (Address and Data Only), f = 0 ($\overline{OE}$ and $\overline{WE}$), V_{CC} = 3.60V		1	4		1	35	µA
I_{SB2}[7]	Automatic CE Power down Current — CMOS Inputs	$\overline{CE}_1 \geq V_{CC}$ – 0.2V, CE_2 < 0.2V $V_{IN} \geq V_{CC}$ – 0.2V or V_{IN} < 0.2V, f = 0, V_{CC} = 3.60V		1	4		1	30	µA

Capacitance (For all packages)[8]

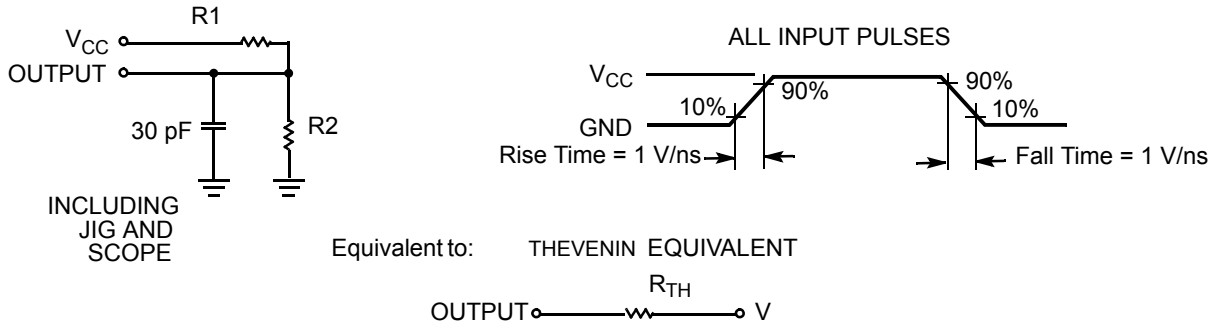
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
4. $V_{IL(min)}$ = –2.0V for pulse durations less than 20 ns.
5. $V_{IH(max)}$ = V_{CC}+0.75V for pulse durations less than 20 ns.
6. Full device AC operation assumes a 100 µs ramp time from 0 to V_{CC}(min) and 200 µs wait time after V_{CC} stabilization.
7. Only chip enables ($\overline{CE}_1$ and CE_2) must be at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
8. Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance

Parameter	Description	Test Conditions	TSOP I	SOIC	STSOP	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	33.01	48.67	32.56	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		3.42	25.86	3.59	°C/W

AC Test Loads and Waveforms

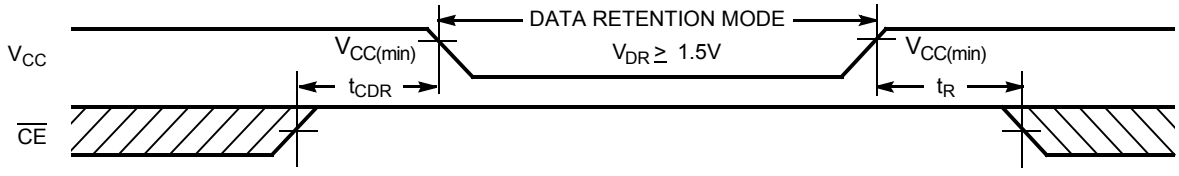


Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions		Min	Typ[3]	Max	Unit
V_{DR}	V_{CC} for Data Retention			1.5			V
I_{CCDR}[7]	Data Retention Current	V_{CC} = 1.5V, $CE_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	Ind'l/Auto-A			3	µA
			Auto-E			30	µA
t_{CDR}[8]	Chip Deselect to Data Retention Time			0			ns
t_R[9]	Operation Recovery Time			t_{RC}			ns

Data Retention Waveform [10]



Notes:
9. Full device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
10. CE is the logical combination of $\overline{CE_1}$ and CE_2. When $\overline{CE_1}$ is LOW and CE_2 is HIGH, CE is LOW; when $\overline{CE_1}$ is HIGH or CE_2 is LOW, CE is HIGH.

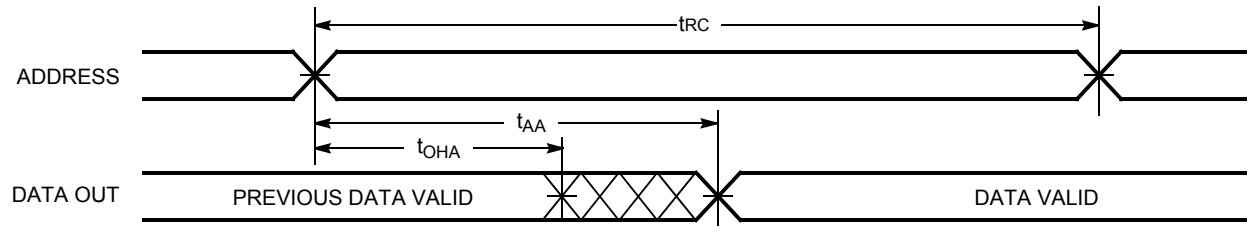
Switching Characteristics (Over the Operating Range)[10, 11]

Parameter	Description	45 ns (Ind'l/Auto-A)		55 ns (Auto-E)		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read Cycle Time	45		55		ns
t_{AA}	Address to Data Valid		45		55	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		22		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[12]	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[12,13]		18		20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[12]	10		10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[12, 13]		18		20	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Up		45		55	ns
Write Cycle[14]						
t_{WC}	Write Cycle Time	45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	35		40		ns
t_{AW}	Address Setup to Write End	35		40		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Setup to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	35		40		ns
t_{SD}	Data Setup to Write End	25		25		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[12, 13]		18		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[12]	10		10		ns

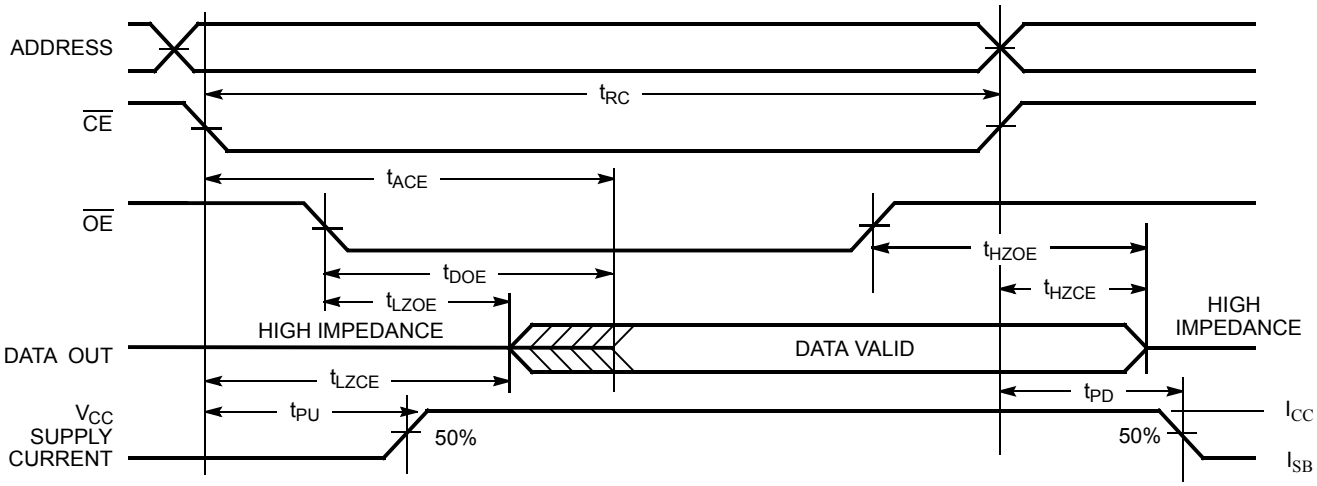
Notes:
11. Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" on page 4.
12. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
13. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the output enter a high impedance state.
14. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

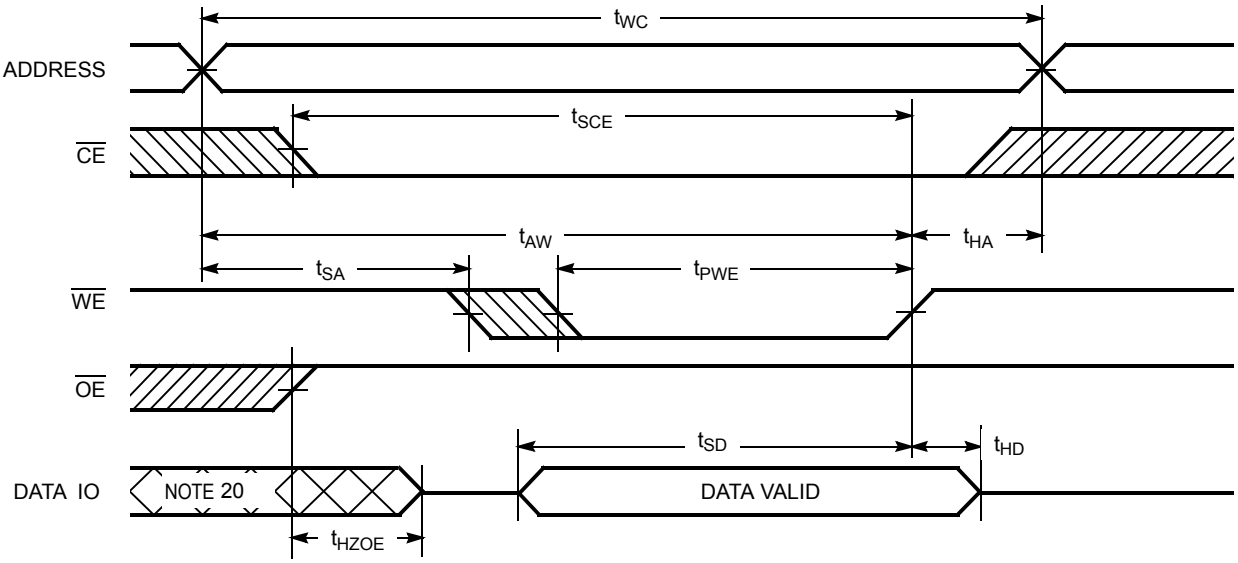
Read Cycle 1 (Address transition controlled) [15, 16]



Read Cycle No. 2 ($\overline{OE}$ controlled) [10, 16, 17]



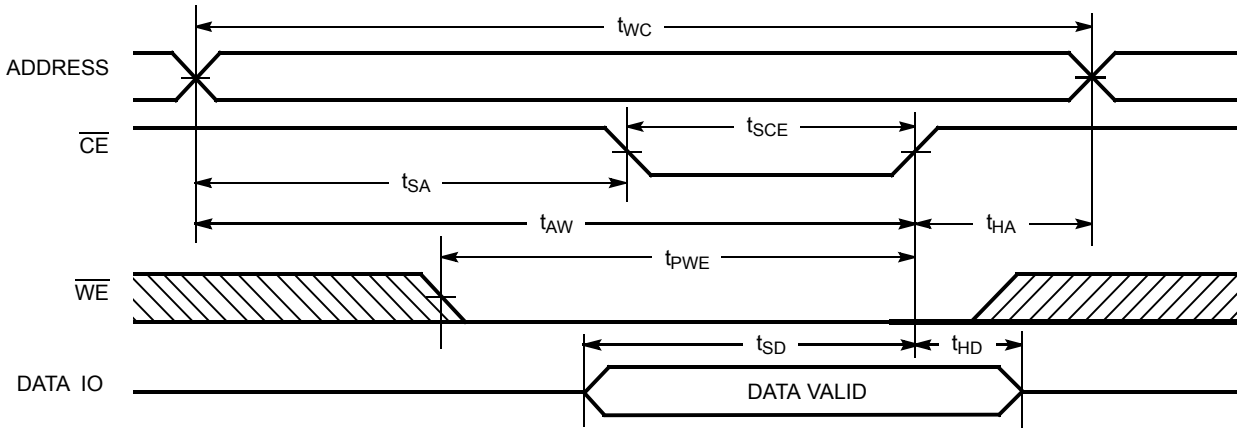
Write Cycle No. 1 ($\overline{WE}$ controlled) [10, 15, 18, 19]



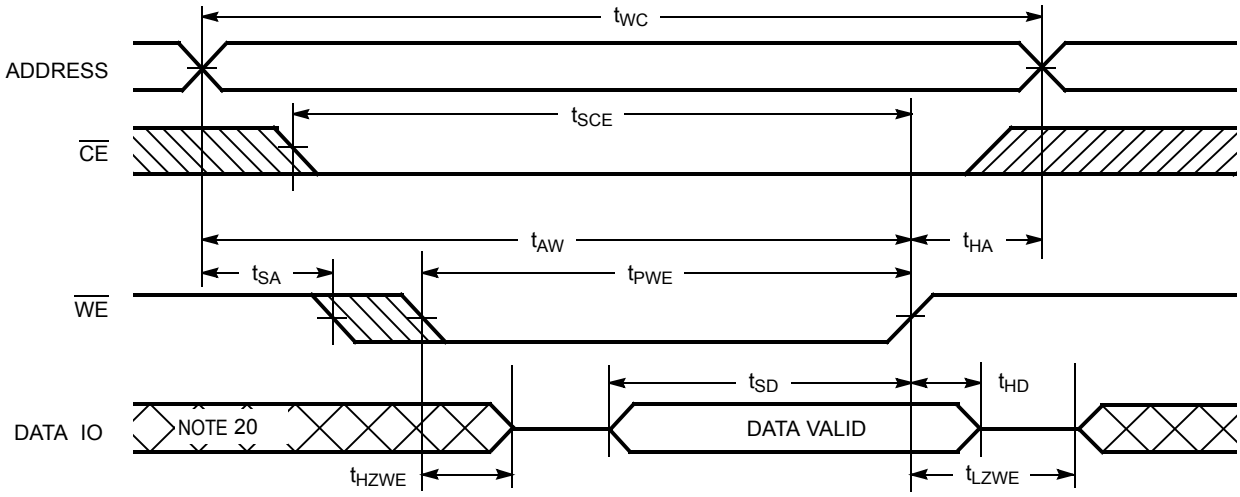
Notes:
15. The device is continuously selected. $\overline{OE}$, $\overline{CE}_1$ = V_{IL}, CE_2 = V_{IH}.
16. $\overline{WE}$ is HIGH for read cycle.
17. Address valid before or similar to $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.
18. Data IO is high impedance if $\overline{OE}$ = V_{IH}.
19. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
20. During this period, the IOs are in output state. Do not apply input signals.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE1}$ or CE2 controlled) [10, 14, 18, 19]



Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) [10, 19]



Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	X	High Z	Deselect/Power Down	Standby (I_{SB})
X	L	X	X	High Z	Deselect/Power Down	Standby (I_{SB})
L	H	H	L	Data Out	Read	Active (I_{CC})
L	H	H	H	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	Data in	Write	Active (I_{CC})

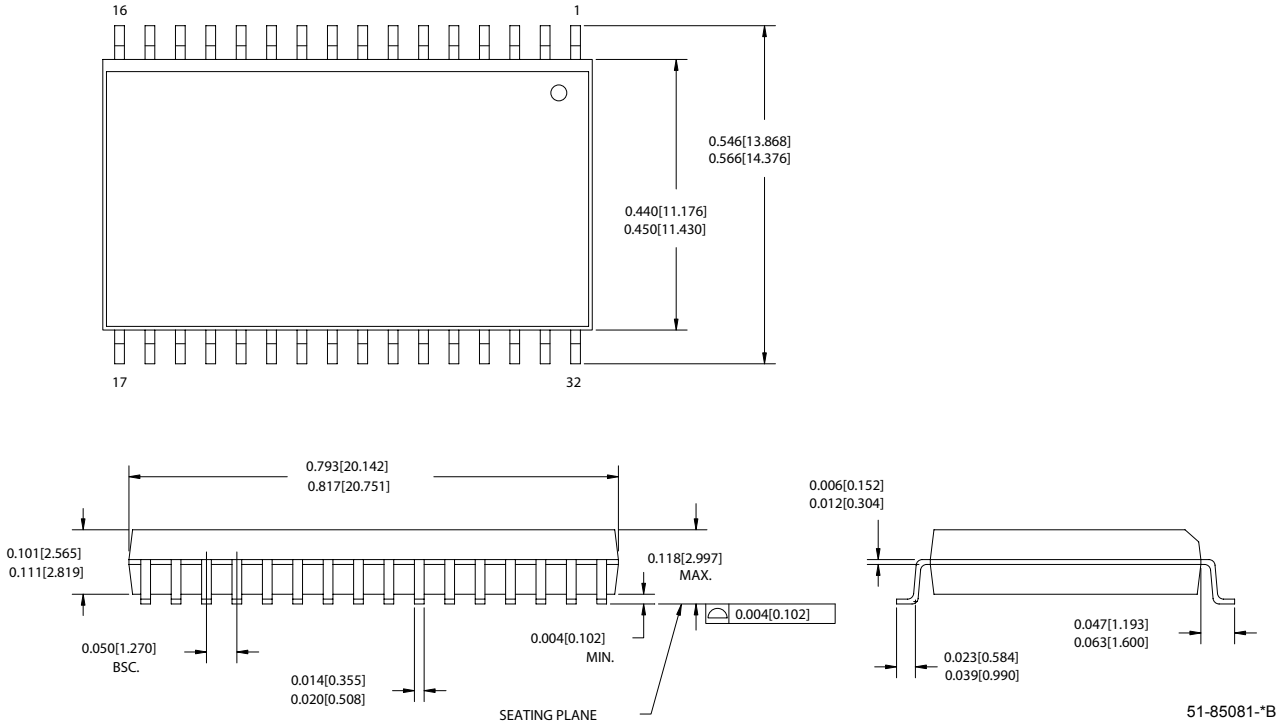
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62128EV30LL-45SXI	51-85081	32-pin 450-Mil SOIC (Pb-free)	Industrial
	CY62128EV30LL-45ZXI	51-85056	32-pin TSOP Type I (Pb-free)	
	CY62128EV30LL-45ZAXI	51-85094	32-pin STSOP (Pb-free)	
45	CY62128EV30LL-45ZXA	51-85056	32-pin TSOP Type I (Pb-free)	Automotive-A
55	CY62128EV30LL-55ZXE	51-85056	32-pin TSOP Type I (Pb-free)	Automotive-E

Contact your local Cypress sales representative for availability of these parts.

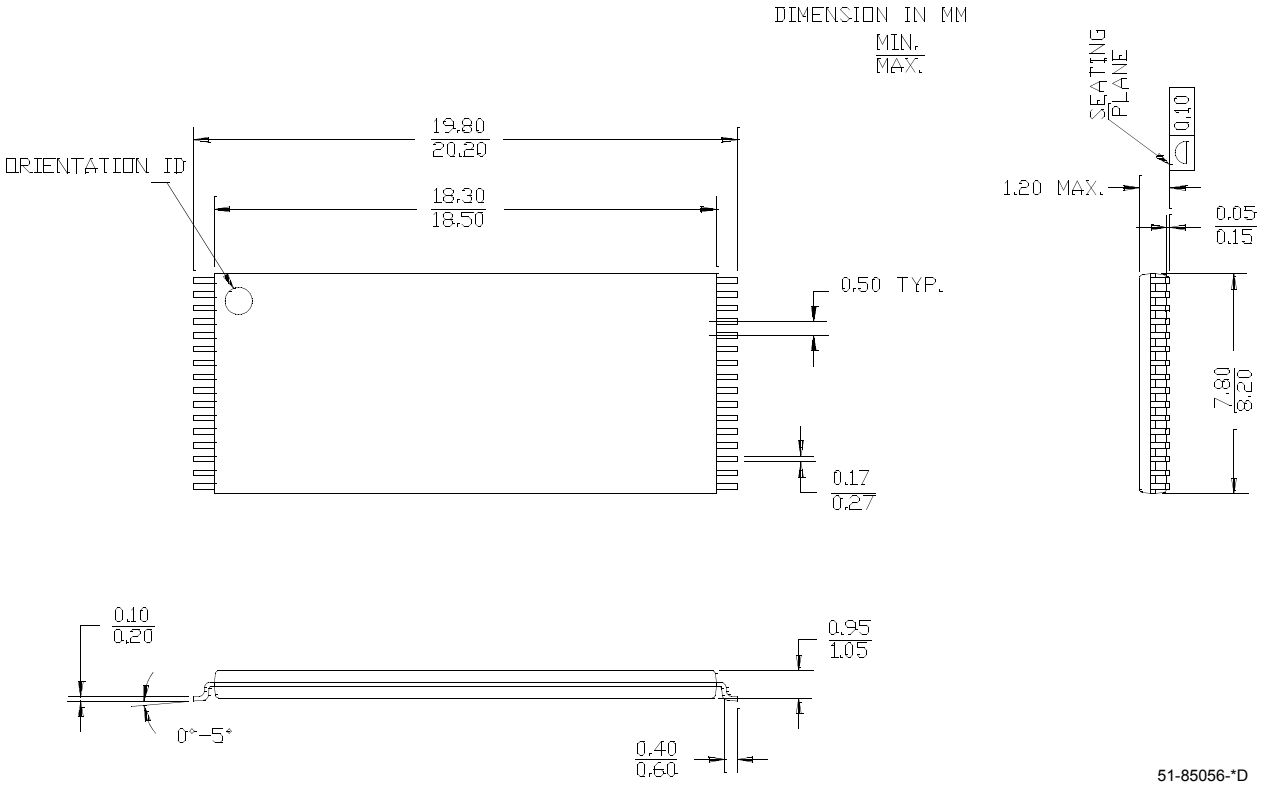
Package Diagrams

Figure 1. 32-Pin (450 Mil) Molded SOIC, 51-85081



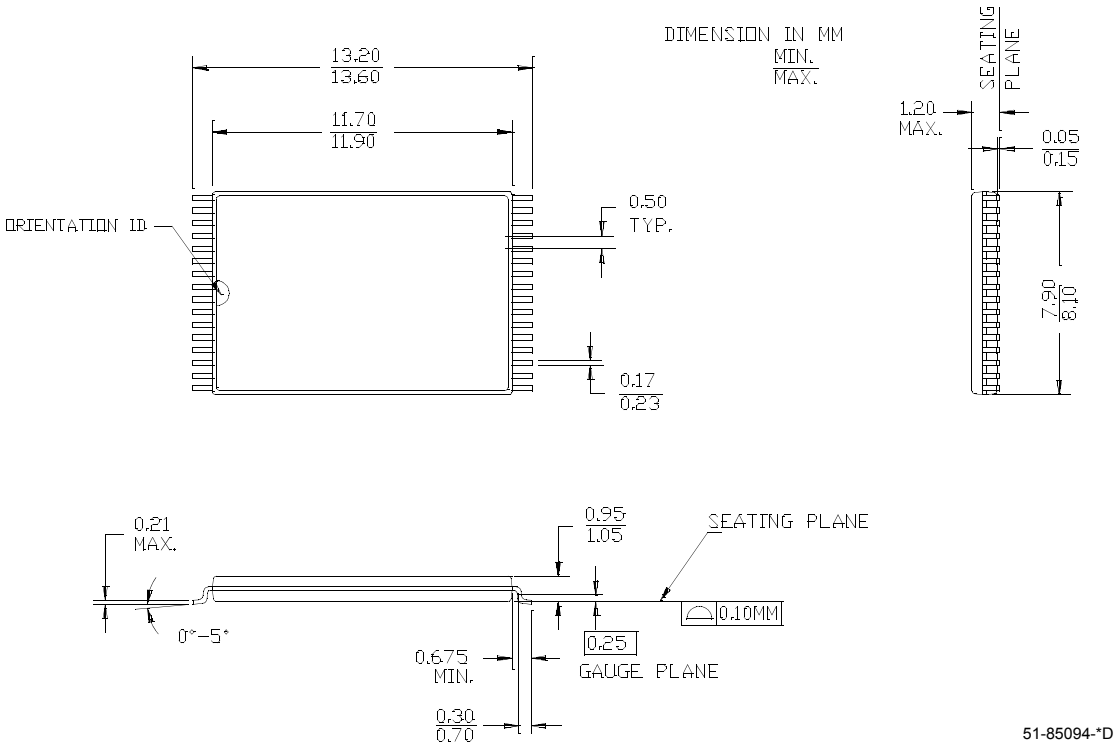
Package Diagrams (continued)

Figure 2. 32-Pin Thin Small Outline Package Type I (8 x 20 mm), 51-85056



Package Diagrams (continued)

Figure 3. 32-Pin Shrunk Thin Small Outline Package (8 x 13.4 mm), 51-85094



Document History Page

Document Title: CY62128EV30 MoBL® 1 Mbit (128K x 8) Static RAM Document Number: 38-05579				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	285473	See ECN	PCI	New Data Sheet
*A	461631	See ECN	NXR	Converted from Preliminary to Final Removed 35 ns Speed Bin Removed “L” version of CY62128EV30 Removed Reverse TSOP I package from Product offering. Changed $I_{CC\ (Typ)}$ from 8 mA to 11 mA and $I_{CC\ (Max)}$ from 12 mA to 16 mA for f = f_{max} Changed $I_{CC\ (max)}$ from 1.5 mA to 2.0 mA for f = 1 MHz Changed $I_{SB2\ (max)}$ from 1 μA to 4 μA Changed $I_{SB2\ (Typ)}$ from 0.5 μA to 1 μA Changed $I_{CCDR\ (max)}$ from 1 μA to 3 μA Changed the AC Test load Capacitance value from 50 pF to 30 pF Changed t_{LZOE} from 3 to 5 ns Changed t_{LZCE} from 6 to 10 ns Changed t_{HZCE} from 22 to 18 ns Changed t_{PWE} from 30 to 35 ns Changed t_{SD} from 22 to 25 ns Changed t_{LZWE} from 6 to 10 ns Updated the Ordering Information table.
*B	464721	See ECN	NXR	Updated the Block Diagram on page # 1
*C	1024520	See ECN	VKN	Added final Automotive-A and Automotive-E information Added footnote #9 related to I_{SB2} and I_{CCDR} Updated Ordering Information table