EPSON

E0C6244

4-bit Single Chip Microcomputer

Wide Voltage Operation Products

- Core CPU Architecture
- Dot Matrix LCD Driver
- Programmable SVD Circuit/Sound Generator

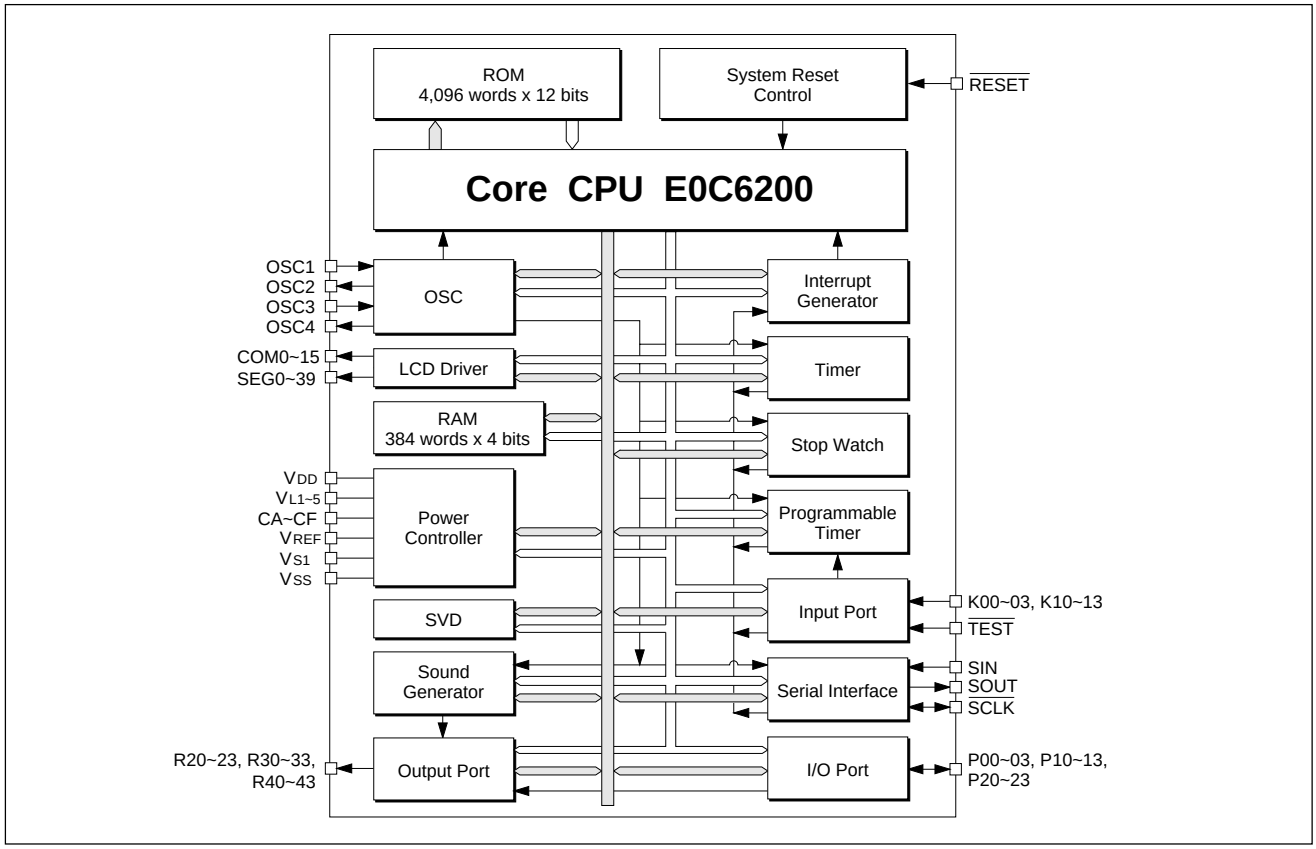
■ DESCRIPTION

The E0C6244 is an advanced single-chip CMOS 4-bit microcomputer consisting of the E0C6200 4-bit core CPU. The chip contains the ROM, RAM, dot matrix LCD driver, programmable SVD circuit, time base counter and clock synchronous serial port.
The E0C6244 is suitable for dot matrix display systems.

■ FEATURES

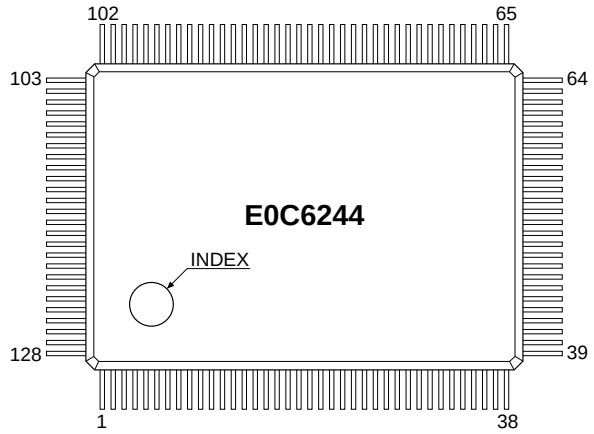
- CMOS LSI 4-bit parallel processing
- Clock ..... 32.768kHz/2MHz (Max.) (selectable by software)
- Instruction set ..... 108 instructions
- Instruction cycle time ..... 153µsec, 214µsec or 366µsec at 32kHz (depending on instruction)
  2µsec, 3µsec or 6µsec at 2MHz (depending on instruction)
- ROM capacity ..... 4,096 × 12 bits
- RAM capacity ..... 384 × 4 bits
- Input port ..... 8 bits (pull-up resistors are available by mask option)
- Output port ..... 12 bits (clock output or buzzer output is available by mask option)
- I/O port ..... 12 bits (pull-up resistors are available by mask option)
- Serial I/O port ..... 1 port (clock sync.)
- Dot matrix LCD driver ..... 40 segments × 8 commons/40 segments × 16 commons (1/8 or 1/16 duty is selectable by mask option)
- Built-in SVD circuit ..... Programmable
- Built-in stopwatch timer
- Built-in watchdog timer
- Built-in time base counter ..... 3 lines
- Interrupts ..... External : Input interrupt 2 lines
  Internal : Timer interrupt 3 lines
  Serial I/O interrupt 1 line
- Built-in sound generator ..... With digital envelope (8 sounds programmable)
- Supply voltage ..... 2.2V to 5.5V
- Current consumption ..... HALT mode (32kHz) : 2.5µA (Typ.)
  OPERATING mode (1MHz) : 400µA (Typ.)
- Package ..... QFP5-128pin-S1 (plastic)
  Die form

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

QFP5-128pin



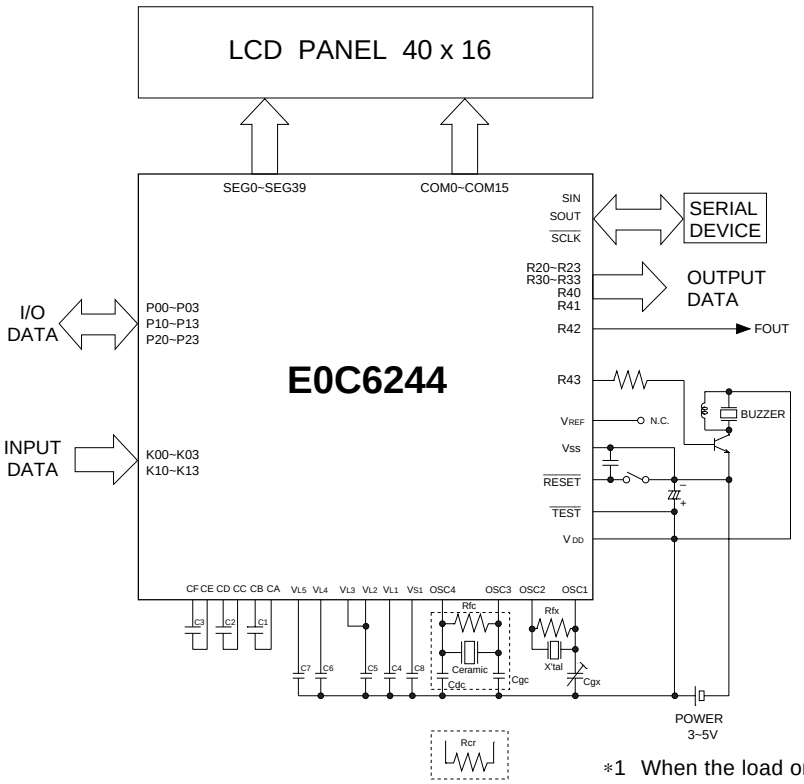
No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	N.C.	33	SEG30	65	SEG1	97	R40
2	CC	34	SEG29	66	N.C.	98	N.C.
3	N.C.	35	N.C.	67	SEG0	99	N.C.
4	CB	36	SEG28	68	N.C.	100	N.C.
5	CA	37	N.C.	69	N.C.	101	R33
6	N.C.	38	SEG27	70	$\overline{SCLK}$	102	R32
7	COM0	39	N.C.	71	SOUT	103	R31
8	COM1	40	SEG26	72	SIN	104	R30
9	COM2	41	SEG25	73	K13	105	R23
10	COM3	42	SEG24	74	K12	106	R22
11	COM4	43	SEG23	75	K11	107	R21
12	COM5	44	SEG22	76	K10	108	R20
13	COM6	45	SEG21	77	K03	109	V_{SS}
14	COM7	46	SEG20	78	K02	110	$\overline{RESET}$
15	COM8	47	SEG19	79	K01	111	$\overline{TEST}$
16	COM9	48	SEG18	80	K00	112	OSC4
17	COM10	49	SEG17	81	P23	113	OSC3
18	COM11	50	SEG16	82	P22	114	N.C.
19	COM12	51	SEG15	83	P21	115	V_{S1}
20	COM13	52	SEG14	84	P20	116	OSC2
21	COM14	53	SEG13	85	P13	117	OSC1
22	COM15	54	SEG12	86	P12	118	N.C.
23	N.C.	55	SEG11	87	P11	119	V_{DD}
24	SEG39	56	SEG10	88	P10	120	V_{REF}
25	SEG38	57	SEG9	89	P03	121	V_{L1}
26	SEG37	58	SEG8	90	P02	122	V_{L2}
27	SEG36	59	SEG7	91	P01	123	V_{L3}
28	SEG35	60	SEG6	92	P00	124	V_{L4}
29	SEG34	61	SEG5	93	R43	125	V_{L5}
30	SEG33	62	SEG4	94	R42	126	CF
31	SEG32	63	SEG3	95	N.C.	127	CE
32	SEG31	64	SEG2	96	R41	128	CD

N.C. = No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V_{DD}	119	I	Power source (+) terminal
V_{SS}	109	I	Power source (-) terminal
V_{S1}	115	–	Oscillation and internal logic system regulated voltage
V_{L1}–V_{L5}	121–125	–	LCD system power (1/4 or 1/5 bias may be selected by mask option)
V_{REF}	120	O	LCD system power test terminal
CA–CF	5, 4, 2, 128–126	–	Booster capacitor connecting terminal
OSC1	117	I	Crystal or CR oscillation input terminal (selected by mask option)
OSC2	116	O	Crystal or CR oscillation output terminal (selected by mask option)
OSC3	113	I	Ceramic or CR oscillation input terminal (selected by mask option)
OSC4	112	O	Ceramic or CR oscillation output terminal (selected by mask option)
K00–K03, K10–K13	80–73	I	Input terminal (Use of pull up resistor is selected by mask option)
P00–P03, P10–P13 P20–P23	92–81	I/O	I/O terminal
R20–R23, R30–R32	108–102	O	Output terminal
R33	101	O	Output terminal (DC or $\overline{SRDY}$ output may be selected by mask option)
R40	97	O	Output terminal (DC, CL or $\overline{FOUT}$ output may be selected by mask option)
R41	96	O	Output terminal (DC or FR output may be selected by mask option)
R42	94	O	Output terminal (DC, $\overline{BZ}$ or FOUT output may be selected by mask option)
R43	93	O	Output terminal (DC or BZ output may be selected by mask option)
SIN	72	I	Serial interface input terminal
SOUT	71	O	Serial interface output terminal
$\overline{SCLK}$	70	I/O	Serial interface clock input/output terminal
SEG0–39	67, 65–40, 38 36, 34–24	O	LCD segment output terminal
COM0–15	7–22	O	LCD common output terminal
$\overline{RESET}$	110	I	Initial reset input terminal
$\overline{TEST}$	111	I	Test input terminal

■ BASIC EXTERNAL CONNECTION DIAGRAM



X'tal	Crystal oscillator	32.768kHz CI(Max.)=35kΩ
Rfx	Feedback resistor	10MΩ
Cgx	Trimmer capacitor	5~25pF
Ceramic	Ceramic oscillator	500kHz~2MHz
Rfc	Feedback resistor	1MΩ
Cgc	Gate capacitance	100pF
Cdc	Drein capacitance	100pF
Rcr	Resistance for CR oscillation	20kΩ~100kΩ
C1~C3	Voltage booster capacitor (1)~(3)	0.1µF ∗1
C4	Capacitor between V_{DD} and V_{L1}	0.1µF ∗1
C5	Capacitor between V_{DD} and V_{L2}	0.1µF ∗1
C6	Capacitor between V_{DD} and V_{L4}	0.1µF ∗1
C7	Capacitor between V_{DD} and V_{L5}	0.1µF ∗1
C8	Capacitor between V_{DD} and V_{S1}	0.1µF

∗1 When the load on the liquid crystal system is large, increase the capacitance of the voltage booster capacitors (C1–C3) and the capacitors between V_{DD} and liquid crystal system power (C4–C7).

Note: The above table is simply an example, and is not guaranteed to work.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{SS}	-7.0 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1} - 0.3 to 0.5	V
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *1	P_D	250	mW

*1: In case of plastic package (QFP5-128pin).

● Recommended Operating Conditions

(Ta=-20 to 70°C)

Condition	Symbol	Remark		Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	VSC="0"	-3.8	-3.0	-1.8	V
			VSC="1"	-5.5	-3.0	-2.2	V
			VSC="2"	-5.5	-3.0	-3.5	V
Oscillation frequency (1)	f_{OSC1}			20	32.768	50	kHz
Oscillation frequency (2)	f_{OSC3}	VSC="1"		50	1,000	1,200	kHz
Oscillation frequency (3)	f_{OSC3}	VSC="2"		50	2,000	2,300	kHz
Voltage booster capacitor (1)	C1				0.1		µF
Voltage booster capacitor (2)	C2				0.1		µF
Voltage booster capacitor (3)	C3				0.1		µF
Capacitor between V_{DD} and V_{L1}	C4				0.1		µF
Capacitor between V_{DD} and V_{L2}	C5				0.1		µF
Capacitor between V_{DD} and V_{L4}	C6				0.1		µF
Capacitor between V_{DD} and V_{L5}	C7				0.1		µF
Capacitor between V_{DD} and V_{S1}	C8				0.1		µF

● DC Characteristics

(Unless otherwise specified: V_{DD}=0V,V_{SS}=-3.0V,V_{L1}=-1.0V,V_{L2}=-2.0V,V_{L4}=-3.0V,V_{L5}=-4.0V,f_{OSC1}=32.768kHz,f_{OSC3}=1MHz,Ta=25°C,C1–C8=0.047µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage	V_{HIN}	V_{SS}=-2.2 to -5.5V	K00–03•10–13, P00–03•10–13	0.2•V_{SS}		0	V
Low level input voltage	V_{LIN}	Ta=25°C	P20–P23, SIN, $\overline{SCLK}$	V_{SS}		0.8•V_{SS}	V
High level input voltage	V_{HIN}	V_{SS}=-2.2 to -5.5V	$\overline{RESET}$	-0.2		0	V
Low level input voltage	V_{LIN}	Ta=25°C		V_{SS}		V_{SS}+0.2	V
High level input current	I_{IH}	V_{SS}=-3.0V V_{IH}=0V	K00–03•10–13, P00–03•10–13 P20–P23, SIN, $\overline{SCLK}$ $\overline{RESET}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{SS}=-3.0V V_{IL1}=V_{SS} With pull-up resistor	K00–03•10–13, P00–03•10–13 P20–P23, SIN, $\overline{SCLK}$ $\overline{RESET}$	-45		-15	µA
Low level input current (2)	I_{IL2}	V_{SS}=-3.0V V_{IL2}=V_{SS} No pull-up resistor	K00–03•10–13, P00–03•10–13 P20–P23, SIN, $\overline{SCLK}$ $\overline{RESET}$	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{SS}=-2.2V V_{OH1}=-0.5V	P00–03•10–13•20–23 R20–23•30–33 R40•41, SOUT, $\overline{SCLK}$			-1.0	mA
Low level output current (1)	I_{OL1}	V_{SS}=-2.2V V_{OL1}=V_{SS}+0.5V	P00–03•10–13•20–23 R20–23•30–33 R40•41, SOUT, $\overline{SCLK}$	4.0			mA
High level output current (2)	I_{OH2}	V_{SS}=-2.2V V_{OH2}=-0.5V	R42•43			-2.0	mA
Low level output current (2)	I_{OL2}	V_{SS}=-2.2V V_{OL1}=V_{SS}+0.5V	R42•43	8.0			mA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–15			-30	µA
	I_{OL3}	V_{OL3}=V_{L5}+0.05V		30			µA
Segment output current	I_{OH4}	V_{OH4}=-0.05V	SEG0–39			-10	µA
	I_{OL4}	V_{OL4}=V_{L5}+0.05V		10			µA

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V_{DD}=0V,V_{SS}=-3.0V,V_{L1}=-1.0V,V_{L2}=-2.0V,V_{L4}=-3.0V,V_{L5}=-4.0V,f_{OSC1}=32.768kHz,f_{OSC3}=1MHz,Ta=25°C,C1–C8=0.047µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Liquid crystal drive voltage (Normal mode)	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (No panel load)		1/2•V_{L2} -0.1		1/2•V_{L2} ×0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (No panel load)	LC="0"		-1.80		
			LC="1"		-1.85		
			LC="2"		-1.90		
			LC="3"		-1.95		
			LC="4"		-2.01		
			LC="5"		-2.06		
			LC="6"		-2.11		
			LC="7"	Typ.×1.12	-2.17	Typ.×0.88	V
			LC="8"		-2.22		
			LC="9"		-2.27		
			LC="10"		-2.32		
			LC="11"		-2.38		
			LC="12"		-2.43		
			LC="13"		-2.48		
			LC="14"		-2.53		
			LC="15"		-2.59		
	V_{L4}	Connect 1MΩ load resistor between V_{DD} and V_{L4} (No panel load)		3/2•V_{L2}		3/2•V_{L2} ×0.95	V
	V_{L5}	Connect 1MΩ load resistor between V_{DD} and V_{L5} (No panel load)		2•V_{L2}		2•V_{L2} ×0.95	V
Liquid crystal drive voltage (Heavy load protection mode)	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (No panel load)	LC="0"		-0.92		
			LC="1"		-0.95		
			LC="2"		-0.97		
			LC="3"		-1.00		
			LC="4"		-1.03		
			LC="5"		-1.05		
			LC="6"		-1.08		
			LC="7"	Typ.×1.12	-1.11	Typ.×0.88	V
			LC="8"		-1.13		
			LC="9"		-1.16		
			LC="10"		-1.18		
			LC="11"		-1.21		
			LC="12"		-1.24		
			LC="13"		-1.26		
			LC="14"		-1.29		
			LC="15"		-1.32		
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (No panel load)		2•V_{L1}		2•V_{L1} ×0.90	V
	V_{L4}	Connect 1MΩ load resistor between V_{DD} and V_{L4} (No panel load)		3•V_{L1}		3•V_{L1} ×0.90	V
	V_{L5}	Connect 1MΩ load resistor between V_{DD} and V_{L5} (No panel load)		4•V_{L1}		4•V_{L1} ×0.90	V
SVD voltage	V_{SVD0}	SVC="0"		-2.35	-2.20	-2.05	V
	V_{SVD1}	SVC="1"		-2.70	-2.50	-2.30	V
	V_{SVD2}	SVC="2"		-3.30	-3.10	-2.90	V
	V_{SVD3}	SVC="3"		-4.50	-4.20	-3.90	V
SVD circuit response time	t_{SVD}					100	µS
Current consumption	I_{HLT}	During HALT	No panel load *1		2.5	5.0	µA
	I_{EX1}	During operation at 32kHz			6.5	9.0	µA
	I_{EX2}	During operation at 1MHz	No panel load *2		400	600	µA
	I_{EX3}	During operation at 2MHz	No panel load *3		1,000	1,500	µA
Current consumption (OSC1•CR oscillation)	I_{HLT}	During HALT	No panel load *4		20	70	µA
	I_{EX1}	During operation at f_{OSC1}			25	80	µA
	I_{EX2}	During operation at 1MHz			420	600	µA
	I_{EX3}	During operation at 2MHz	No panel load *5		1,000	1,500	µA

*1: SVD circuit: OFF status, VSC = "0", OSC1: oscillating with crystal, OSCC= "0"
*2: SVD circuit: OFF status, VSC = "1", OSC1: oscillating with crystal
*3: SVD circuit: OFF status, VSC = "2", OSC1: oscillating with crystal, V_{SS} = -5.0V
*4: SVD circuit: OFF status, VSC = "0" or "1", OSC1: oscillating with CR, OSCC = "0", R_{OSC} for OSC1 = 1.6MΩ
*5: SVD circuit: OFF status, VSC = "2", OSC1: oscillating with CR, OSCC = "0", R_{OSC} for OSC1 = 1.6MΩ

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (C_I=35kΩ), C_{GX}=25pF, C_{DX}=built-in, R_{fX}=10MΩ, VSC="0", Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			5	Sec
Built-in capacitance (drain)	C_D	Package as assembled		22		pF
		Bare chip		21		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -5.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF			-5.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{S1}	200			MΩ

OSC1 CR oscillation circuit

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, VSC="0" or "1", Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			3	mS
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -5.5V	-5		5	%
Oscillation frequency	f_{CR}	R_{OSC}=1.6MΩ	32×70%	32	32×130%	kHz

OSC3 CR oscillation circuit (1)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, VSC="1", Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			3	mS
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -5.5V	-5		5	%
Oscillation frequency	f_{CR}	R_{OSC}=40kΩ	860×70%	860	860×130%	kHz

OSC3 CR oscillation circuit (2)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-5.0V, VSC="2", Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-3.5 to -5.5V			3	mS
Frequency/voltage deviation	∂f/∂V	V_{SS}=-3.5 to -5.5V	-5		5	%
Oscillation frequency	f_{CR}	R_{OSC}=20kΩ	1.7×70%	1.7	1.7×130%	MHz

OSC3 ceramic oscillation circuit (1)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, VSC="1", Ceramic: CSB 1000J (Murata Mfg. Co.), C_{GC}=C_{DC}=100pF, R_{fC}=1MΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			3	mS
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -5.5V	-3		3	%

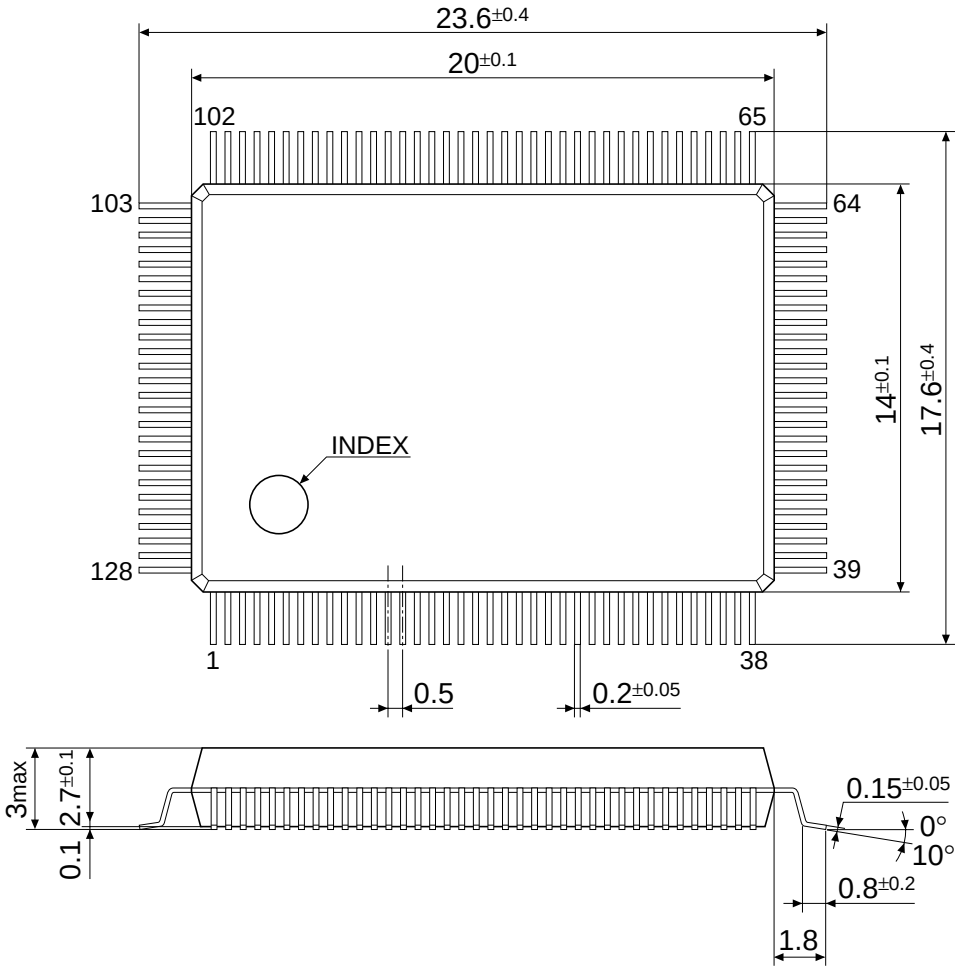
OSC3 ceramic oscillation circuit (2)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-5.0V, VSC="2", Ceramic: CSA 2.00MG (Murata Mfg. Co.), C_{GC}=C_{DC}=100pF, R_{fC}=1MΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-3.5 to -5.5V			3	mS
Frequency/voltage deviation	∂f/∂V	V_{SS}=-3.5 to -5.5V	-3		3	%

■ PACKAGE DIMENSIONS

Plastic QFP5-128pin



Unit: mm

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