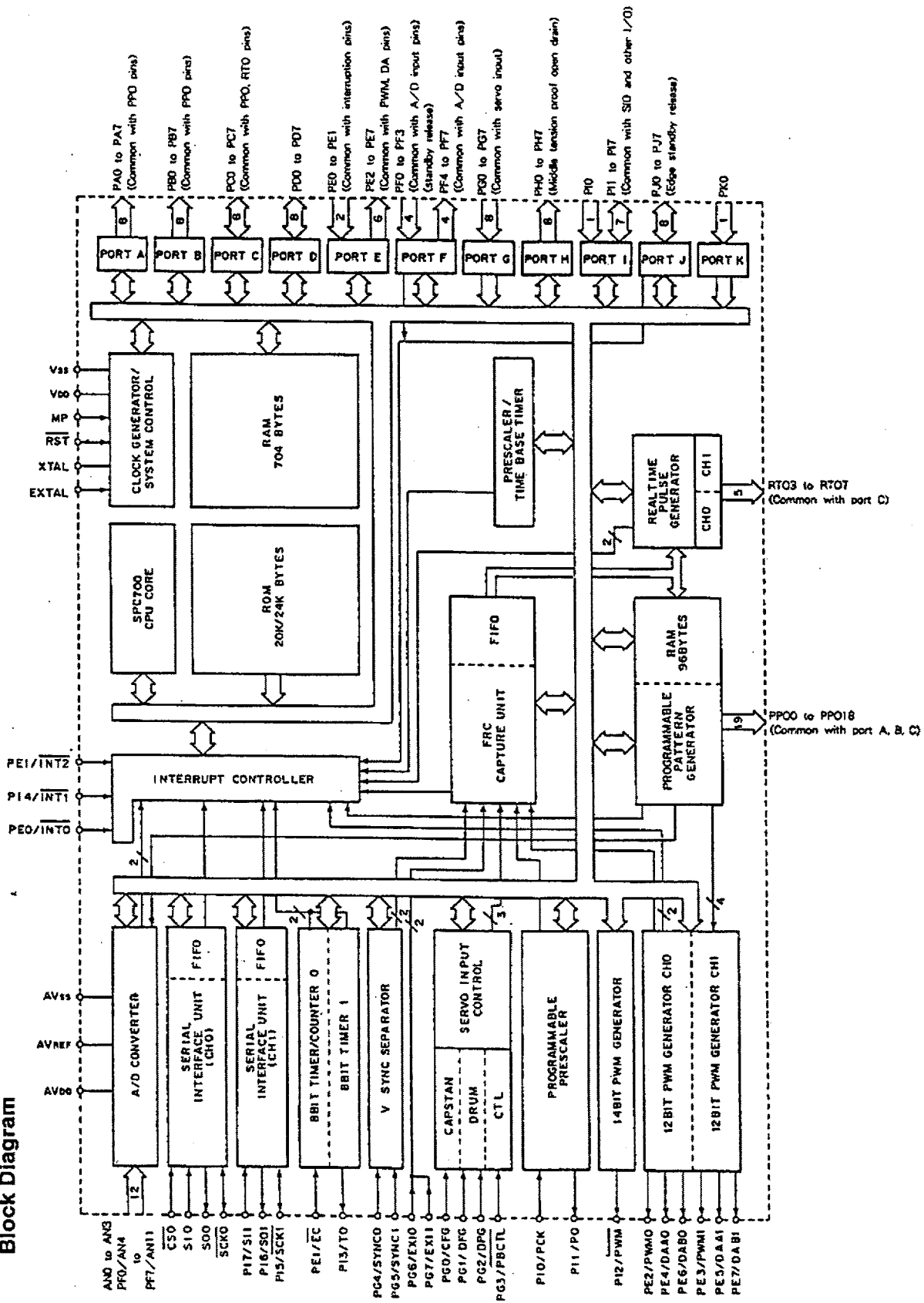


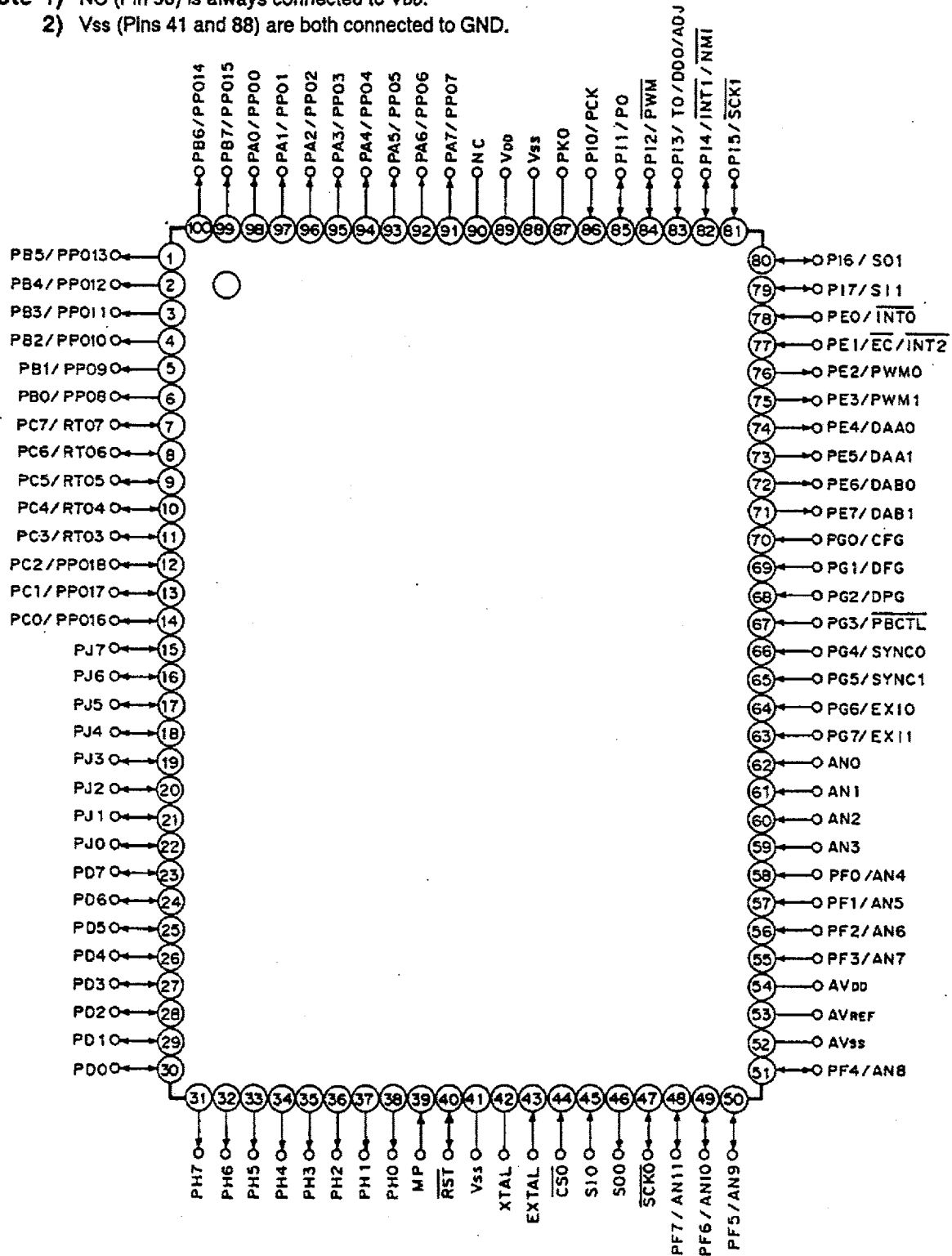


Block Diagram



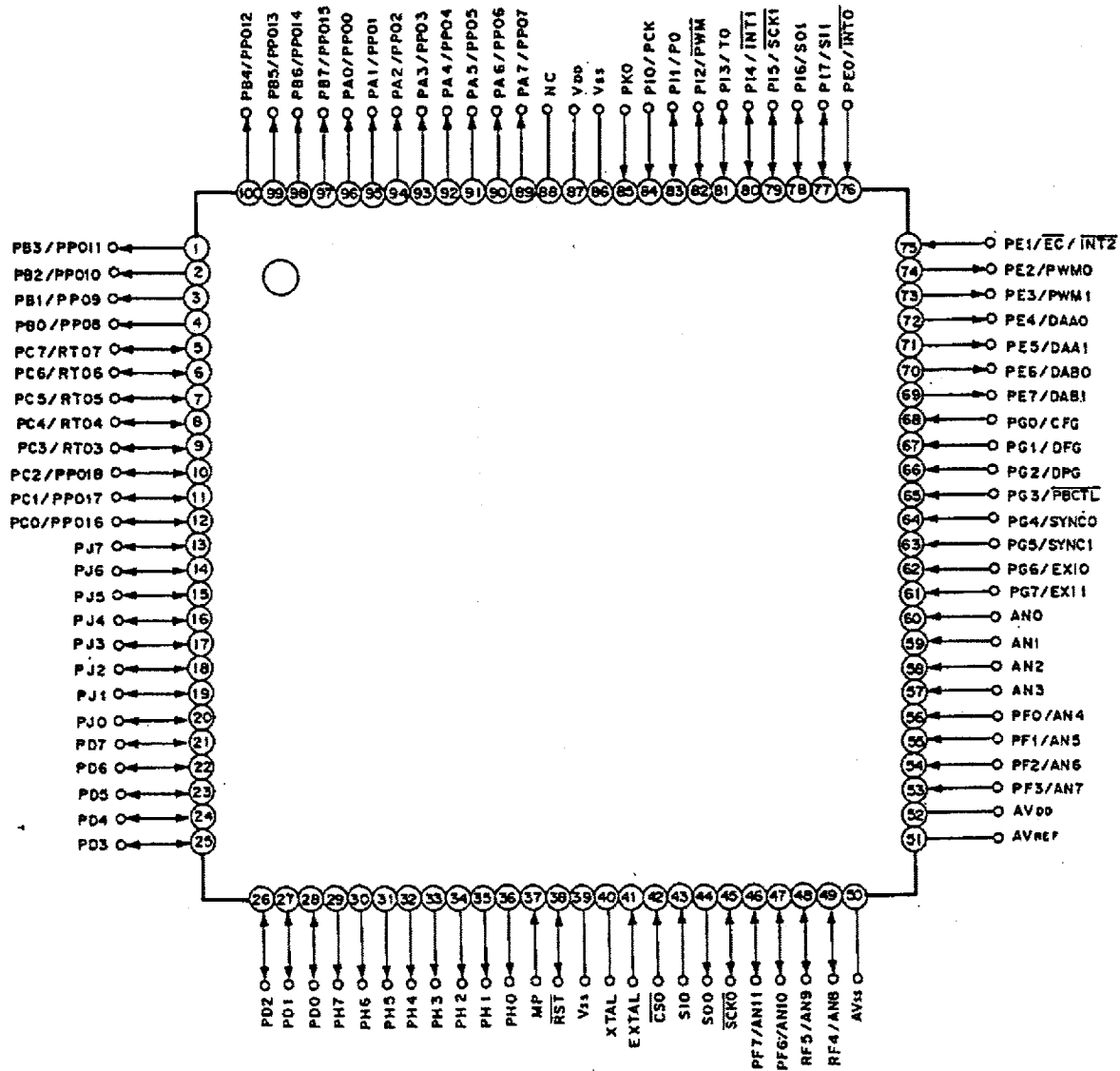
Pin Configuration 1 (Top View) 100 pin QFP Package

- Note 1) NC (Pin 90) is always connected to V<sub>DD</sub>.  
 2) V<sub>SS</sub> (Pins 41 and 88) are both connected to GND.



Pin Configuration 2 (Top View) 100 pin VQFP Package

- Note 1) NC (Pin 88) is always connected to V<sub>DD</sub>.  
 2) V<sub>SS</sub> (Pins 39 and 86) are both connected to GND.



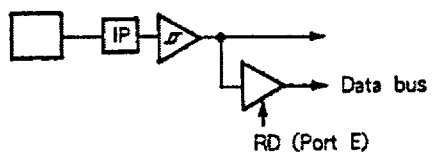
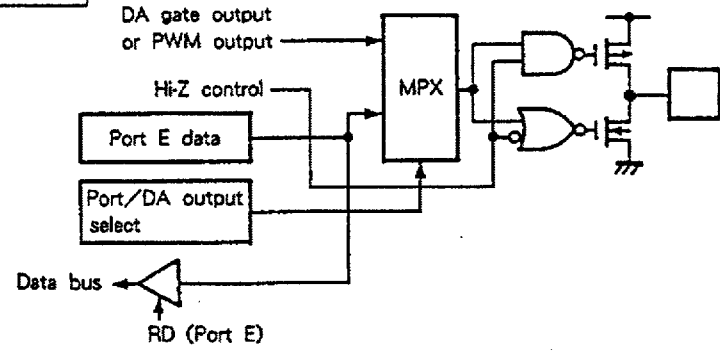
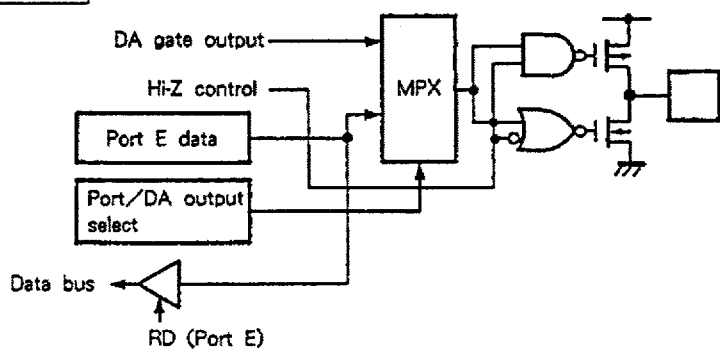
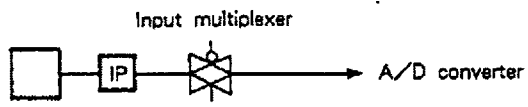
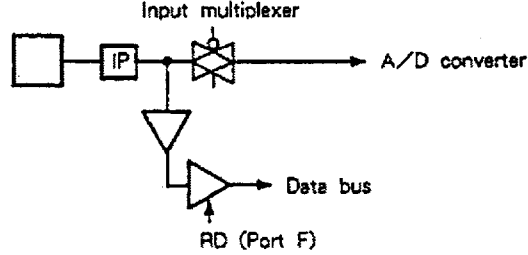
## Pin Description

Symbol	I/O	Description		
PA0/PPO0 to PA7/PPO7	Output/ Real time Output	(Port A) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG) output. Functions as high precision real time pulse output port. (19 pins)	
PB0/PPO8 to PB7/PPO15	Output/ Real time Output	(Port B) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)		
PC0/PPO16 to PC2/PPO18	I/O/ Real time Output	(Port C) 8-bit input/output port, enables to specify input/output by bit unit. Data is gated with PPO or RTO contents by OR-gate and they are output. (8 pins)		
PC3/RTO3 to PC7/RTO7	I/O/ Real time Output		Real time pulse generator (RTG) output. Functions as high precision real time pulse output port. (5 pins)	
PD0 to PD7	I/O	(Port D) 8-bit input/output port. Enable to specify input/output by 4-bit unit. Enables to drive 12mA sink current. (8 pins)		
PE0/INT0	Input	(Port E) 8-bit port. Lower 2 bits are input pins and upper 6 bits are output pins. (8 pins)	Input pin to request external interruption. Active when falling edge.	
PE1/EC/INT2	Input		External event input pin for timer/counter.	Input pin to request external interruption. Active when falling edge.
PE2/PWM0	Output		PWM output pins. (2 pins)	
PE3/PWM1	Output			
PE4/DAA0	Output			
PE5/DAA1	Output			
PE6/DAB0	Output		DA gate pulse output pins. (4 pins)	
PE7/DAB1	Output			
AN0 to AN3	Input	Analog input pins to A/D converter. (12 pins)		
PF0/AN4 to PF3/AN7	Input	(Port F) Lower 4 bits are input port and upper 4 bits are output port. Lower 4 bits also serve as standby release input pin. (8 pins)		
PF4/AN8 to PF7/AN11	Output/Input			
SCK0	I/O	Serial clock (CH0) input/output pin.		
SO0	Output	Serial data (CH0) output pin.		

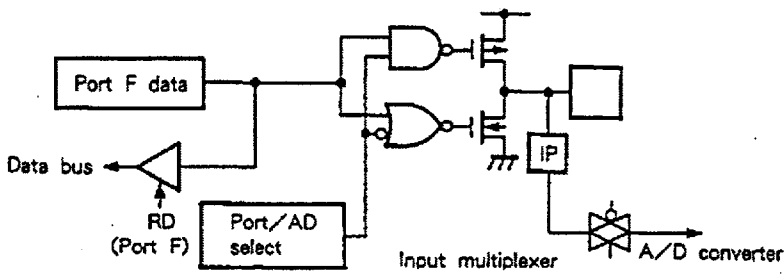
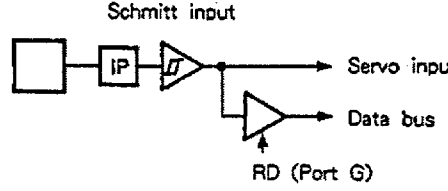
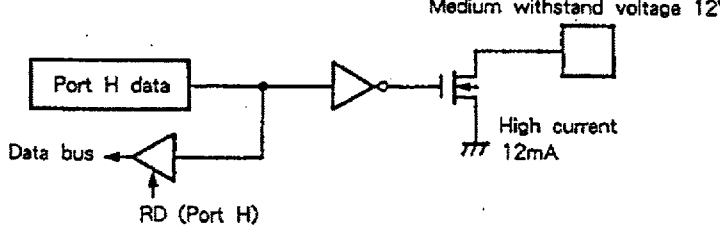
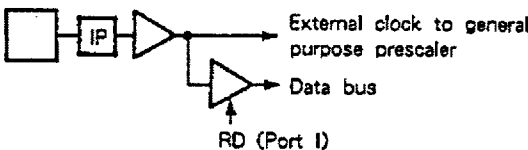
Symbol	I/O	Description	
SIO	Input	Serial data (CH0) input pin.	
$\overline{CS0}$	Input	Serial chip select (CH0) input pin.	
PG0/CFG	Input	(Port G) 8-bit input port. (8 pins)	Capstan FG input pin.
PG1/DFG	Input		Drum FG input pin.
PG2/DPG	Input		Drum PG input pin.
PG3/PBCTL	Input		Playback CTL pulse input pin.
PG4/SYNC0	Input		Composite sync signal input pin.
PG5/SYNC1	Input		
PG6/EXI0	Input		External input pin to FRC capture unit.
PG7/EXI1	Input		
PH0 to PH7	Output	(Port H) 8-bit output port ; Medium withstand voltage (12V) and high current (12mA), N-ch open drain output. (8 pins)	
PI0/PCK	Input	(Port I) Lower 1 bit is input port and upper 7 bits are input/output port. Input/output port can be specified by bit unit (8 pins).	External clock input pin of general purpose prescaler.
PI1/PO	I/O / Output		General purpose prescaler output pin.
PI2/PWM	I/O / Output		14-bit PWM output pin
PI3/TO	I/O / Output		Timer/counter output pin. (duty=50%)
PI4/ $\overline{INT1}$	I/O / Input		Input pin to request external interruption. Active when falling edge.
PI5/SCKT	I/O / I/O		Serial clock (CH1) input/output pin.
PI6/SO1	I/O / Output		Serial data (CH1) output pin.
PI7/SI1	I/O / Input		Serial data (CH1) input pin.
PJ0 to PJ7	I/O	(Port J) 8-bit input /output port. Function as standby release input can be specified by bit unit. Input/output can be specified by bit unit.	
PK0	Input	Input port	
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
RST	I/O	System reset pin of active "L" level. RST pin is input/output pin, which output "L" level by incorporated power on reset function when power on. (Mask option)	
MP	Input	Microprocessor mode input pin. Always connect to GND.	
AVDD		Positive power supply pin of A/D converter.	
AVREF	Input	Reference voltage input pin of A/D converter.	
AVSS		GND pin of A/D converter.	
VDD		Positive power supply pin.	
VSS		GND pin. Connect both VSS pins to GND.	

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
<p>Port A Port B</p> <p>PA0/PPO0 to PA7/PPO7 PB0/PPO8 to PB7/PPO15</p> <p>16 pins</p>	<p>PPO data</p> <p>Port A or Port B</p> <p>Data bus</p> <p>RD</p> <p>Output becomes active from high impedance by data writing to port register.</p>	<p>Hi-Z</p>
<p>Port C</p> <p>PC0/PPO16 to PC2/PPO18 PC3/RTO3 to PC7/RTO7</p> <p>8 pins</p>	<p>PPO, RTO data</p> <p>Port C data</p> <p>Port C direction</p> <p>Data bus</p> <p>RD (Port C)</p> <p>Input protection circuit</p> <p>(Every bit)</p> <p>IP</p>	<p>Hi-Z</p>
<p>Port D</p> <p>PD0 to PD7</p> <p>8 pins</p>	<p>Port D data</p> <p>Port D direction</p> <p>Data bus</p> <p>RD (Port D)</p> <p>High current 12mA</p> <p>(Every 4 bits) (PD0 to 3) (PD4 to 7)</p> <p>IP</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
PE0/INT0 PE1/EC/INT2  2 pins	Port E Schmitt input 	Hi-Z
PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1  4 pins	Port E DA gate output or PWM output Hi-Z control Port E data Port/DA output select Data bus RD (Port E) 	Hi-Z
PE6/DAB0 PE7/DAB1  2 pins	Port E DA gate output Hi-Z control Port E data Port/DA output select Data bus RD (Port E) 	H level
AN0 to AN3  4 pins	Input multiplexer A/D converter 	Hi-Z
PF0/AN4 to PF3/AN7  4 pins	Port F Input multiplexer A/D converter Data bus RD (Port F) 	Hi-Z



Pin	Circuit format	When reset
<p>PF4/AN8 to PF7/AN11</p> <p>4 pins</p>	<p>Port F</p>  <p>Port F data</p> <p>Data bus</p> <p>RD (Port F)</p> <p>Port/AD select</p> <p>Input multiplexer</p> <p>A/D converter</p>	<p>Hi-Z</p>
<p>PG0/CFG PG1/DFG PG2/DPG PG3/PBCTL PG4/SYNC0 PG5/SYNC1 PG6/EXI0 PG7/EXI1</p> <p>8 pins</p>	<p>Port G</p>  <p>Schmitt input</p> <p>IP</p> <p>Servo input</p> <p>Data bus</p> <p>RD (Port G)</p> <p>Note) For PG4/SYNC0, PG5/SYNC1, CMOS schmitt input and TTL schmitt input can be selected with the mask option.</p>	<p>Hi-Z</p>
<p>PH0 to PH7</p> <p>8 pins</p>	<p>Port H</p>  <p>Port H data</p> <p>Data bus</p> <p>RD (Port H)</p> <p>Medium withstand voltage 12V</p> <p>High current 12mA</p>	<p>Hi-Z</p>
<p>PI0/PCK</p> <p>1 pin</p>	<p>Port I</p>  <p>IP</p> <p>External clock to general purpose prescaler</p> <p>Data bus</p> <p>RD (Port I)</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PI1/PO PI2/PWM PI3/TO</p> <p>3 pins</p>	<p>Port I</p> <p>Port I function select</p> <p>( PI1 ... From general purpose prescaler PI2 ... From 14-bit RWM PI3 ... From timer/counter</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>MPX</p> <p>IP</p>	<p>Hi-Z</p>
<p>PI4/INT1 PI7/S11</p> <p>2 pins</p>	<p>Port I</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>Schmitt input</p> <p>IP</p> <p>P14 ... To interruption circuit P17 ... To serial CH1</p>	<p>Hi-Z</p>
<p>PI5/SCK1 PI6/SO1</p> <p>2 pins</p>	<p>Port I</p> <p>Port I function select</p> <p>Serial From CH1</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>MPX</p> <p>MPX</p> <p>IP</p> <p>Note) P15 is schmitt input P16 is inverter input</p> <p>To serial CH1</p>	<p>Hi-Z</p>
<p>PJ0 to PJ7</p> <p>8 pins</p>	<p>Port J</p> <p>Port J data</p> <p>Port J direction</p> <p>Data bus</p> <p>RD (Port J)</p> <p>Edge detection</p> <p>Standby release</p> <p>IP</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
PK0 1 pin	<p>Port K</p>	Hi-Z
$\overline{CS0}$ SIO 2 pins		Hi-Z
SO0 1 pin		Hi-Z
$\overline{SCK0}$ 1 pin		Hi-Z
EXTAL XTAL 2 pins	<ul style="list-style-type: none"> <li>• Shows the circuit composition during oscillation.</li> <li>• Feedback resistor is removed during stop.</li> </ul>	Oscillation
$\overline{RST}$ 1 pin		L level
MP 1 pin		Hi-Z

## Absolute Maximum Ratings

(V<sub>SS</sub>=0V)

Item	Symbol	Rating	Unit	Remarks
Power supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
	AV <sub>DD</sub>	AV <sub>SS</sub> to +7.0*1	V	
	AV <sub>SS</sub>	-0.3 to +0.3	V	
Input voltage	V <sub>IN</sub>	-0.3 to +7.0*2	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0*2	V	
Medium withstand output voltage	V <sub>OUTP</sub>	-0.3 to +15.0	V	PH pin
High level output current	I <sub>OH</sub>	-5	mA	
High level total output current	Σ I <sub>OH</sub>	-50	mA	Total of output pins
Low level output current	I <sub>OL</sub>	15	mA	Other than high current output pins: per pin
	I <sub>OLC</sub>	20	mA	High current port pin*3 : per pin
Low level total output current	Σ I <sub>OL</sub>	130	mA	Total of output pins
Operating temperature	T <sub>opr</sub>	-20 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	600	mW	QFP
		380		VQFP

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

\*1) AV<sub>DD</sub> and V<sub>DD</sub> should be set to a same voltage.

\*2) V<sub>IN</sub> and V<sub>OUT</sub> should not exceed V<sub>DD</sub>+0.3V.

\*3) The high current operation transistors are the N-CH transistors of the PD and PH ports.

## Recommended Operating Conditions

(V<sub>SS</sub>=0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	V <sub>DD</sub>	4.5	5.5	V	Guaranteed range during high speed mode (1/2 dividing clock) operation
		3.5	5.5	V	Guaranteed range during low speed mode (1/16 dividing clock) operation
		2.5	5.5	V	Guaranteed data hold operation range during STOP
Analog power supply	AV <sub>DD</sub>	4.5	5.5	V	*1
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	*2
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	C-MOS schmitt input*3
	V <sub>IHTS</sub>	2.2	V <sub>DD</sub>	V	TTL schmitt input*4
	V <sub>IHEX</sub>	V <sub>DD</sub> -0.4	V <sub>DD</sub> +0.3	V	EXTAL pin*5
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	*2
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	C-MOS schmitt input*3
	V <sub>ILTS</sub>	0	0.8	V	TTL schmitt input*4
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL pin*5
Operating temperature	T <sub>opr</sub>	-20	+75	°C	

- \* 1)  $V_{DD}$  and  $V_{DD}$  should be set to a same voltage.
- \* 2) Normal input port (each pin of PC, PD, PE0 to PE1, PF0 to PF3, PG, PI, PJ and PK), MP pin
- \* 3) Each pin of  $\overline{CS0}$ , SIO,  $\overline{SCK0}$ ,  $\overline{RST}$ , PE0/ $\overline{INT0}$ , PE1/ $\overline{EC}/\overline{INT2}$ , PG (For PG4 and PG5, when CMOS schmitt input is selected with mask option), PI4/ $\overline{INT1}$ , PI5/ $\overline{SCK1}$  and PI7/SI1.
- \* 4) Each pin of PG4 and PG5 (When TTL schmitt input is selected with mask option)
- \* 5) It specifies only when the external clock is input.

## Electrical Characteristics

## DC characteristics

(Ta = -20 to +75 °C, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	$V_{OH}$	PA to PD, PE2 to PE7, PF4, to PF7, PH (Vol only), PI1 to PI7, PJ, SO, $\overline{SCK}$ , $\overline{RST}$ *1 (Vol only)	$V_{DD}=4.5V, I_{OH}=-0.5mA$	4.0			V
			$V_{DD}=4.5V, I_{OH}=-1.2mA$	3.5			V
Low level output voltage	$V_{OL}$	PD, PH	$V_{DD}=4.5V, I_{OL}=1.8mA$			0.4	V
			$V_{DD}=4.5V, I_{OL}=3.6mA$			0.6	V
			$V_{DD}=4.5V, I_{OL}=12.0mA$			1.5	V
Input current	$I_{IH}$	EXTAL	$V_{DD}=5.5V, V_{IH}=5.5V$	0.5		40	$\mu A$
	$I_{IL}$		$V_{DD}=5.5V, V_{IL}=0.4V$	-0.5		-40	$\mu A$
	$I_{ILR}$		$\overline{RST}$ *2	$V_{DD}=5.5V, V_{IL}=0.4V$	-1.5		-400
I/O leakage current	$I_{IZ}$	PA to PG, PI to PK, MP, AN0 to AN3, $\overline{CS0}$ , SIO, SO, $\overline{RST}$ *2	$V_{DD}=5.5V$ $V_I=0, 5.5V$			$\pm 10$	$\mu A$
Open drain output leakage current (N-CH Tr OFF in state)	$I_{LOH}$	PH	$V_{DD}=5.5V$ $V_{OH}=12V$			50	$\mu A$
Supply current*3	$I_{DD}$	$V_{DD}$	Crystal oscillation (C1=C2=15pF) of 12MHz		21	45	mA
	$I_{DDs1}$		$V_{DD}=5V \pm 10\%$ *4		1.1	8	mA
			SLEEP mode $V_{DD}=5V \pm 10\%$				
	$I_{DDs2}$		STOP mode $V_{DD}=5V \pm 10\%$				10
Input capacity	$C_{IN}$	Other than $V_{DD}$ , $V_{SS}$ , $AV_{DD}$ , $AV_{SS}$ pins	Clock 1MHz 0V other than the measured pins		10	20	pF

- \* 1)  $\overline{RST}$  pin specifies only when the power on reset circuit has been selected with mask option.
- \* 2)  $\overline{RST}$  pin specifies the input current when the pull-up resistance is selected, and specifies leakage current when non-resistance is selected.
- \* 3) When entire output pins are open.
- \* 4) When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FEH) to "00" and operating in high speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing

( $T_a = -20$  to  $+75$  °C,  $V_{DD} = 4.5$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	$f_c$	XTAL EXTAL	Fig. 1, Fig. 2	1	12	MHz
System clock input pulse width	$t_{xL}$ $t_{xH}$	EXTAL	Fig. 1, Fig. 2 (External clock drive)	37.5		ns
System clock input rising and falling times	$t_{cR}$ $t_{cF}$				200	ns
Event count clock input pulse width	$t_{eL}$ $t_{eH}$	$\overline{EC}$	Fig. 3	$t_{sys}^*$ +50		ns
Event count clock input rising and falling times	$t_{eR}$ $t_{eF}$	$\overline{EC}$	Fig. 3		20	ms

\*  $t_{sys}$  indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

$t_{sys}$  [ns] =  $2000/f_c$  (Upper 2-bit="00"),  $4000/f_c$  (Upper 2-bit="01"),  $16000/f_c$  (Upper 2-bit="11")

Fig. 1 Clock timing

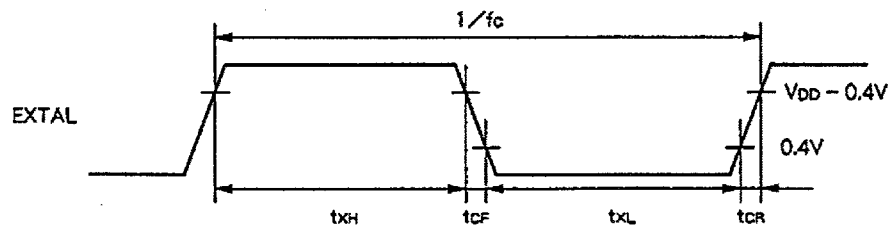


Fig. 2 Clock applying condition

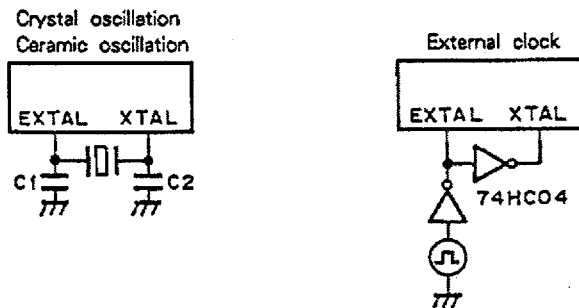
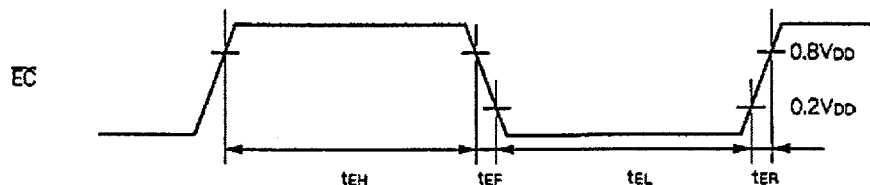


Fig. 3 Event count clock timing



## (2) Serial transfer (CH0)

(Ta = -20 to +75°C, V<sub>DD</sub>=4.5 to 5.5V, V<sub>SS</sub>=0V)

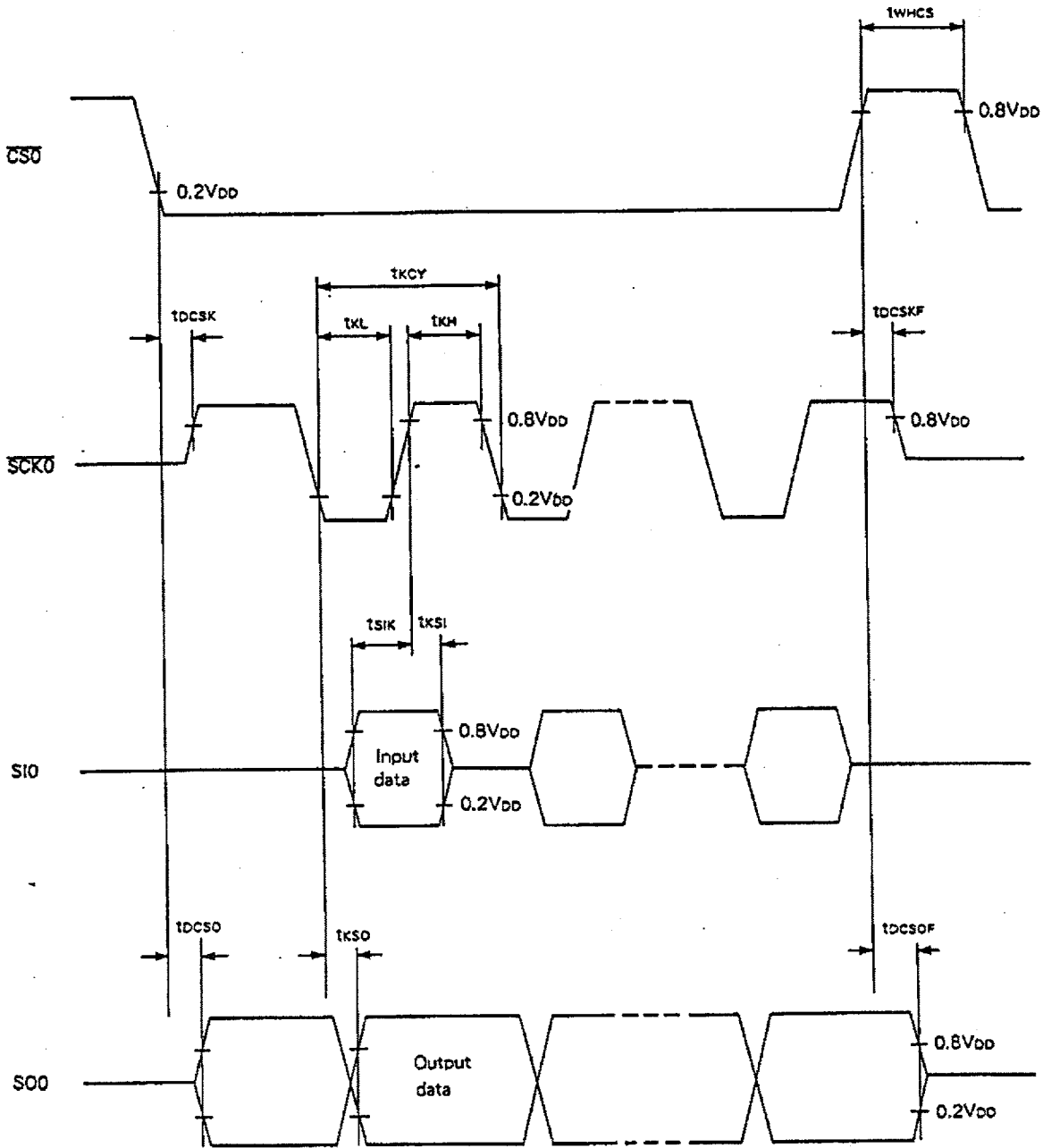
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t <sub>DCSK</sub>	$\overline{SCK0}$	Chip select transfer mode ( $\overline{SCK0}$ =output mode)		t <sub>sys</sub> +200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ floating delay time	t <sub>DCSKF</sub>	$\overline{SCK0}$			t <sub>sys</sub> +200	ns
$\overline{CS0} \downarrow \rightarrow SO0$ delay time	t <sub>DCSO</sub>	SO0	Chip select transfer mode		t <sub>sys</sub> +200	ns
$\overline{CS0} \downarrow \rightarrow SO0$ floating delay time	t <sub>DCSOF</sub>	SO0			t <sub>sys</sub> +200	ns
$\overline{CS0}$ high level width	t <sub>WHCS</sub>	$\overline{CS0}$			t <sub>sys</sub> +200	ns
$\overline{SCK0}$ cycle time	t <sub>KCY</sub>	$\overline{SCK0}$	Input mode	2t <sub>sys</sub> +200		ns
			Output mode	16000/f <sub>c</sub>		ns
$\overline{SCK0}$ high and low level widths	t <sub>KH</sub> t <sub>KL</sub>	$\overline{SCK0}$	Input mode	t <sub>sys</sub> +100		ns
			Output mode	8000/f <sub>c</sub> -50		ns
SIO input setup time (against $\overline{SCK0} \uparrow$ )	t <sub>SIK</sub>	SIO	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SIO input hold time (against $\overline{SCK0} \uparrow$ )	t <sub>HSI</sub>	SIO	$\overline{SCK0}$ input mode	t <sub>sys</sub> +200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow SO0$ delay time	t <sub>KSO</sub>	SO0	$\overline{SCK0}$ input mode		t <sub>sys</sub> +200	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) t<sub>sys</sub> indicates three values according to the contents of the clock control register (address; 00FEh) upper 2 bits (CPU clock selection).

t<sub>sys</sub> [ns] = 2000/f<sub>c</sub> (Upper 2-bit="00"), 4000/f<sub>c</sub> (Upper 2-bit="01"), 16000/f<sub>c</sub> (Upper 2-bit="11")

2) The Load of  $\overline{SCK0}$  output mode and SO0 output delay time is 50pF+1TTL.

Fig. 4 Serial transfer CH0 timing





Serial transfer (CH1) (SIO mode)

( $T_a = -20$  to  $+75$  °C,  $V_{DD} = 4.5$  to  $5.5V$ ,  $V_{SS} = 0V$ )

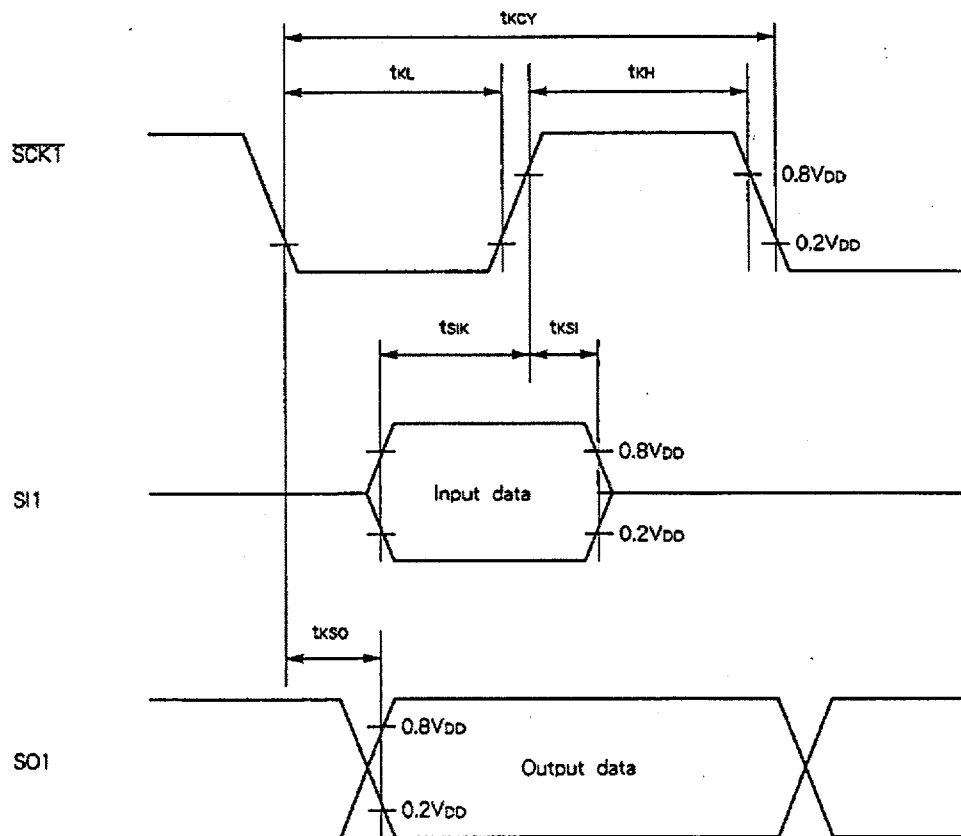
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	$t_{KCY}$	$\overline{SCK1}$	Input mode	$2t_{sys} + 200$		ns
			Output mode	$16000/f_c$		ns
$\overline{SCK1}$ high and low level widths	$t_{KH}$ $t_{KL}$	$\overline{SCK1}$	Input mode	$t_{sys} + 100$		ns
			Output mode	$8000/f_c - 50$		ns
SI1 input setup time (against $\overline{SCK1} \uparrow$ )	$t_{SIK}$	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (against $\overline{SCK1} \uparrow$ )	$t_{SIS}$	SI1	$\overline{SCK1}$ input mode	$t_{sys} + 200$		ns
			$\overline{SCK1}$ output mode	100		ns
$\overline{SCK1} \downarrow \rightarrow$ SO1 delay time	$t_{KSO}$	SO1	$\overline{SCK1}$ input mode		$t_{sys} + 200$	ns
			$\overline{SCK1}$ output mode		100	ns

**Note 1)**  $t_{sys}$  indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

$t_{sys}$  [ns] = 2000 /  $f_c$  (Upper 2-bit="00"), 4000 /  $f_c$  (Upper 2-bit="01"), 16000 /  $f_c$  (Upper 2-bit="11").

**2)** The Load of  $\overline{SCK1}$  output mode and SO1 output delay time is 50pF + 1TTL.

Fig. 5 Serial transfer CH1 timing (SIO mode)



**Serial transfer (CH1) (Special mode)**

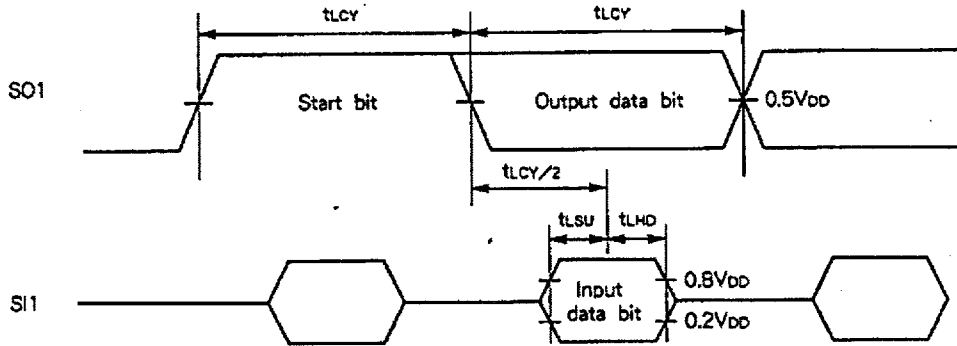
( $T_a = -20$  to  $+75$  °C,  $V_{DD} = 4.5$  to  $5.5$  V,  $V_{SS} = 0$  V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	$t_{CY}$	SO1 SI1	Note 1)		104		$\mu$ s
SI1 data setup time	$t_{SU}$	SI1		2			$\mu$ s
SI1 data hold time	$t_{HD}$	SI1		2			$\mu$ s

**Note 1)**  $t_{CY}$  specifies only serial mode register (CH1) (SIOM1: Address 01FAh) lower 2 bits (SO1 clock selection) has been set at 104  $\mu$ s.

**2)** The Load of SO1 pin is 50pF +1TTL.

**Fig. 6 Serial transfer CH1 timing (Special mode)**

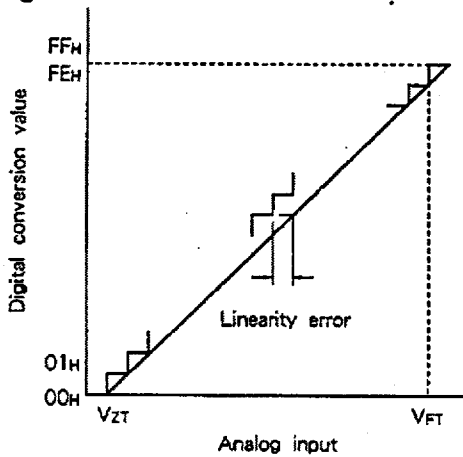


(3) A/D converter characteristics

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = AV_{DD} = 4.5$  to  $5.5\text{V}$ ,  $AV_{REF} = 4.0\text{V}$  to  $AV_{DD}$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ )

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			$\pm 1$	LSB
Zero transition voltage	$V_{ZT}^{*1}$			-10	30	70	mV
Full scale transition voltage	$V_{FT}^{*2}$			4930	4970	5010	mV
Conversion time	$t_{CONV}$			$160/f_{ADC}^{*3}$			$\mu\text{s}$
Sampling time	$t_{SAMP}$			$12/f_{ADC}^{*3}$			$\mu\text{s}$
Reference input voltage	$V_{REF}$	$AV_{REF}$		$AV_{DD} - 0.5$		$AV_{DD}$	V
Analog input voltage	$V_{IAN}$	AN0 to AN11		0		$AV_{REF}$	V
$AV_{REF}$ current	$I_{REF}$	$AV_{REF}$	Operating mode		0.6	1.0	mA
	$I_{REFS}$		SLEEP mode STOP mode			10	$\mu\text{A}$

Fig. 7. Definitions of A/D converter terms



- \*1)  $V_{ZT}$ : Indicates the value that digital conversion value changes from 00H to 01H and vice versa.
- \*2)  $V_{FT}$ : Indicates the value that digital conversion value changes from FEH to FFH and vice versa.
- \*3) The value of  $f_{ADC}$  is as follows by selecting ADC operation clock (MSC: Address 01FFH bit 0).  
When PS2 is selected,  $f_{ADC} = f_c/2$   
When PS1 is selected,  $f_{ADC} = f_c$

(4) Interruption, reset input

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	$t_{IH}$ , $t_{IL}$	INT0, INT1, INT2 PJ0 to PJ7		1		$\mu\text{s}$
Reset input low level width	$t_{RSL}$	RST		8/fc		$\mu\text{s}$

Fig. 8 Interruption input timing

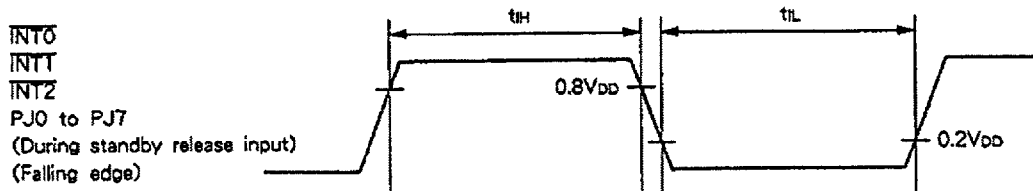
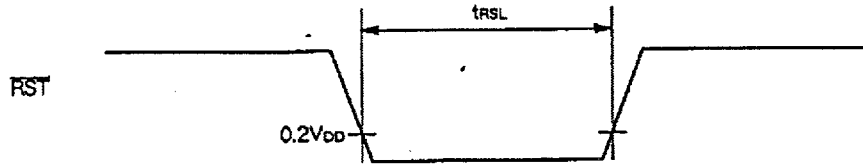


Fig. 9 Reset input timing



(5) Power on reset

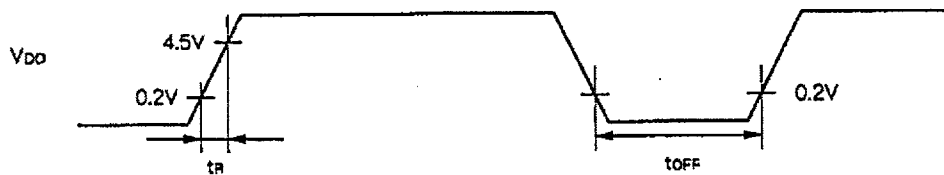
Power on reset \*

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising time	$t_r$	$V_{DD}$	Power on reset	0.05	50	ms
Power supply cut-off time	$t_{off}$		Repetitive power on reset	1		ms

\* Specifies only when power on reset function is selected.

Fig. 10 Power on reset



The power supply should rise smoothly.

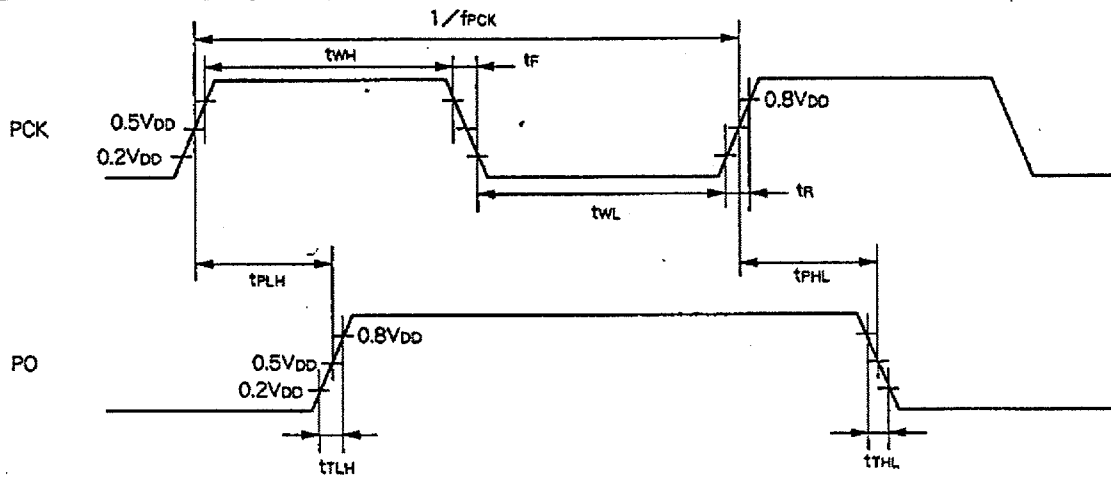
(6) General purpose prescaler

(Ta=-20 to +75 °C, VDD=4.5 to 5.5V, VSS=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
External clock input frequency	fPCK	PCK				12	MHz
External clock input pulse width	tWH, tWL	PCK		33			ns
External clock input rising and falling times	tr, tf	PCK				200	ns
Prescaler output delay time (against PCK ↑)	tPLH	PO	External clock input PCK tr=tf=6ns		80	130	ns
	tPHL				60	100	ns
Prescaler output rising and falling times	tTLH	PO	External clock input PCK tr=tf=6ns		50	100	ns
	tTHL				20	40	ns

Note) The Load of PO pin is 50pF.

Fig. 11 General purpose prescaler timing



(7) Others

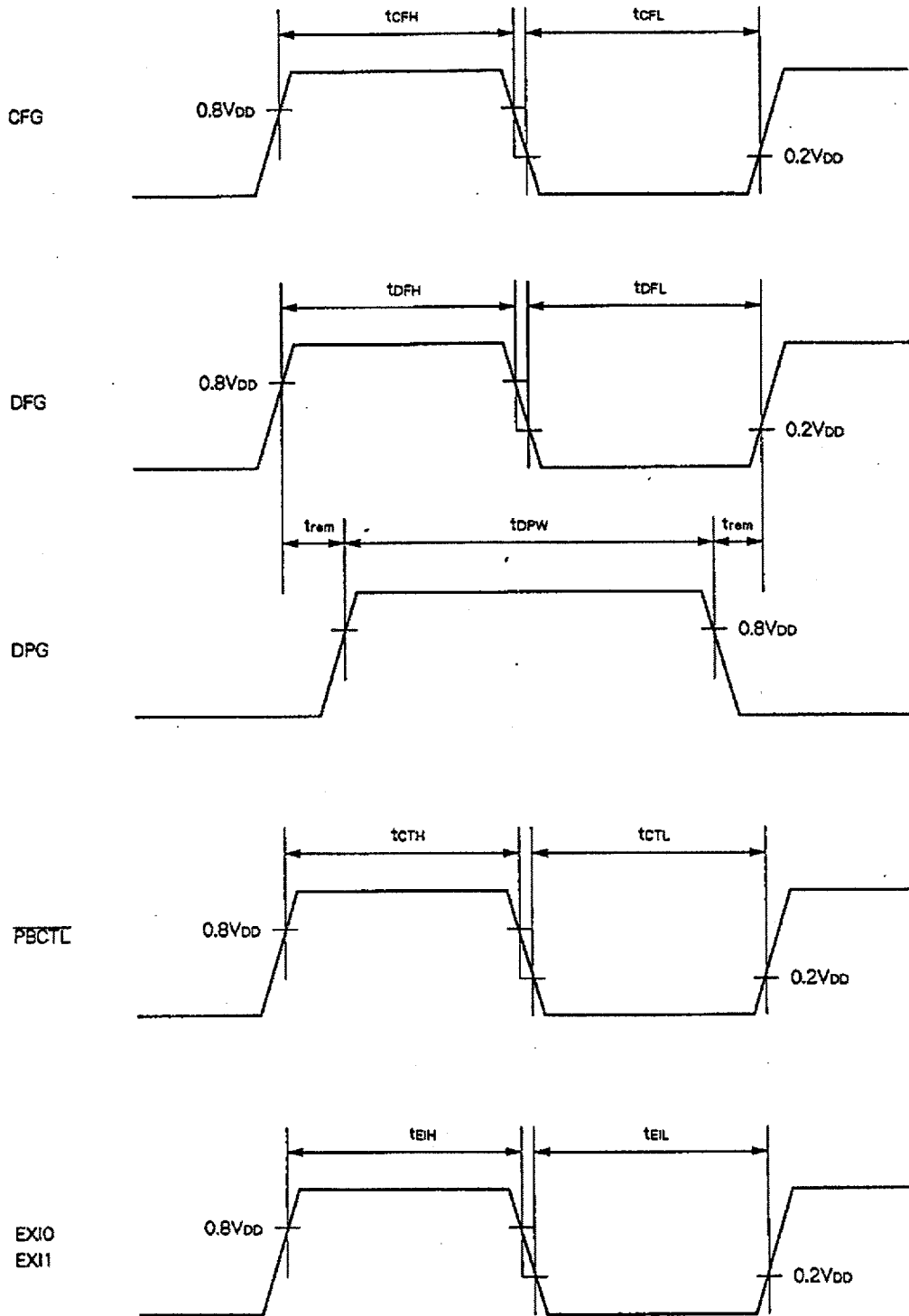
(Ta = -20 to +75 °C, VDD=4.5 to 5.5V, VSS=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
CFG input high and low level widths	tCFH, tCFL	CFG		tsys+200		ns
DFG input high and low level widths	tDFH, tDFL	DFG		1000/fc+200		ns
DPG minimum pulse width	tDPW	DPG		50		ns
DPG minimum removal time	trem	DPG		50		ns
PBCTL input high and low level widths	tCTH, tCTL	PBCTL	tsys=2000/fc	tsys+200		ns
EXI input high and low level widths	tEIH, tEIL	EXI0 EXI1	tsys=2000/fc	tsys+200		ns

Note) tsys indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

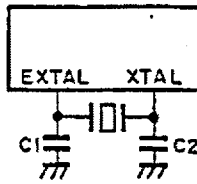
tsys [ns] = 2000/fc (Upper 2-bit="00"), 4000/fc (Upper 2-bit="01"), 16000/fc (Upper 2-bit="11")

Fig. 12 Others timing



Supplement

Fig. 13 Recommended oscillation circuit



Manufacturer	Model	Frequency range (MHz)	C <sub>1</sub> , C <sub>2</sub> (pF)
MURATA MFG CO., LTD.	CSA12.0MTZ0C3	12	30

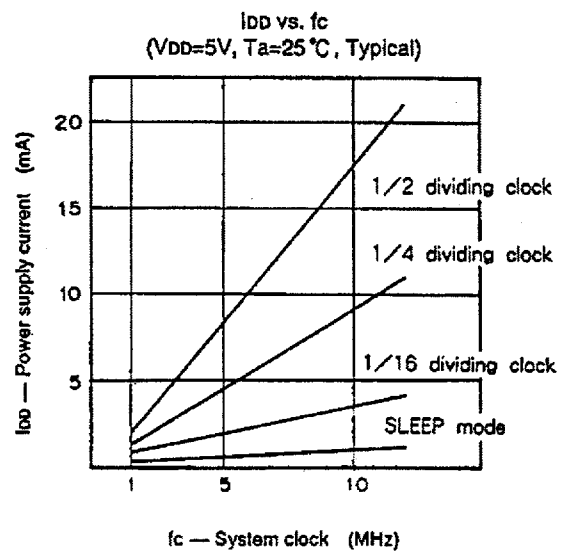
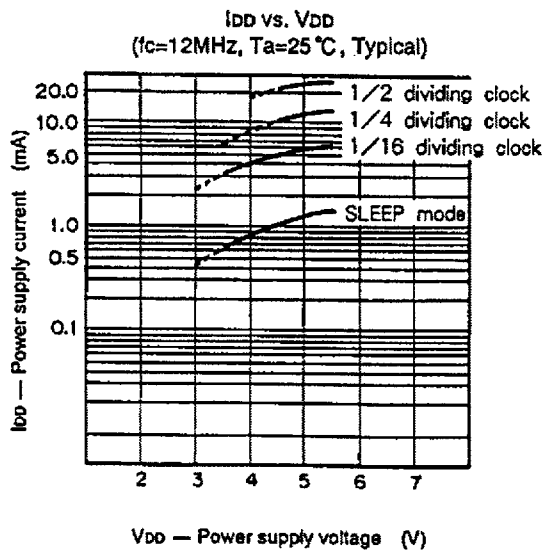
Manufacturer	Model	Frequency range (MHz)	C <sub>1</sub> , C <sub>2</sub> (pF)
RIVER ELETEC CO., LTD.	HC-49/U03	12	12
KINSEKI LTD.	HC-49/U	12	15
CITIZEN WATCH CO., LTD.	CSA-309	12	10

Mask option table

Item	Content	
Reset pin pull-up resistor	Non-existent	Exsistent
Power on reset circuit	Non-existent	Exsistent
Input circuit format Note)	C-MOS schmitt	TTL schmitt

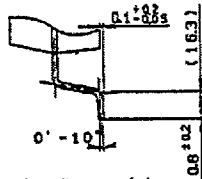
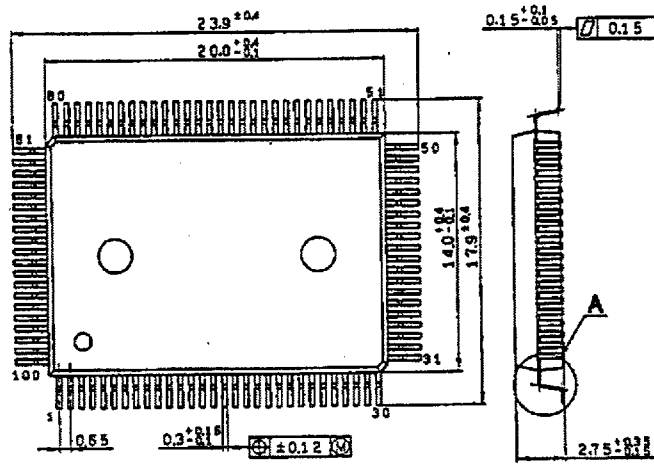
Note) In PG4/SYNC0 pin and PG5/SYNC1 pin, the input circuit format can be selected to every pin.

Characteristics Curve



Package Outline Unit : mm

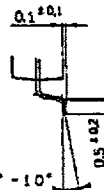
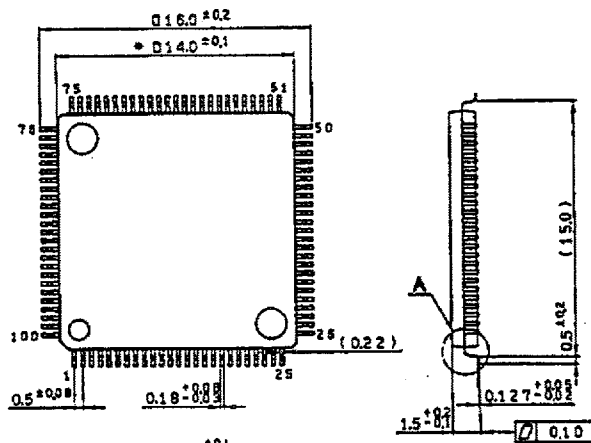
100pin QFP (Plastic) 1.7g



SONY NAME	QFP-100P-L01
EIAJ NAME	*QFP100-P-1420-A
JEDEC CODE	

Detailed diagram of A

100pin VQFP (Plastic)



SONY NAME	VQFP-100P-L01
EIAJ NAME	*QFP100-P-1414-A
JEDEC CODE	

Detailed diagram of A

Note) Dimensions marked with \* does not include resin residue.