Elektronische Bauelemente

SSG4825PE

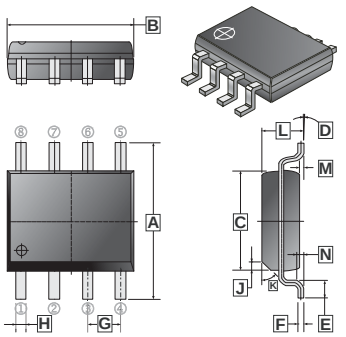
-11.5 A, 30 V, $R_{DS(ON)}$ 13 mΩ
P-Channel Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

SOP-8



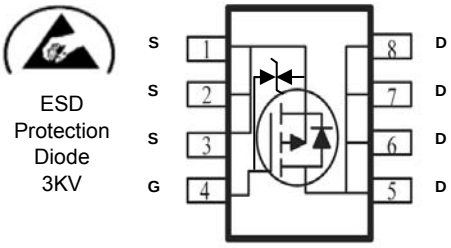
REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	H	0.35	0.49
B	4.80	5.00	J	0.375 REF.	
C	3.80	4.00	K	45°	
D	0°	8°	L	1.35	1.75
E	0.40	0.90	M	0.10	0.25
F	0.19	0.25	N	0.25 REF.	
G	1.27 TYP.				

FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe SOP-8 saves board space.
- Fast switching speed.
- High performance trench technology.

PACKAGE INFORMATION

Package	MPQ	LeaderSize
SOP-8	2.5K	13' inch



MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±25	V
Continuous Drain Current [1]	I_D @ T_A = 25°C	-11.5	A
	I_D @ T_A = 70°C	-9.3	A
Pulsed Drain Current [2]	I_{DM}	±50	A
Continuous Source Current (Diode Conduction) [1]	I_S	-2.1	A
Total Power Dissipation [1]	P_D @ T_A = 25°C	3.1	W
	P_D @ T_A = 70°C	2.3	W
Operating Junction & Storage Temperature Range	T_J, T_{STG}	-55 ~ 150	°C
Thermal Resistance Ratings			
Thermal Resistance Junction-Case (Max.) [1]	t ≦ 5 sec	$R_{\theta JC}$	25	°C / W
Thermal Resistance Junction-Ambient (Max.) [1]	t ≦ 5 sec	$R_{\theta JA}$	50	°C / W

Notes:
1 Surface Mounted on 1" x 1" FR4 Board.
2 Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	-30	-	-	V	V_{GS}= 0V, I_D= -250μA
Gate Threshold Voltage	$V_{GS(th)}$	-1	-	-	V	V_{DS}= V_{GS}, I_D= -250μA
Gate-Body Leakage Current	I_{GSS}	-	-	±1	μA	V_{DS}= 0V, V_{GS}= ±25V
Zero Gate Voltage Drain Current	I_{DSS}	-	-	-1	μA	V_{DS}= -24V, V_{GS}= 0V
		-	-	-5	μA	V_{DS}= -24V, V_{GS}= 0V, T_J= 55°C
On-State Drain Current [1]	$I_{D(on)}$	-50	-	-	A	V_{DS}= -5V, V_{GS}= -10V
Drain-Source On-Resistance [1]	$R_{DS(ON)}$	-	-	13	mΩ	V_{GS}= -10V, I_D= -11.5A
		-	-	19		V_{GS}= -4.5V, I_D= -9.3A
Forward Transconductance [1]	g_{fs}	-	29	-	S	V_{DS}= -15V, I_D= -11.5A
Diode Forward Voltage	V_{SD}	-	-0.8	-	V	I_S= 2.5A, V_{GS}= 0V
Dynamic [2]						
Total Gate Charge	Q_g	-	25	-	nC	I_D= -11.5A V_{DS}= -15V V_{GS}= -5V
Gate-Source Charge	Q_{gs}	-	11	-		
Gate-Drain Charge	Q_{gd}	-	17	-		
Input Capacitance	C_{iss}	-	2300	-	pF	V_{DS}= -15V V_{GS}= 0V f= 1MHz
Output Capacitance	C_{oss}	-	600	-		
Reverse Transfer Capacitance	C_{rss}	-	300	-		
Turn-On Delay Time	$T_{d(on)}$	-	15	-	nS	V_{DD}= -15V I_D= -1A V_{GEN}= -10V R_L= 6Ω
Rise Time	T_r	-	13	-		
Turn-Off Delay Time	$T_{d(off)}$	-	100	-		
Fall Time	T_f	-	54	-		

Notes:

1 Pulse test : PW ≦ 300μs duty cycle ≦ 2%.

2 Guaranteed by design, not subject to production testing.