FUJITSU

MOS 65536-BIT DYNAMIC RANDOM ACCESS MEMORY

MB 8265A-10
MB 8265A-12
MB 8265A-15

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

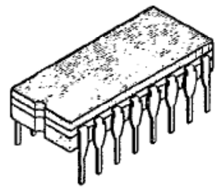
The Fujitsu MB 8265A is a fully decoded, dynamic random access memory organized as 65,536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MB 8265A to be housed in a standard 16 pin DIP and 18 pad LCC. Pin-outs conform to the JEDEC approved pin out.

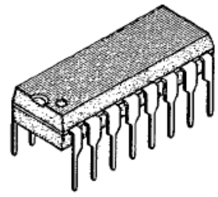
The MB 8265A is fabricated using silicon gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

- 65,536 x 1 RAM, 16 pin DIP/18 pad LCC
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  100 ns max (MB 8265A-10)
  120 ns max (MB 8265A-12)
  150 ns max (MB 8265A-15)
- Cycle time,
  190 ns min (MB 8265A-10)
  230 ns min (MB 8265A-12)
  260 ns min (MB 8265A-15)
- Single +5V Supply, ±10% tolerance
- Low power (active)
  275 mW max (MB 8265A-10)
  248 mW max (MB 8265A-12)
  220 mW max (MB 8265A-15)
  25mW standby (max)
- 2 ms/128 refresh cycle
- $\overline{RAS}$-only and $\overline{RFSH}$ (pin 1) refresh capability
- Offers two variations of Hidden refresh
- Read-Modify-Write, and Page-mode capability
- Common I/O capability using Early Write operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- On-chip latches for Addresses and Data-in
- t_{AR}, t_{WCR}, t_{DHR} are eliminated
- Standard 16-pin Ceramic (Cerdip) DIP: Suffix-Z
  Standard 16-pin Plastic DIP: Suffix-P
  Standard 18-pad Ceramic LCC: Suffix-TV



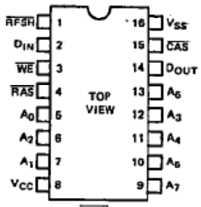
CERAMIC PACKAGE
CERDIP
DIP-16C-C04

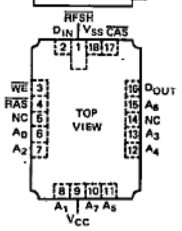


PLASTIC PACKAGE
DIP-16P-M03

LCC-18C-F02: See Page 1-218

PIN ASSIGNMENT





LCC PAD CONFIGURATION: See Page 1-218.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	–1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	–1 to +7	V
Storage temperature	Ceramic	T_{STG}	–55 to +150	°C
	Pastic		–55 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current			50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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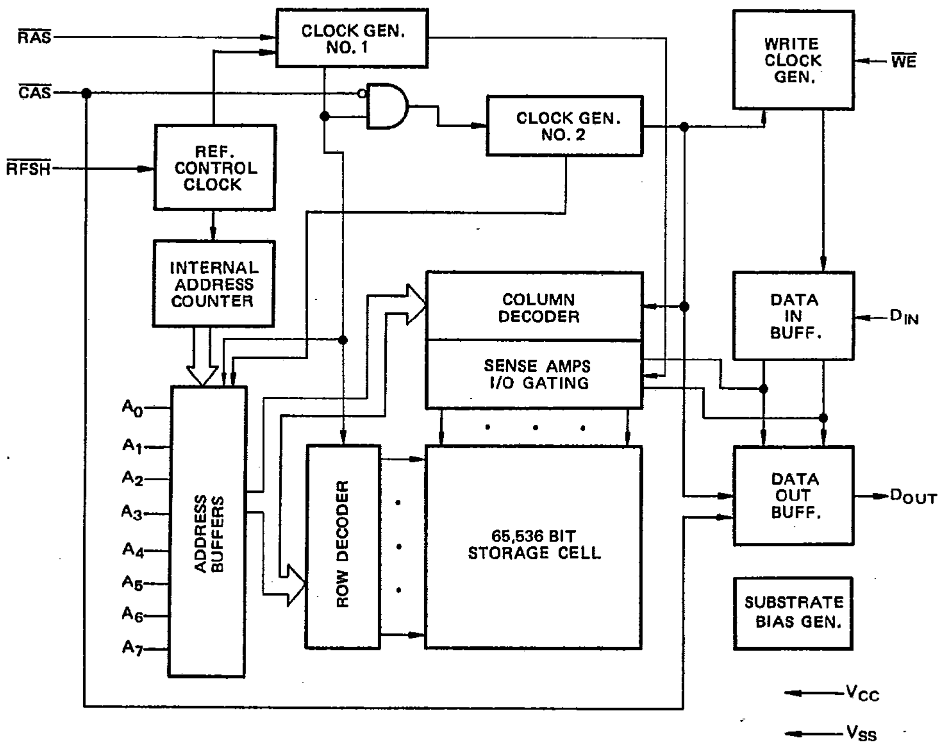
Fig. 1 – MB 8265A BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0 to A_7, D_{IN}	C_{IN1}		5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{RFSH}$	C_{IN2}		8	pF
Output Capacitance D_{OUT}	C_{OUT}		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V	0°C to +70°C
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}*	-1.0		0.8	V	

Note * : The device can withstand undershoots to the –2V level with a pulse width of 20 ns.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING CURRENT* Average power supply current ($\overline{RFSH}$ = V_{IH}, $\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 8265A-10	I_{CC1}		50	mA
	MB 8265A-12			45	
	MB 8265A-15			40	
STANDBY CURRENT Standby power supply current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{RFSH}$ = V_{IH})		I_{CC2}		4.5	mA
REFRESH CURRENT 1* Average power supply current ($\overline{CAS}$ = $\overline{RFSH}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB 8265A-10	I_{CC3}		38	mA
	MB 8265A-12			35	
	MB 8265A-15			31	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{RFSH}$ = V_{IH}, $\overline{CAS}$ cycling; t_{PC} = min)	MB 8265A-10	I_{CC4}		35	mA
	MB 8265A-12			32	
	MB 8265A-15			28	
REFRESH CURRENT 2* Average power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, $\overline{RFSH}$ cycling; t_{FC} = min)	MB 8265A-10	I_{CC5}		42	mA
	MB 8265A-12			38	
	MB 8265A-15			34	
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≦ V_{IN} ≦ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not test = 0V)		$I_{I(L)}$	-10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		$I_{O(L)}$	-10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH} = -5mA) Output low voltage (I_{OL} = 4.2mA)		V_{OH} V_{OL}	2.4	 0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1,2,3

Parameter NOTES	Symbol	MB 8265A-10		MB 8265A-12		MB 8265A-15		Unit
		Min	Max	Min	Max	Min	Max	
Time between Refresh	t_{REF}		2		2		2	ms
Random Read/Write Cycle Time	t_{RC}	190		230		260		ns
Read-Write Cycle Time	t_{RWC}	230		265		280		ns
Page Mode Cycle Time	t_{PC}	105		120		145		ns
Page Mode Read-Write Cycle Time	t_{PRWC}	135		155		180		ns
Access Time from RAS [4] [6]	t_{RAC}		100		120		150	ns
Access Time from CAS [5] [6]	t_{CAC}		50		60		75	ns
Output Buffer Turn Off Delay	t_{OFF}	0	30	0	35	0	40	ns
Transition Time	t_T	3	50	3	50	3	50	ns
RAS Precharge Tim	t_{RP}	80		100		100		ns
RAS Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns
RAS Hold Time	t_{RSH}	50		60		75		ns
CAS Precharge Time (Page mode only)	t_{CP}	45		50		60		ns
CAS Precharge Time (All cycles except page mode)	t_{CPN}	20		20		25		ns
CAS Pulse Width	t_{CAS}	50	10000	60	10000	75	10000	ns
CAS Hold Time	t_{CSH}	100		120		150		ns
RAS to CAS Delay Time [7] [8]	t_{RCD}	20	50	20	60	25	75	ns
CAS to RAS Precharge Time	t_{CRP}	0		0		0		ns
Row Address Set Up Time	t_{ASR}	0		0		0		ns
Row Address Hold Time	t_{RAH}	10		10		15		ns
Column Address Set Up Time	t_{ASC}	0		0		0		ns
Column Address Hold Time	t_{CAH}	15		15		20		ns
Read Command Set Up Time	t_{RCS}	0		0		0		ns
Read Command Hold Time Referenced to CAS [10]	t_{RCH}	0		0		0		ns
Read Command Hold Time Referenced to RAS [10]	t_{RRH}	20		20		20		ns
Write Command Set Up Time [9]	t_{WCS}	0		0		0		ns
Write Command Hold Time	t_{WCH}	20		25		30		ns
Write Command Pulse Width	t_{WP}	20		25		30		ns
Write Command to RAS Lead Time	t_{RWL}	35		40		45		ns
Write Command to CAS Lead Time	t_{CWL}	35		40		45		ns
Data In Set Up Time	t_{DS}	0		0		0		ns
Data In Hold Time	t_{DH}	20		25		30		ns
CAS to WE Delay [9]	t_{CWD}	40		50		60		ns
RAS to WE Delay [9]	t_{RWD}	90		110		120		ns
RAS Precharge to CAS Hold Time (RAS-only refresh)	t_{RPC}	20		20		20		ns

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1,2,3

Parameter	NOTES	Symbol	MB 8265A-10		MB 8265A-12		MB8265A-15		Unit
			Min	Max	Min	Max	Min	Max	
$\overline{RFSH}$ Set up Time Referenced to $\overline{RAS}$		t_{FSR}	90		100		100		ns
$\overline{RAS}$ to $\overline{RFSH}$ Delay ($\overline{RFSH}$ refresh)		t_{RFD}	90		100		100		ns
$\overline{RFSH}$ Cycle Time ($\overline{RFSH}$ refresh)		t_{FC}	200		230		260		ns
$\overline{RFSH}$ Pulse Width ($\overline{RFSH}$ refresh)		t_{FP}	100		120		150		ns
$\overline{RFSH}$ Inactive Time ($\overline{RFSH}$ refresh)		t_{FI}	90		100		100		ns
$\overline{RFSH}$ to $\overline{RAS}$ Delay	11	t_{FRD}	20		30		40		ns
$\overline{RFSH}$ Hold Time	11	t_{FSH}	30		40		50		ns

Notes:

1. An initial pause of 200 μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RFSH}$ cycles before proper device operation is achieved.
   If internal refresh counter is to be effective, a minimum of 8 active $\overline{RFSH}$ initialization cycles is required. The internal refresh counter must be activated a minimum of 128 times every 2 ms if the $\overline{RFSH}$ refresh function is used.
   If the $\overline{RFSH}$ refresh function is not used, $\overline{RFSH}$ (pin 1) pin can be open.
2. AC characteristics assume t_T = 5ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max.).
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T=5ns) + t_{ASC} (min)
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.
   If $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. $\overline{RFSH}$ counter test read/write cycle only.

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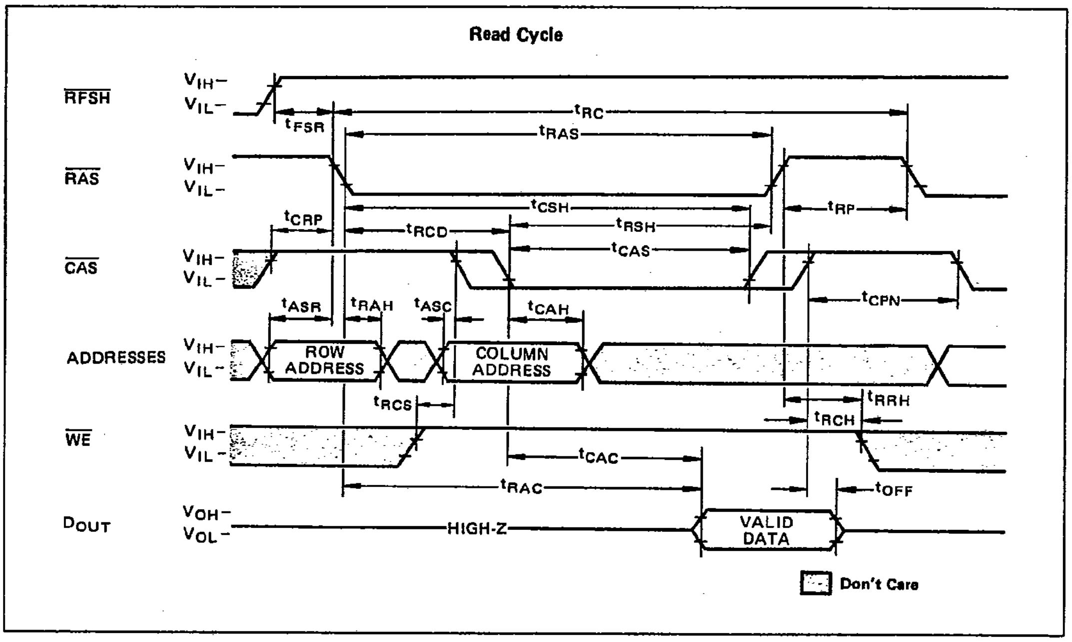
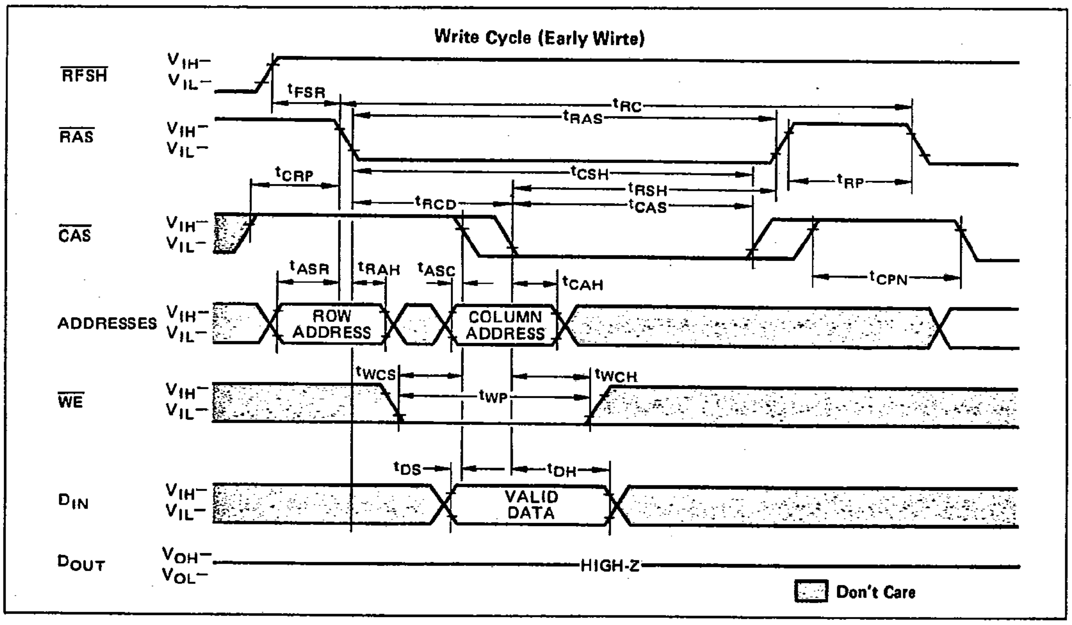
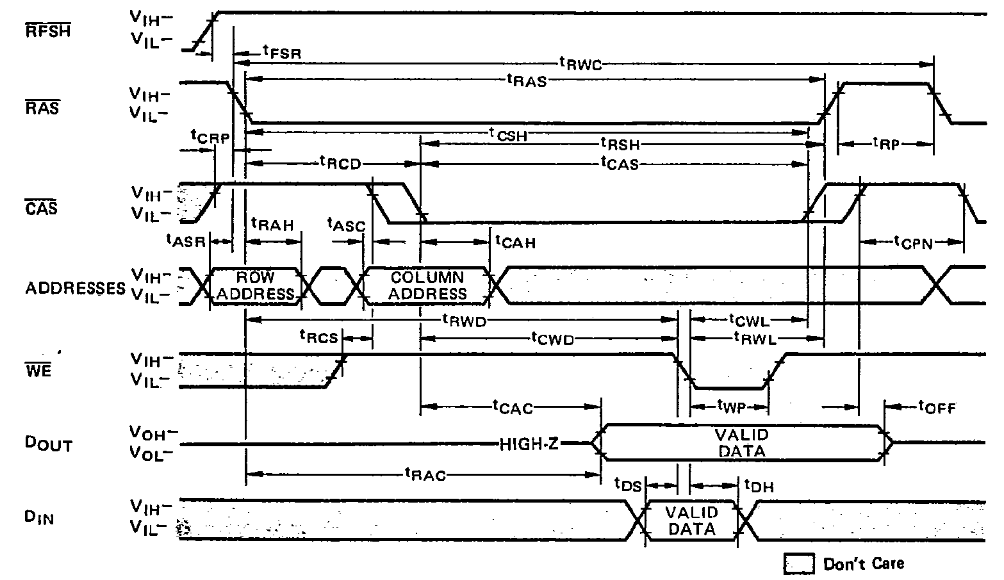
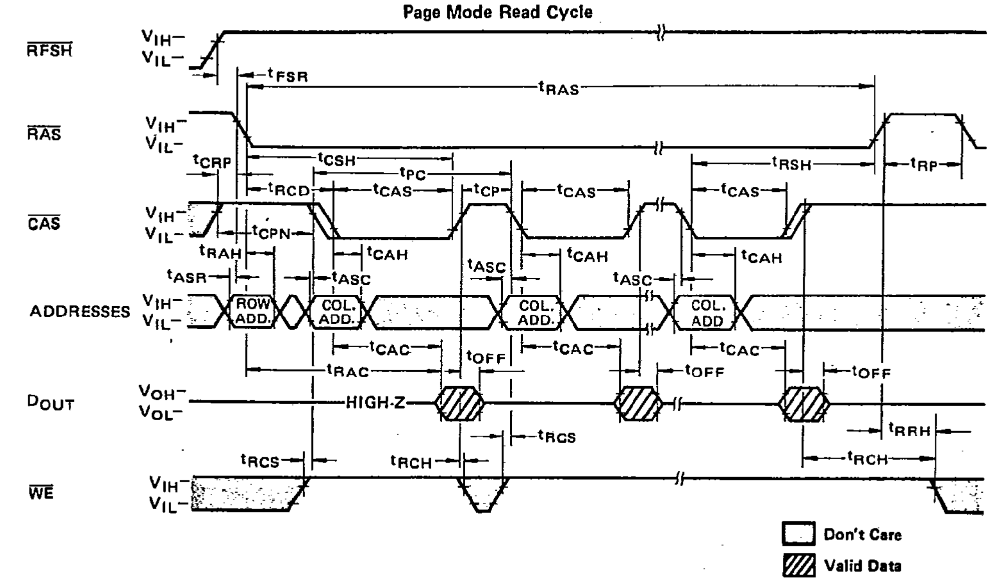


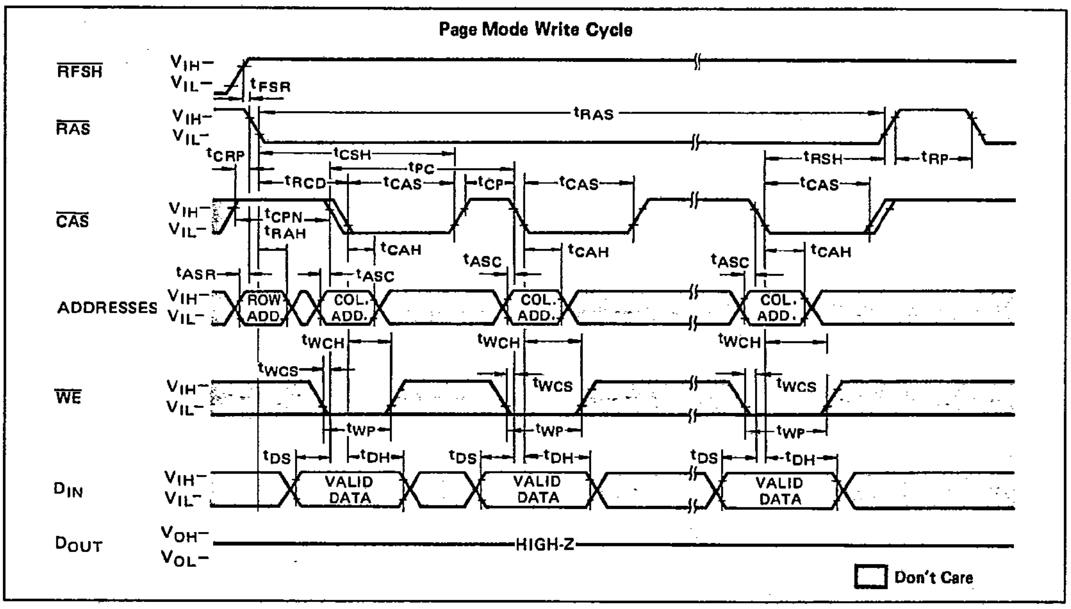


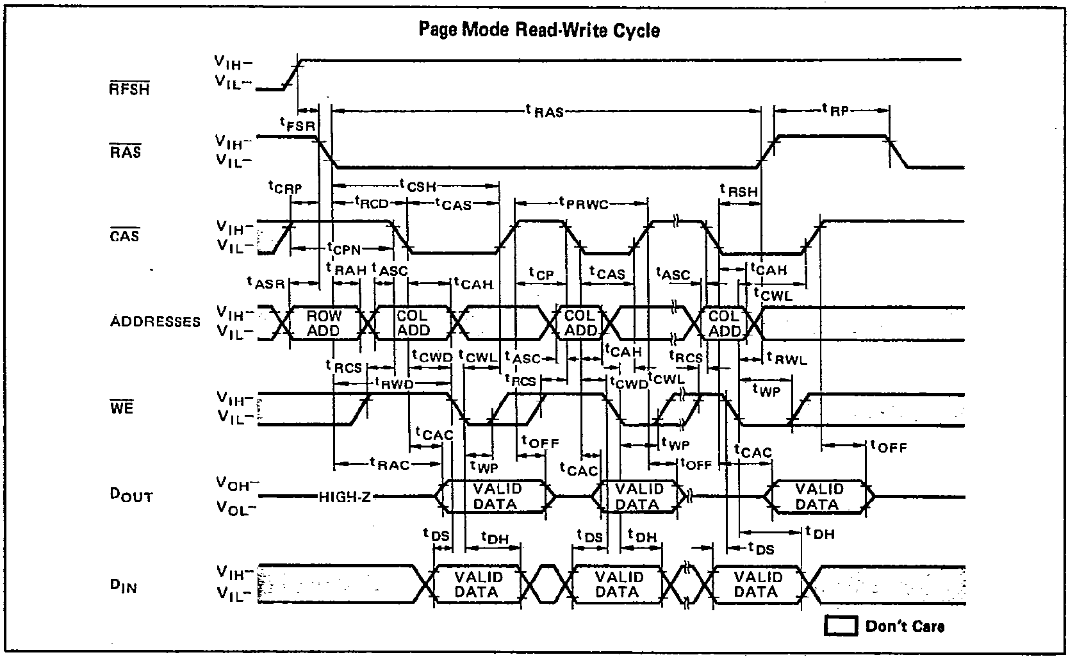
Read–Write/Read–Modify–Write Cycle

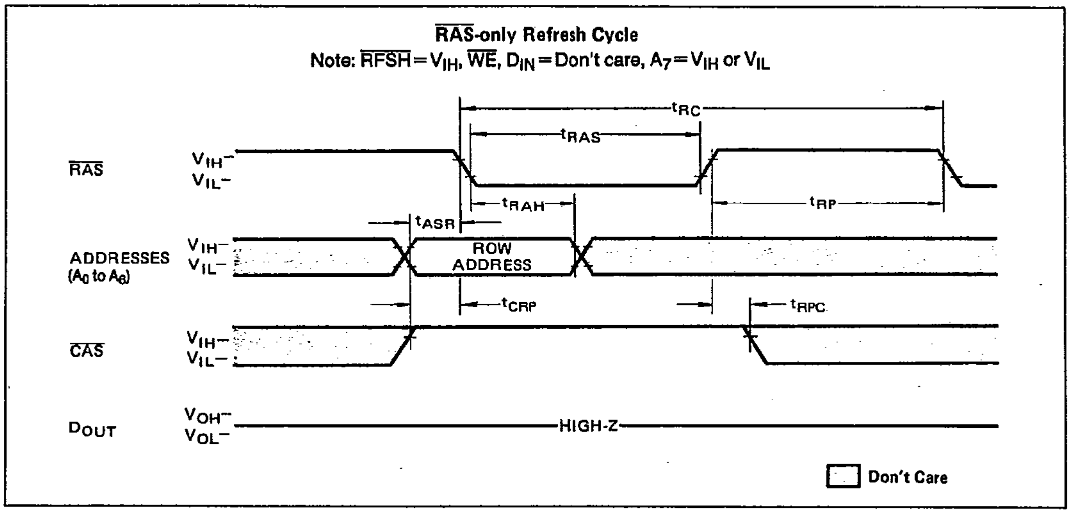


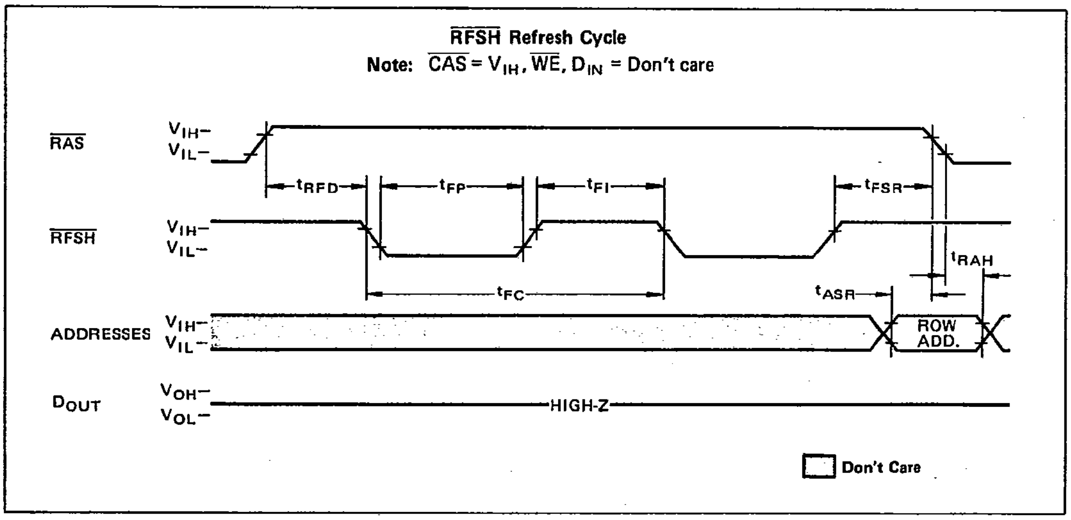
Page Mode Read Cycle



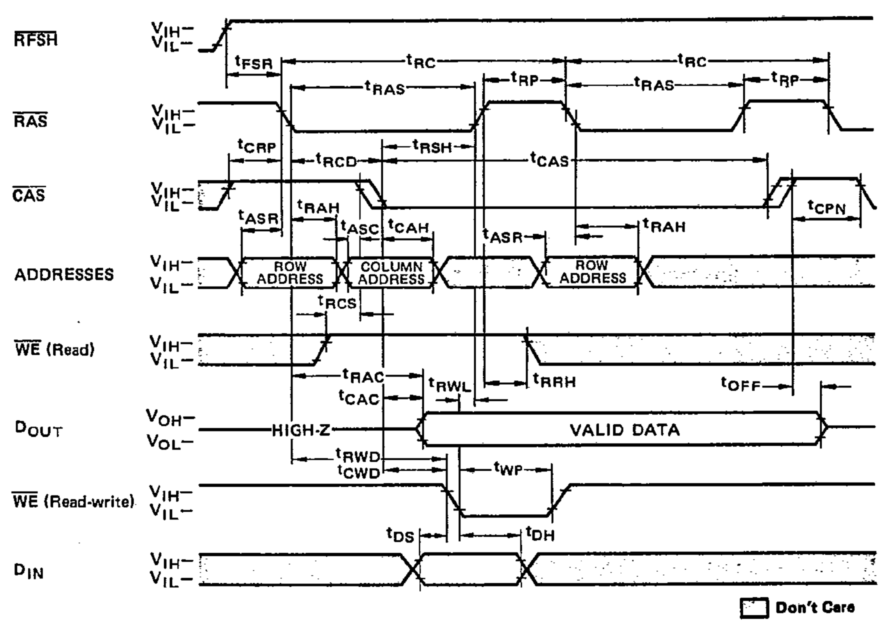

Page Mode Write Cycle
RFSH
RAS
CAS
ADDRESSES
WE
DIN
DOUT
VIH
VIL
VOH
VOL
tFSR
tRAS
tCRP
tCSH
tPC
tRCD
tCAS
tCP
tRSH
tRP
tCPN
tRAH
tCAH
tASC
tASR
ROW ADD.
COL. ADD.
tWCH
tWCS
tWP
tDS
tDH
VALID DATA
HIGH-Z
Don't Care


Page Mode Read-Write Cycle
RFSH
RAS
CAS
ADDRESSES
WE
DOUT
DIN
VIH
VIL
VOH
VOL
tFSR
tRAS
tRP
tCRP
tCSH
tRCD
tCAS
tPRWC
tRSH
tCPN
tRAH
tASC
tASR
tCAH
tCP
tCWL
ROW ADD
COL ADD
tCWD
tRCS
tRWD
tRWL
tWP
tCAC
tOFF
tRAC
HIGH-Z
VALID DATA
tDS
tDH
Don't Care

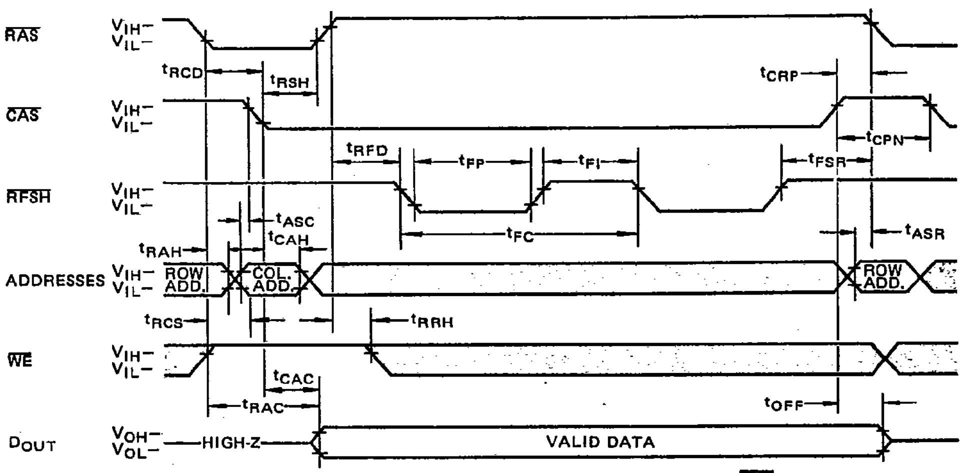

RAS-only Refresh Cycle
Note: RFSH = VIH, WE, DIN = Don't care, A7 = VIH or VIL
tRC
tRAS
tRAH
tASR
tRP
tCRP
tRPC
RAS
ADDRESSES (A0 to A6)
ROW ADDRESS
CAS
DOUT
VIH
VIL
VOH
VOL
HIGH-Z
Don't Care

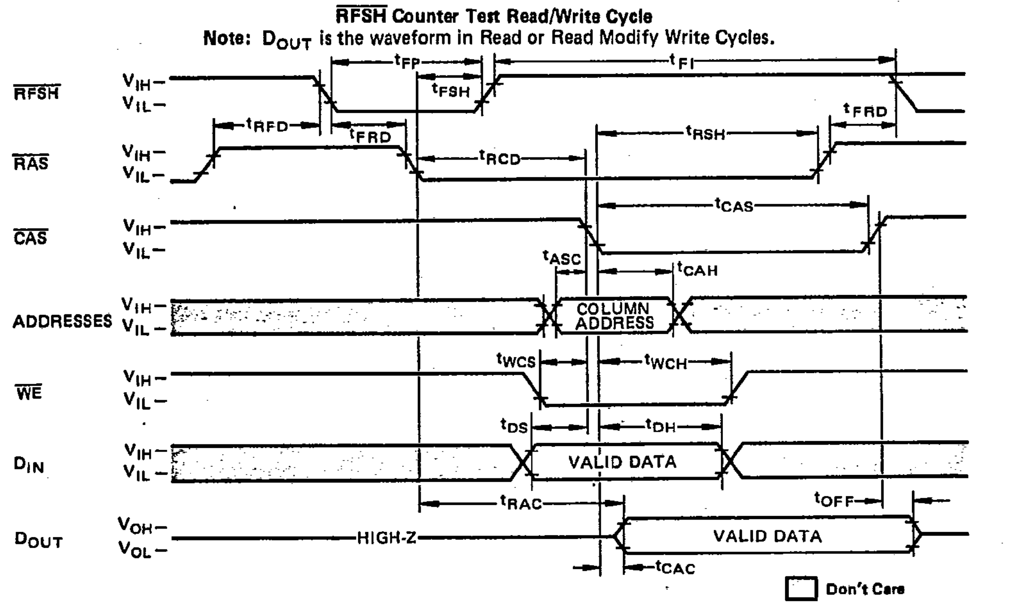

RFSH Refresh Cycle
Note: CAS = VIH, WE, DIN = Don't care
RAS
RFSH
ADDRESSES
DOUT
tRFD
tFP
tFI
tFSR
tFC
tRAH
tASR
ROW ADD.
VIH
VIL
VOH
VOL
HIGH-Z
Don't Care

Hidden $\overline{RAS}$ only Refresh Cycle



Hidden $\overline{RFSH}$ Refresh Cycle





DESCRIPTION

Address Inputs:
A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MB 8265A. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permite triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:
The read mode or write mode is selected with the $\overline{WE}$ input. A high on $\overline{WE}$ selects read mode and low selects write mode. Data input is disabled when read mode is selected.

Data Input:
Data is written into the MB 8265A during a write or read-write cycle. The later falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ can be low after $\overline{CAS}$ has been low and $\overline{CAS}$ to $\overline{WE}$ Delay Time (t_{CWD}) has been satisfied. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:
The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from the falling edge of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high. In a write cycle the indentical sequence occurs, but data is not valid.

Page Mode:
Page-mode operation permits strobing

the row-address into the MB 8265A while maintaining $\overline{RAS}$ at low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the falling edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses (A_0 ~ A_6) at least every two milliseconds. The MB 8265A offers the following three types of refresh.

1) $\overline{RAS}$-only Refresh;
$\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation. During $\overline{RAS}$ only refresh, either V_{IL} or V_{IH} is permitted for A_7.

2) $\overline{RFSH}$ Refresh;
$\overline{RFSH}$ type refreshing available on the MB 8265A offers an alternate refresh method: (1) When $\overline{RFSH}$ is brought low (active) during $\overline{RAS}$ is high (inactive), on-chip refresh control clock generators and a refresh address counter are enabled and an internal refresh operation takes place.
(2) When $\overline{RFSH}$ is brought high (inactive), the internal refresh address counter is automatically incremented in preparation for the next $\overline{RFSH}$ refresh cycle. Only $\overline{RFSH}$ activated cycles affect the internal address counter.
The use of $\overline{RFSH}$ type refreshing eliminates the need of providing any additional external devices to generate refresh addresses. Refer to the Fig. 2 for the example of $\overline{RFSH}$ refresh.

3) Hidden Refresh;
Hidden Refresh Cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read or cycle or read-write.
The MB 8265A offers two types of Hidden Refresh. They are referred to as Hidden $\overline{RAS}$-only Refresh and Hidden $\overline{RFSH}$ Refresh.
A) Hidden $\overline{RAS}$-only Refresh
Hidden $\overline{RAS}$-only Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified percharge period (t_{RP}), executing "$\overline{RAS}$-only" refresh, but with $\overline{CAS}$ held low.
$\overline{RFSH}$ has to be held at V_{IH}.
B) Hidden $\overline{RFSH}$ Refresh
Hidden $\overline{RFSH}$ Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RFD}), executing $\overline{RFSH}$ refresh, but with $\overline{CAS}$ held low.
A specified precharge period (t_{CPN}) is required before normal memory Read, Write or Read-Modify-Write cycle after performing either type of Hidden Refresh.

Refresh Counter Test Cycle:
A special timing sequence provides a convenient method of verifying the functionality of the $\overline{RFSH}$ activated circuitry.

(A) $\overline{RFSH}$ Test Read/Write Cycle:
When $\overline{RFSH}$ is given a signal in timing as shown in timing diagram of $\overline{RFSH}$ counter Test Read/Write Cycle, Read/Write Operation is enabled. A memory cell address (consisting of a row address (8 bits) and a column address (8 bits)) to be accessed can be defined as follows:

*A ROW ADDRESS – Bits A_0 ~ A_6 are defined when contents of the internal address counter are latched. (The other bit A_7 is set low internally.)

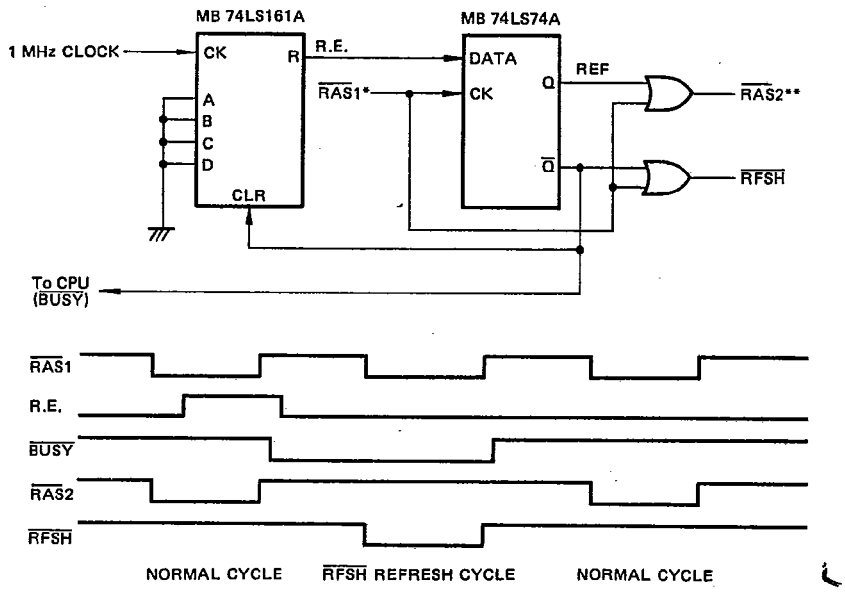
*A COLUMN ADDRESS – All the bits A_0~A_7 are defined by latching levels on A_0~A_7 pins in a high-to-low transition of $\overline{CAS}$.

By using a 15-bit address latched into the on-chip address buffers by means of the above operation, any of 32K (in the fixed half cell array) memory cells can be read/written into/from.

(B) $\overline{RFSH}$ Test Read Modify Wirte Cycle:
Also, Read Modify Write Operation (not only the above normal Read/Write Operations) can be used in this $\overline{RFSH}$ Counter Test Cycle.

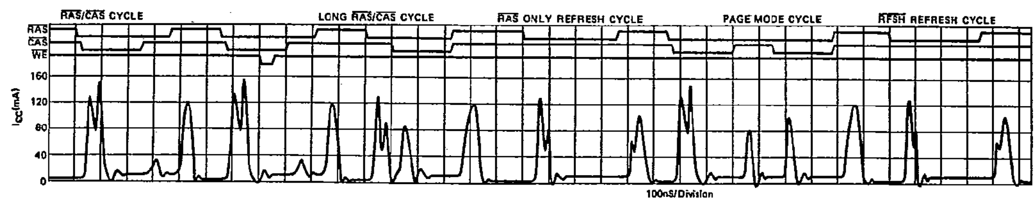
(C) Example of Refresh Counter Test Procedure:
(1) Initialize the internal refresh counter. For this operation, 8 $\overline{RFSH}$ cycles are required.
(2) Write a test pattern of lows into memory cells at a single column address and 128 row addresses by using 128 $\overline{RFSH}$ Test Write Cycle or $\overline{RFSH}$ Test Read Modify Write Cycle.
(3) Verify the data written into the memory cells in the above step (2) by using the column address used in step (2) and sequence through 128 row address combinations (A_0 ~ A_6) by means of normal Read Cycle.
(4) Compliment the test pattern and repeat the steps (2) and (3).

Fig.2 – EXAMPLE OF $\overline{RFSH}$ REFRESH



**If $\overline{RFSH}$ refresh in not used, $\overline{RAS1}$ is connected to $\overline{RAS}$ input.
**$\overline{RAS2}$ should be connected $\overline{RAS}$ input.

Fig.3 – CURRENT WAVE FORM (V_{CC} = 5.5V, T_A = 25°C)



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MB 8265A-15

TYPICAL CHARACTERISTICS CURVES

Fig. 4 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

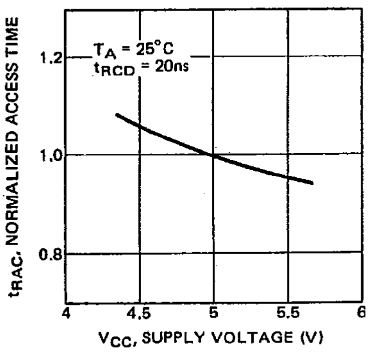

Fig. 5 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

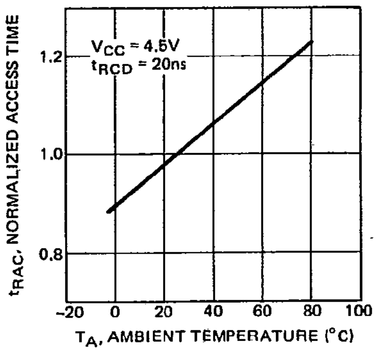

Fig. 6 – OPERATING CURRENT vs CYCLE RATE

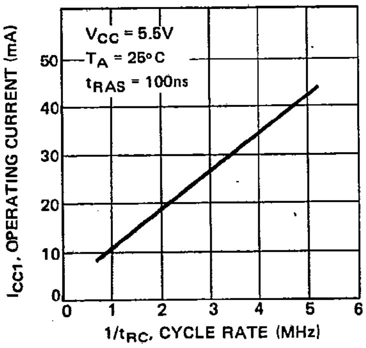

Fig. 7 – OPERATING CURRENT vs SUPPLY VOLTAGE

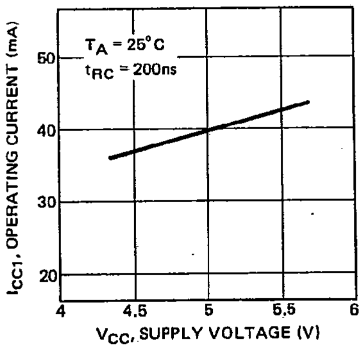

Fig. 8 – OPERATING CURRENT vs AMBIENT TEMPERATURE

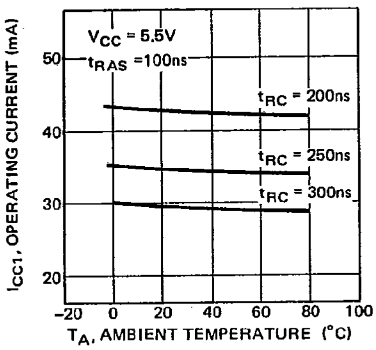

Fig. 9 – STANDBY CURRENT vs SUPPLY VOLTAGE

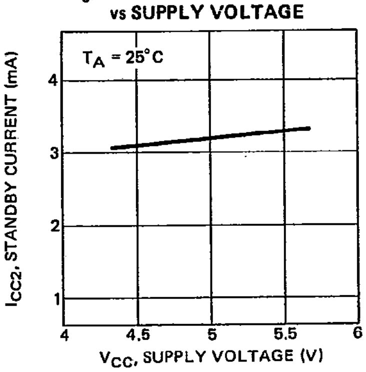

Fig. 10 – STANDBY CURRENT vs AMBIENT TEMPERATURE

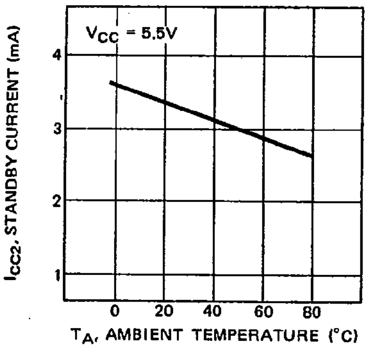

Fig. 11 – REFRESH CURRENT 1 vs CYCLE RATE

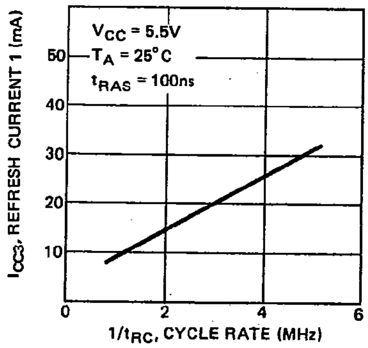

Fig. 12 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

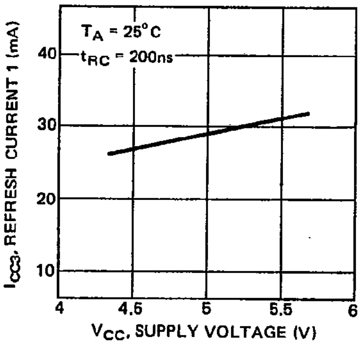

Fig. 13 – REFRESH CURRENT 1 vs AMBIENT TEMPERATURE

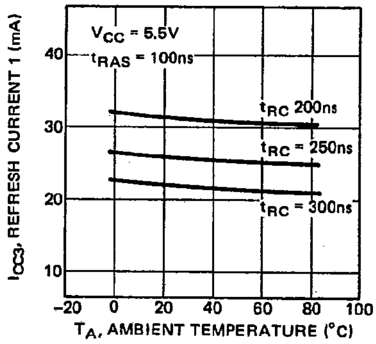

Fig. 14 – PAGE MODE CURRENT vs CYCLE RATE

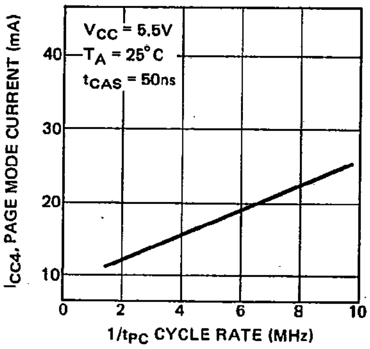

Fig. 15 – PAGE MODE CURRENT vs SUPPLY VOLTAGE

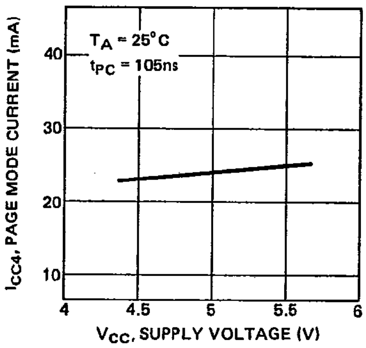

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Fig. 16 — PAGE MODE CURRENT vs AMBIENT TEMPERATURE

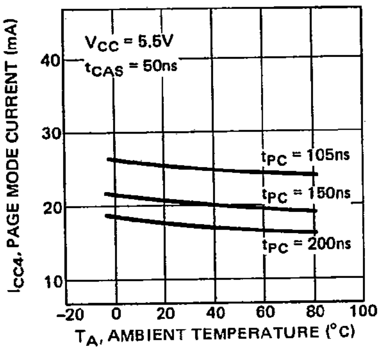


Fig. 17 — REFRESH CURRENT 2 vs CYCLE RATE

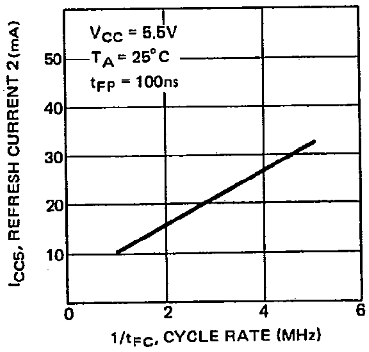


Fig. 18 — REFRESH CURRENT 2 vs SUPPLY VOLTAGE

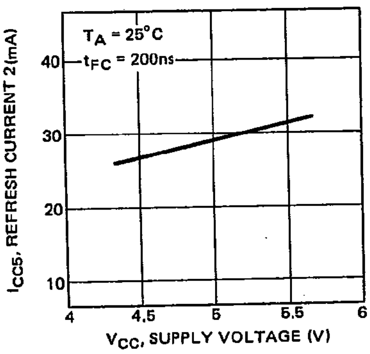


Fig. 19 — REFRESH CURRENT 2 vs AMBIENT TEMPERATURE

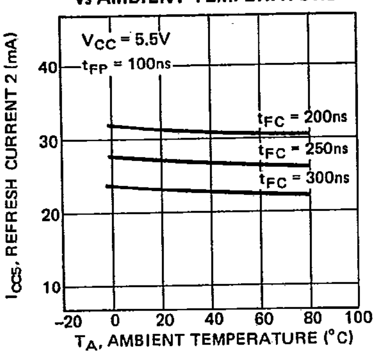


Fig. 20 — ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

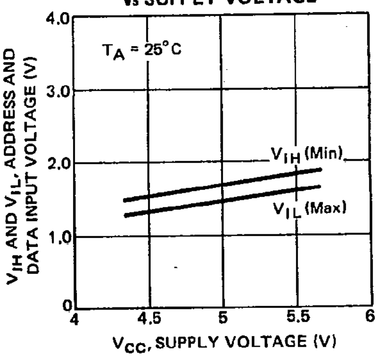


Fig. 21 — ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

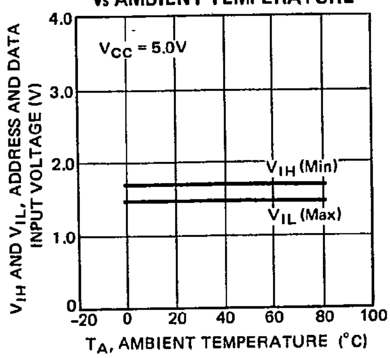


Fig. 22 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

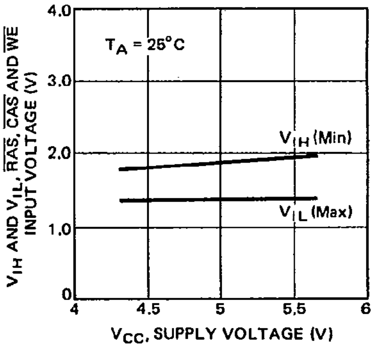


Fig. 23 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ VOLTAGE vs AMBIENT TEMPERATURE

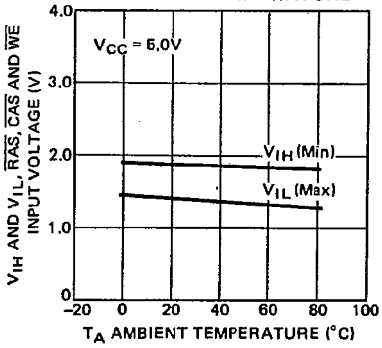


Fig. 24 – CURRENT WAVE FORM DURING POWER UP

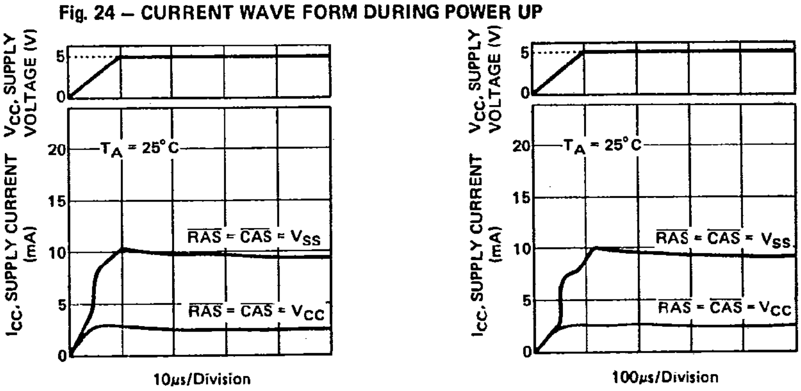


Fig. 25 – CURRENT WAVE FORM DURING POWER UP (ON MEMORY BOARD)

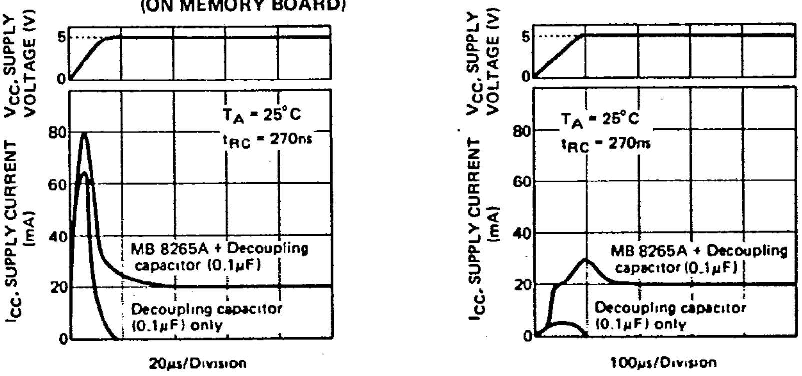
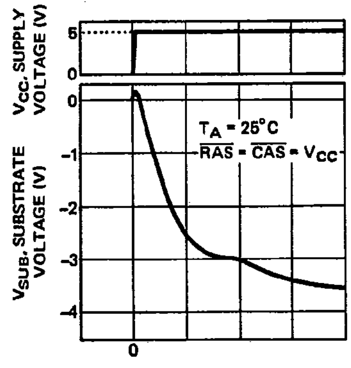
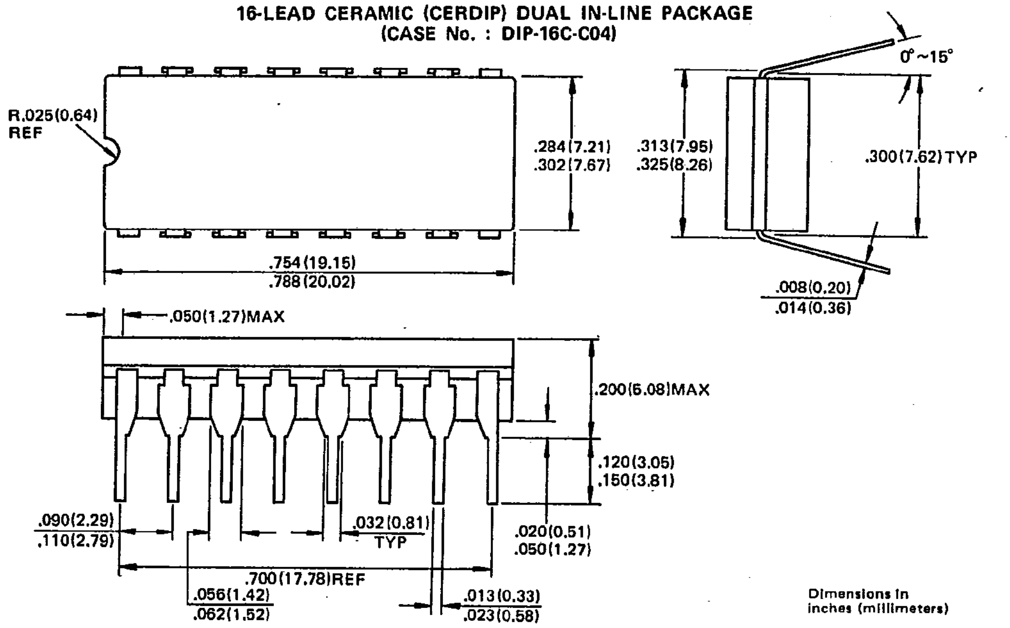


Fig. 26 – SUBSTRATE VOLTATE vs SUPPLY VOLTAGE (DURING POWER UP)



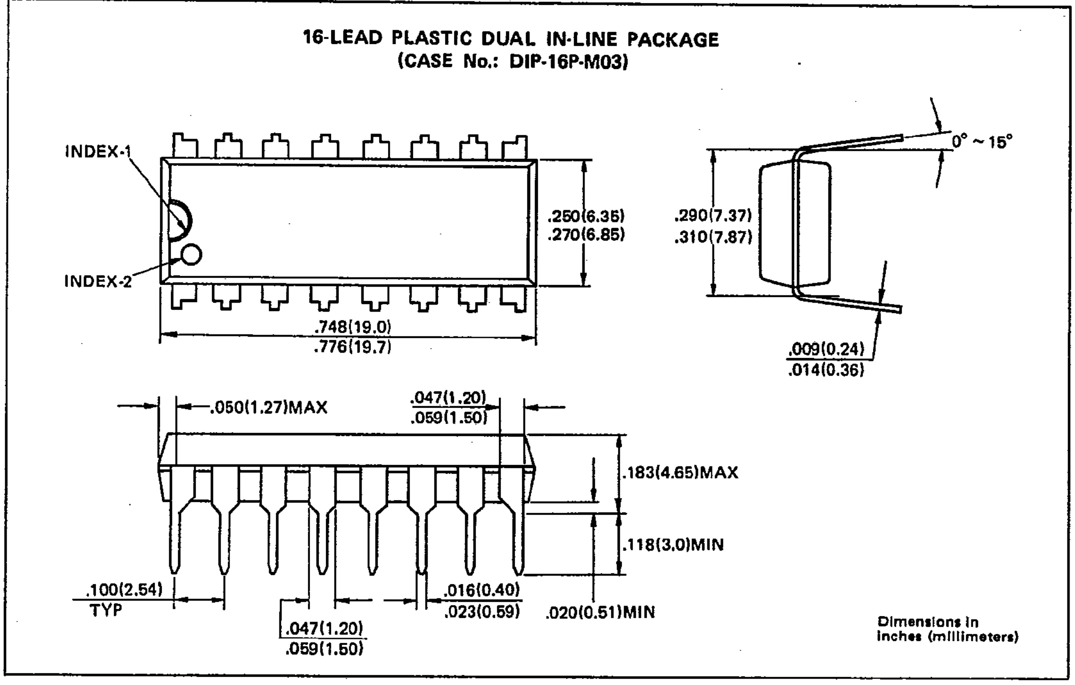
PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Surfix : -Z)



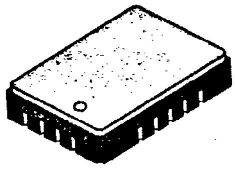
PACKAGE DIMENSIONS

Standard 16-pin Plastic DIP (Surfix : -P)

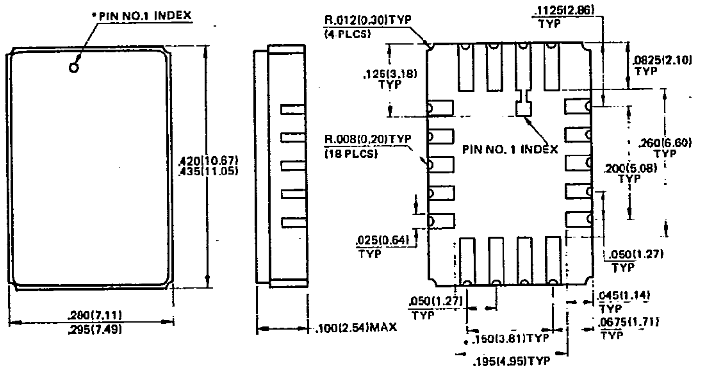


PACKAGE DIMENSIONS

Standard 18-pad Ceramic LCC (Surfix : -TV)



18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-18C-F02)



*Shape of Pin 1 index: Subject to change without notice

Dimensions in inches
(millimeters)