

Section 19 Electrical Specifications

19.1 Absolute Maximum Ratings

Table 19-1 lists the absolute maximum ratings.

Table 19-1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	-0.3 to +7.0	V
Programming voltage	V_{PP}	-0.3 to +13.5	V
Input voltage	V_{in}	-0.3 to $V_{CC} + 0.3$	V
Operating temperature	T_{opr}	Regular specifications: -20 to +75	°C
		Wide-range specifications: -40 to +85	°C
Storage temperature	T_{stg}	-55 to +125	°C

Note: Exceeding the absolute maximum ratings shown in table 19-1 can permanently damage the chip.

19.2 Electrical Characteristics

19.2.1 DC Characteristics

Tables 19-2, 19-3, and 19-4 list the DC characteristics of the 5 V, 4 V, and 3 V versions, respectively. Table 19-5 gives the allowable current output values of the 5 V and 4 V versions, and table 19-6 gives the allowable current output values of the 3 V version. Bus drive characteristics common to the 5 V, 4 V, and 3 V versions are listed in table 19-7.

Table 19-2 DC Characteristics (5 V Version) — Preliminary —

Conditions: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger Input voltage	P7 ₇ , P7 ₅ to P7 ₀ * ³ , FTCl, FTI, TMRI ₀ , TMRI ₁ , TMCI ₀ , TMCI ₁ , VSYNCl, HSYNCl, CSYNCl, FBACKI, KEYIN ₇ to KEYIN ₀	(1) V_T^-	1.0	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.7$		
		$V_T^+ - V_T^-$	0.4	—	—		
Input high voltage	RES, STBY, MD ₁ , MD ₀ , EXTAL, NMI	(2) V_{IH}	$V_{CC} - 0.7$	—	$V_{CC} + 0.3$	V	
	SCL ₀ , SCL ₁ , SDA ₀ , SDA ₁ , P7 ₃ , P7 ₂ (when bus drive function is selected)		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$		
	All input pins other than (1) and (2) above		2.0	—	$V_{CC} + 0.3$		
Input low voltage	RES, STBY, MD ₁ , MD ₀	(3) V_{IL}	-0.3	—	0.5	V	
	SCL ₀ , SCL ₁ , SDA ₀ , SDA ₁ , P7 ₃ , P7 ₂ (when bus drive function is selected)		-0.3	—	1.0		
	All input pins other than (1) and (3) above		-0.3	—	0.8		
Output high voltage	All output pins* ⁴	V_{OH}	$V_{CC} - 0.5$	—	—	V	$I_{OH} = -200 \mu\text{A}$
			3.5	—	—		$I_{OH} = -1.0 \text{ mA}$

Table 19-2 DC Characteristics (5 V Version) (cont) — Preliminary —

Conditions: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
Output low voltage	All output pins* ⁴	V_{OL}	—	0.4	V	$I_{OL} = 1.6 \text{ mA}$	
	P1 ₇ to P1 ₀ , P2 ₇ to P2 ₀ , P3 ₇ to P3 ₀		—	1.0		$I_{OL} = 10.0 \text{ mA}$	
Input leakage current	$\overline{\text{RES}}$	$ I_{in} $	—	10.0	μA	$V_{in} = 0.5 \text{ V}$ to $V_{CC} - 0.5 \text{ V}$	
	$\overline{\text{STBY}}$, $\overline{\text{NMI}}$, MD ₁ , MD ₀		—	1.0			
Leakage current in three-state (off state)	Ports 1 to 7	$ I_{TSL} $	—	1.0	μA	$V_{in} = 0.5 \text{ V}$ to $V_{CC} - 0.5 \text{ V}$	
Input pull-up MOS current	Ports 1 to 3	$-I_p$	30	—	250	μA	$V_{in} = 0 \text{ V}$
	P7 ₃ to P7 ₀ , P6 ₃ to P6 ₀		60	—	500		
Input capacitance	$\overline{\text{RES}}$ (4)	C_{in}	—	—	60	pF	$V_{in} = 0 \text{ V}$, $f = 1 \text{ MHz}$, $T_a = 25^\circ\text{C}$
	$\overline{\text{NMI}}$		—	—	50		
	P7 ₃ to P7 ₀		—	—	20		
	All input pins other than (4)		—	—	15		
Current dissipation* ¹	Normal operation	I_{CC}	—	27	45	mA	$f = 12 \text{ MHz}$
			—	36	60		$f = 16 \text{ MHz}$
	Sleep mode		—	18	30		$f = 12 \text{ MHz}$
			—	24	40		$f = 16 \text{ MHz}$
	Standby modes* ²		—	0.01	5.0	μA	$T_a \leq 50^\circ\text{C}$
			—	—	20.0		$50^\circ\text{C} < T_a$
RAM standby voltage	V_{RAM}	2.0	—	—	V		

Notes: 1. Value when $V_{IH \text{ min}} = V_{CC} - 0.5 \text{ V}$, $V_{IL \text{ max}} = 0.5 \text{ V}$, all output pins are unloaded, and input MOS pull-ups are off.

2. Value when $V_{RAM} \leq V_{CC} < 4.5 \text{ V}$, $V_{IH \text{ min}} = V_{CC} \times 0.9$ and $V_{IL \text{ max}} = 0.3 \text{ V}$.

3. P7₇ and P7₅ to P7₀ do not include SCL₀, SDA₀, SCL₁, SDA₁, HA₀, $\overline{\text{IOW}}$, $\overline{\text{CS}}_1$, and WAIT.

4. When IICS = ICE = 0. The output low level when the bus drive function is selected with P7₃, P7₂, SDA₁, SCL₁, SDA₀, and SCL₀ is determined separately.

Table 19-3 DC Characteristics (4 V Version) — Preliminary —

Conditions: $V_{CC} = 4.0 \text{ V to } 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
Schmitt trigger input voltage	P7 ₇ , P7 ₅ to P7 ₀ * ³ , FTCl, FTI, TMRI ₀ , TMRI ₁ , TMCI ₀ , TMCI ₁ , VSYNCl, HSYNCl, CSYNCl, FBACKI, KEYIN ₇ to KEYIN ₀	(1) V_T^-	1.0	—	—	V	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$
		V_T^+	—	—	$V_{CC} \times 0.7$		
		$V_T^+ - V_T^-$	0.4	—	—		
		V_T^-	0.8	—	—		$V_{CC} = 4.0 \text{ V to } 4.5 \text{ V}$
		V_T^+	—	—	$V_{CC} \times 0.7$		
		$V_T^+ - V_T^-$	0.3	—	—		
Input high voltage	RES, STBY, MD ₁ , MD ₀ , EXTAL, NMI	(2) V_{IH}	$V_{CC} - 0.7$	—	$V_{CC} + 0.3$	V	
	SCL ₀ , SCL ₁ , SDA ₀ , SDA ₁ , P7 ₃ , P7 ₂ (when bus drive function is selected)		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$		
	All input pins other than (1) and (2) above		2.0	—	$V_{CC} + 0.3$		
Input low voltage	RES, STBY, MD ₁ , MD ₀	(3) V_{IL}	-0.3	—	0.5	V	
	SCL ₀ , SCL ₁ , SDA ₀ , SDA ₁ , P7 ₃ , P7 ₂ (when bus drive function is selected)		-0.3	—	1.0		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$
			-0.3	—	0.8		$V_{CC} = 4.0 \text{ V to } 4.5 \text{ V}$
	All input pins other than (1) and (3) above		-0.3	—	0.8		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$
			-0.3	—	0.6		$V_{CC} = 4.0 \text{ V to } 4.5 \text{ V}$

Table 19-3 DC Characteristics (4 V Version) (cont) — Preliminary —

Conditions: $V_{CC} = 4.0\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Output high voltage	All output pins*4	V_{OH}	$V_{CC} - 0.5$	—	—	V	$I_{OH} = -200\ \mu\text{A}$
			3.5	—	—		$I_{OH} = -1.0\ \text{mA}$, $V_{CC} = 4.5\ \text{V to }5.5\ \text{V}$
			2.8	—	—		$I_{OH} = -1.0\ \text{mA}$, $V_{CC} = 4.0\ \text{V to }4.5\ \text{V}$
Output low voltage	All output pins*4	V_{OL}	—	—	0.4	V	$I_{OL} = 1.6\ \text{mA}$
			—	—	1.0		$I_{OL} = 10.0\ \text{mA}$
Input leakage current	$\overline{\text{RES}}$	$ I_{in} $	—	—	10.0	μA	$V_{in} = 0.5\ \text{V to }V_{CC} - 0.5\ \text{V}$
	$\overline{\text{STBY}}$, $\overline{\text{NMI}}$, MD_1 , MD_0		—	—	1.0		
Leakage current in three-state (off state)	Ports 1 to 7	$ I_{TSL} $	—	—	1.0	μA	$V_{in} = 0.5\ \text{V to }V_{CC} - 0.5\ \text{V}$
Input pull-up MOS current	Ports 1 to 3	$-I_p$	30	—	250	μA	$V_{in} = 0\ \text{V}$, $V_{CC} = 4.5\ \text{V to }5.5\ \text{V}$
	P7_3 to P7_0 , P6_3 to P6_0		60	—	500		
	Ports 1 to 3		20	—	200		
	P7_3 to P7_0 , P6_3 to P6_0		40	—	400		
Input capacitance	$\overline{\text{RES}}$	(4) C_{in}	—	—	60	pF	$V_{in} = 0\ \text{V}$, $f = 1\ \text{MHz}$, $T_a = 25^\circ\text{C}$
	$\overline{\text{NMI}}$		—	—	50		
	P7_3 to P7_0		—	—	20		
	All input pins other than (4)		—	—	15		

Table 19-3 DC Characteristics (4 V Version) (cont) — Preliminary —

Conditions: $V_{CC} = 4.0 \text{ V to } 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	
Current dissipation* ¹	Normal operation	I_{CC}	—	27	45	mA	$f = 12 \text{ MHz}$	
			—	36	60		$f = 16 \text{ MHz}$, $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	
	Sleep mode		—	18	30		$f = 12 \text{ MHz}$	
			—	24	40		$f = 16 \text{ MHz}$, $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	
	Standby modes* ²			—	0.01	5.0	μA	$T_a \leq 50^\circ\text{C}$
				—	—	20.0		$50^\circ\text{C} < T_a$
RAM standby voltage		V_{RAM}	2.0	—	—	V		

- Notes: 1. Value when $V_{IH \text{ min}} = V_{CC} - 0.5 \text{ V}$, $V_{IL \text{ max}} = 0.5 \text{ V}$, all output pins are unloaded, and input MOS pull-ups are off.
2. Value when $V_{RAM} \leq V_{CC} < 4.0 \text{ V}$, $V_{IH \text{ min}} = V_{CC} \times 0.9$ and $V_{IL \text{ max}} = 0.3 \text{ V}$.
3. P7₇ and P7₅ to P7₀ do not include SCL₀, SDA₀, SCL₁, SDA₁, HA₀, $\overline{\text{IOW}}$, $\overline{\text{CS}}_1$, and $\overline{\text{WAIT}}$.
4. When IICS = ICE = 0. The output low level when the bus drive function is selected with P7₃, P7₂, SDA₁, SCL₁, SDA₀, and SCL₀ is determined separately.

Table 19-4 DC Characteristics (3 V Version) — Preliminary —

Conditions: $V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	P7 ₇ , P7 ₅ to P7 ₀ * ³ , FTCl, FTI, TMRI ₀ , TMRI ₁ , TMCl ₀ , TMCl ₁ , VSYNCI, HSYNCI, CSYNCI, FBACKI, KEYIN ₇ to KEYIN ₀	(1) V_T^-	$V_{CC} \times 0.15$	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.7$		
		$V_T^+ - V_T^-$	0.2	—	—		
Input high voltage	RES, $\overline{\text{STBY}}$, MD ₁ , MD ₀ , $\overline{\text{EXTAL}}$, $\overline{\text{NMI}}$ SCL ₀ , SCL ₁ , SDA ₀ , SDA ₁ , P7 ₃ , P7 ₂ (when bus drive function is selected) All input pins other than (1) and (2) above	(2) V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V	
			$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$		
			$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$		
Input low voltage	RES, $\overline{\text{STBY}}$, MD ₁ , MD ₀ SCL ₀ , SCL ₁ , SDA ₀ , SDA ₁ , P7 ₃ , P7 ₂ (when bus drive function is selected) All input pins other than (1) and (3) above	(3) V_{IL}	-0.3	—	$V_{CC} \times 0.1$	V	
			-0.3	—	$V_{CC} \times 0.15$		
			-0.3	—	$V_{CC} \times 0.15$		
Output high voltage	All output pins* ⁴	V_{OH}	$V_{CC} - 0.5$	—	—	V	$I_{OH} = -200 \mu\text{A}$
			$V_{CC} - 1.0$	—	—		$I_{OH} = -1.0 \text{ mA}$

Table 19-4 DC Characteristics (3 V Version) (cont) — Preliminary —
 Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
Output low voltage	All output pins*4	V_{OL}	—	—	0.4	V	$I_{OL} = 0.8\text{ mA}$
	P1 ₇ to P1 ₀ , P2 ₇ to P2 ₀ , P3 ₇ to P3 ₀		—	—	0.4		$I_{OL} = 1.6\text{ mA}$
Input leakage current	RES	$ I_{in} $	—	—	10.0	μA	$V_{in} = 0.5\text{ V to }V_{CC} - 0.5\text{ V}$
	STBY, NMI, MD ₁ , MD ₀		—	—	1.0		
Leakage current in three-state (off state)	Ports 1 to 7	$ I_{TSL} $	—	—	1.0	μA	$V_{in} = 0.5\text{ V to }V_{CC} - 0.5\text{ V}$
Input pull-up MOS current	Ports 1 to 3	$-I_p$	3	—	120	μA	$V_{in} = 0\text{ V}$, $V_{CC} = 2.7\text{ V to }4.0\text{ V}$
	P7 ₃ to P7 ₀ , P6 ₃ to P6 ₀		30	—	250		
Input capacitance	RES	(4) C_{in}	—	—	60	pF	$V_{in} = 0\text{ V}$, $f = 1\text{ MHz}$, $T_a = 25^\circ\text{C}$
	NMI		—	—	50		
	P7 ₃ to P7 ₀		—	—	20		
	All input pins other than (4)		—	—	15		

Table 19-4 DC Characteristics (3 V Version) (cont) — Preliminary —
 Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Current dissipation*1	Normal operation	I_{CC}	—	7	—	mA	f = 6 MHz, $V_{CC} = 2.7\text{ V to }3.6\text{ V}$
			—	12	22		f = 10 MHz, $V_{CC} = 2.7\text{ V to }3.6\text{ V}$
			—	25	—		f = 10 MHz, $V_{CC} = 4.0\text{ V to }5.5\text{ V}$
	Sleep mode		—	5	—		f = 6 MHz, $V_{CC} = 2.7\text{ V to }3.6\text{ V}$
			—	9	16		f = 10 MHz, $V_{CC} = 2.7\text{ V to }3.6\text{ V}$
			—	18	—		f = 10 MHz, $V_{CC} = 4.0\text{ V to }5.5\text{ V}$
	Standby modes*2		—	0.01	5.0	μA	$T_a \leq 50^\circ\text{C}$
			—	—	20.0		$50^\circ\text{C} < T_a$
	RAM standby voltage		V_{RAM}	2.0	—	—	V

- Notes: 1. Value when $V_{IH\ min} = V_{CC} - 0.5\text{ V}$, $V_{IL\ max} = 0.5\text{ V}$, all output pins are unloaded, and input MOS pull-ups are off.
2. Value when $V_{RAM} \leq V_{CC} < 2.7\text{ V}$, $V_{IH\ min} = V_{CC} \times 0.9$ and $V_{IL\ max} = 0.3\text{ V}$.
3. P7₇ and P7₅ to P7₀ do not include SCL₀, SDA₀, SCL₁, SDA₁, HA₀, $\overline{\text{IOW}}$, $\overline{\text{CS}}_1$, and WAIT.
4. When IICS = ICE = 0. The output low level when the bus drive function is selected with P7₃, P7₂, SDA₁, SCL₁, SDA₀, and SCL₀ is determined separately.

**Table 19-5 Allowable Output Current Values — Preliminary —
(5 V and 4 V Versions)**

Conditions: $V_{CC} = 4.0\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Allowable output low current (per pin)	SCL ₀ , SCL ₁ , SDA ₀ , SDA ₁ , P7 ₂ , P7 ₃ (when bus drive function is selected)	I _{OL}	—	—	20	mA
	Ports 1, 2 and 3		—	—	10	
	Other output pins		—	—	2	
Allowable output low current (total)	Ports 1, 2 and 3 total	ΣI _{OL}	—	—	80	mA
	Total of all output		—	—	120	
Allowable output high current (per pin)	All output pins	-I _{OH}	—	—	2	mA
Allowable output high current (total)	Total of all output	Σ-I _{OH}	—	—	40	mA

Table 19-6 Allowable Output Current Values (3 V Version) — Preliminary —

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$

Item		Symbol	Min	Typ	Max	Unit
Allowable output low current (per pin)	SCL ₀ , SCL ₁ , SDA ₀ , SDA ₁ , P7 ₂ , P7 ₃ (when bus drive function is selected)	I _{OL}	—	—	10	mA
	Ports 1, 2 and 3		—	—	2	
	Other output pins		—	—	1	
Allowable output low current (total)	Ports 1, 2 and 3 total	ΣI _{OL}	—	—	40	mA
	Total of all output		—	—	60	
Allowable output high current (per pin)	All output pins	-I _{OH}	—	—	2	mA
Allowable output high current (total)	Total of all output	Σ-I _{OH}	—	—	30	mA

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current values in tables 19-5 and 19-6. In particular, when driving a Darlington transistor or

LED directly, be sure to insert a current-limiting resistor in the output path. See figures 19-1 and 19-2.

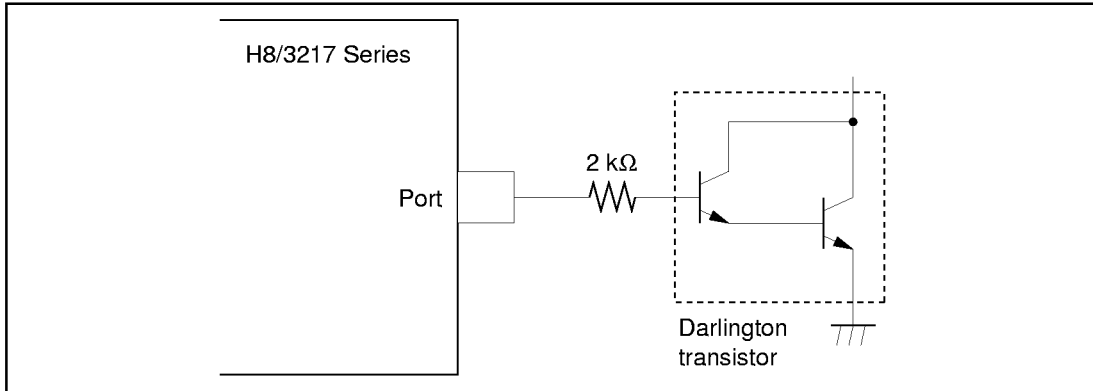


Figure 19-1 Example of Circuit for Driving a Darlington Transistor (5 V Version)

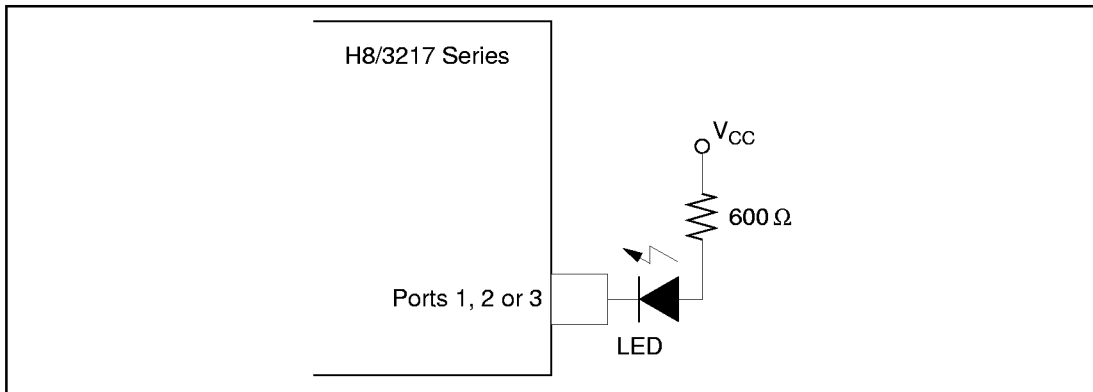


Figure 19-2 Example of Circuit for Driving an LED (5 V Version)

Table 19-7 Bus Drive Characteristics — Preliminary —Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Output low voltage	SCL ₀ , SCL ₁ , SDA ₀ , SDA ₁ , P7 ₂ , P7 ₃ (when bus drive function is selected)	—	—	0.5	V	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OL} = 16\text{ mA}$
		—	—	0.5		$V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $I_{OL} = 8\text{ mA}$

19.2.2 AC Characteristics

The AC characteristics are listed in five tables. Bus timing parameters are given in table 19-8, control signal timing parameters in table 19-9, timing parameters of the on-chip supporting modules in table 19-10, I²C bus interface timing parameters in table 19-11, and External Clock Output Settling Delay Time in table 19-12.

Table 19-8 Bus Timing — Preliminary —

Condition A: $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$, $\phi = 2.0 \text{ MHz}$ to maximum operating frequency, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Condition B: $V_{CC} = 4.0 \text{ V to } 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$, $\phi = 2.0 \text{ MHz}$ to maximum operating frequency, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$, $\phi = 2.0 \text{ MHz}$ to maximum operating frequency, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$

Item	Symbol	Condition C		Condition B		Condition A		Unit	Test Conditions
		10 MHz		12 MHz		16 MHz			
		Min	Max	Min	Max	Min	Max		
Clock cycle time	t_{cyc}	100	500	83.3	500	62.5	500	ns	Fig. 19-4
Clock pulse width low	t_{CL}	30	—	30	—	20	—		
Clock pulse width high	t_{CH}	30	—	30	—	20	—		
Clock rise time	t_{Cr}	—	20	—	10	—	10		
Clock fall time	t_{Cf}	—	20	—	10	—	10		
Address delay time	t_{AD}	—	50	—	35	—	30		
Address hold time	t_{AH}	20	—	15	—	10	—		
Address strobe delay time	t_{ASD}	—	50	—	35	—	30		
Write strobe delay time	t_{WSD}	—	50	—	35	—	30		
Strobe delay time	t_{SD}	—	50	—	35	—	30		
Write strobe pulse width*	t_{WSW}	110	—	90	—	60	—		
Address setup time 1*	t_{AS1}	15	—	10	—	10	—		
Address setup time 2*	t_{AS2}	65	—	50	—	40	—		
Read data setup time	t_{RDS}	35	—	20	—	20	—		
Read data hold time*	t_{RDH}	0	—	0	—	0	—		
Read data access time*	t_{ACC}	—	170	—	160	—	110		
Write data delay time	t_{WDD}	—	75	—	60	—	60		
Write data setup time	t_{WDS}	5	—	5	—	5	—		
Write data hold time	t_{WDH}	20	—	20	—	20	—		
Wait setup time	t_{WTS}	40	—	35	—	30	—		Fig. 19-5
Wait hold time	t_{WTH}	10	—	10	—	10	—		

Note: * Values at maximum operating frequency

Table 19-9 Control Signal Timing — Preliminary —

Condition A: $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $\phi = 2.0\text{ MHz}$ to maximum operating frequency, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition B: $V_{CC} = 4.0\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $\phi = 2.0\text{ MHz}$ to maximum operating frequency, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $\phi = 2.0\text{ MHz}$ to maximum operating frequency, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$

Item	Symbol	Condition C		Condition B		Condition A		Unit	Test Conditions
		10 MHz	12 MHz	12 MHz	16 MHz	16 MHz			
RES setup time	t_{RESS}	300	—	200	—	200	—	ns	Fig. 19-6
RES pulse width	t_{RESW}	10	—	10	—	10	—	t_{cyc}	
NMI setup time (NMI, $\overline{IRQ_0}$ to $\overline{IRQ_2}$, $\overline{IRQ_6}$)	t_{NMIS}	300	—	150	—	150	—	ns	Fig. 19-7
NMI hold time (NMI, $\overline{IRQ_0}$ to $\overline{IRQ_2}$, $\overline{IRQ_6}$)	t_{NMIH}	10	—	10	—	10	—		
Interrupt pulse width for recovery from software standby mode (NMI, $\overline{IRQ_0}$ to $\overline{IRQ_2}$, $\overline{IRQ_6}$)	t_{NMIW}	300	—	200	—	200	—		
Crystal oscillator settling time (reset)	t_{OSC1}	20	—	20	—	20	—	ms	Fig. 19-8
Crystal oscillator settling time (software standby)	t_{OSC2}	8	—	8	—	8	—		Fig. 19-9

Measurement Conditions for AC Characteristics

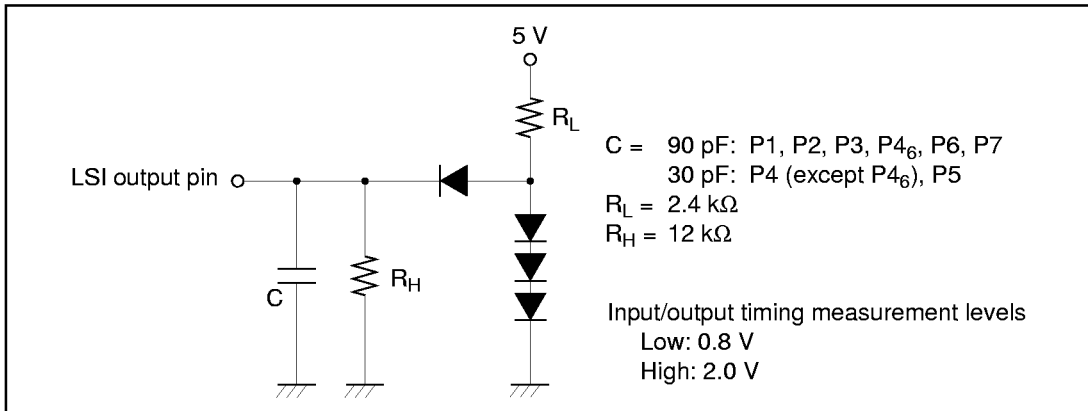


Figure 19-3 Test Conditions for AC Characteristics

Table 19-10 Timing Conditions of On-Chip Supporting Modules — Preliminary —

Condition A: $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $\phi = 2.0\text{ MHz}$ to maximum operating frequency, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition B: $V_{CC} = 4.0\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $\phi = 2.0\text{ MHz}$ to maximum operating frequency, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $\phi = 2.0\text{ MHz}$ to maximum operating frequency, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$

Item	Symbol	Condition C		Condition B		Condition A		Unit	Test Conditions	
		10 MHz		12 MHz		16 MHz				
		Min	Max	Min	Max	Min	Max			
FRT	Timer output delay time	t_{FTOD}	—	150	—	100	—	100	ns	Fig. 19-10
	Timer input setup time	t_{FTIS}	80	—	50	—	50	—		
	Timer clock input setup time	t_{FTCS}	80	—	50	—	50	—		Fig. 19-11
	Timer clock pulse width	t_{FTCWH} t_{FTCWL}	1.5	—	1.5	—	1.5	—	t_{cyc}	
TMR	Timer output delay time	t_{TMOD}	—	150	—	100	—	100	ns	Fig. 19-12
	Timer reset input setup time	t_{TMRS}	80	—	50	—	50	—		Fig. 19-14
	Timer clock input setup time	t_{TMCS}	80	—	50	—	50	—		Fig. 19-13
	Timer clock pulse width (single edge)	t_{TMCWH} t_{TMCWL}	1.5	—	1.5	—	1.5	—	t_{cyc}	
	Timer clock pulse width (both edges)		2.5	—	2.5	—	2.5	—		
PWM	Timer output delay time	t_{PWOD}	—	150	—	100	—	100	ns	Fig. 19-15
SCI	Input clock cycle	(Async) t_{Scyc} (Sync)	4 6	—	4 6	—	4 6	—	t_{cyc}	Fig. 19-16
	Transmit data delay time (Sync)	t_{TXD}	—	200	—	100	—	100	ns	
	Receive data setup time (Sync)	t_{RXS}	150	—	100	—	100	—		
	Receive data hold time (Sync)	t_{RXH}	150	—	100	—	100	—		
	Input clock pulse width	t_{SCKW}	0.4	0.6	0.4	0.6	0.4	0.6	t_{Scyc}	Fig. 19-17

Table 19-10 Timing Conditions of On-Chip Supporting Modules (cont) — Preliminary

Condition A: $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $\phi = 2.0\text{ MHz}$ to maximum operating frequency, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition B: $V_{CC} = 4.0\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $\phi = 2.0\text{ MHz}$ to maximum operating frequency, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $\phi = 2.0\text{ MHz}$ to maximum operating frequency, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$

Item	Symbol	Condition C		Condition B		Condition A		Unit	Test Conditions	
		10 MHz	12 MHz	16 MHz	16 MHz	16 MHz				
PORT	Output data delay time	t_{PWD}	—	150	—	100	—	100	ns	Fig. 19-18
	Input data setup time	t_{PRS}	80	—	50	—	50	—		
	Input data hold time	t_{PRH}	80	—	50	—	50	—		
HIF read cycle	\overline{CS}/HA_0 setup time	t_{HAR}	10	—	10	—	10	—	ns	Fig. 19-19
	\overline{CS}/HA_0 hold time	t_{HRA}	10	—	10	—	10	—		
	$\overline{IO\overline{R}}$ pulse width	t_{HRPW}	220	—	120	—	120	—		
	HDB delay time	t_{HRD}	—	200	—	100	—	100		
	HDB hold time	t_{HRF}	0	40	0	25	0	25		
	HIRQ delay time	t_{HIRQ}	—	200	—	120	—	120		
HIF write cycle	\overline{CS}/HA_0 setup time	t_{HAW}	10	—	10	—	10	—	ns	Fig. 19-20
	\overline{CS}/HA_0 hold time	t_{HWA}	10	—	10	—	10	—		
	$\overline{IO\overline{W}}$ pulse width	t_{HWPW}	100	—	60	—	60	—		
	HDB setup time	t_{HDW}	50	—	30	—	30	—		
	HDB hold time	t_{HWD}	25	—	15	—	15	—		
	GA_{20} delay time	t_{HGA}	—	180	—	90	—	90		

Table 19-11 I²C Bus Timing — Preliminary —Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20^{\circ}\text{C to }+75^{\circ}\text{C}$

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
SCL clock cycle time	t_{SCL}	$12t_{cyc}$	—	—	ns		Fig. 19-21
SCL clock high pulse width	t_{SCLH}	$3t_{cyc}$	—	—	ns		
SCL clock low pulse width	t_{SCLL}	$5t_{cyc}$	—	—	ns		
SCL, SDA rise time	t_{Sr}	—	—	1000	ns	Normal mode 100 kbits/s (max)	
		$20 + 0.1C_b$	—	300		High-speed mode 400 kbits/s (max)	
SCL, SDA fall time	t_{Sf}	—	—	300	ns	Normal mode 100 kbits/s (max)	
		$20 + 0.1C_b$	—	300		High-speed mode 400 kbits/s (max)	
SDA bus free time	t_{BUF}	$7t_{cyc} - 300$	—	—	ns		
SCL start condition hold time	t_{STAH}	$3t_{cyc}$	—	—	ns		
SCL resend start condition setup time	t_{STAS}	$3t_{cyc}$	—	—	ns		
SDA stop condition setup time	t_{STOS}	$3t_{cyc}$	—	—	ns		
SDA data setup time	t_{SDAS}	$1t_{cyc} + 10$	—	—	ns		
SDA data hold time	t_{SDAH}	0	—	—	ns		
SDA load capacitance	C_b	—	—	400	pF		

Table 19-12 External Clock Output Settling Delay Time — Preliminary —
 Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -40^\circ\text{C to }+85^\circ\text{C}$

Item	Symbol	Min	Max	Unit	Notes
External clock output settling delay time	t_{DEXT}^*	500	—	μs	Figure 19-22

Note: * t_{DEXT} includes a $10 t_{cyc} \overline{\text{RES}}$ pulse width (t_{RESW}).

19.3 MCU Operational Timing

This section provides the following timing charts:

19.3.1	Bus Timing	Figures 19-4 and 19-5
19.3.2	Control Signal Timing	Figures 19-6 to 19-9
19.3.3	16-Bit Free-Running Timer Timing	Figures 19-10 and 19-11
19.3.4	8-Bit Timer Timing	Figures 19-12 to 19-14
19.3.5	Pulse Width Modulation Timer Timing	Figure 19-15
19.3.6	Serial Communication Interface Timing	Figures 19-16 and 19-17
19.3.7	I/O Port Timing	Figure 19-18
19.3.8	Host Interface Timing	Figure 19-19 and 19-20
19.3.9	I ² C Bus Interface Timing (Option)	Figure 19-21
19.3.10	External Clock Output Timing	Figure 19-22

19.3.1 Bus Timing

(1) Basic Bus Cycle (without Wait States) in Expanded Modes

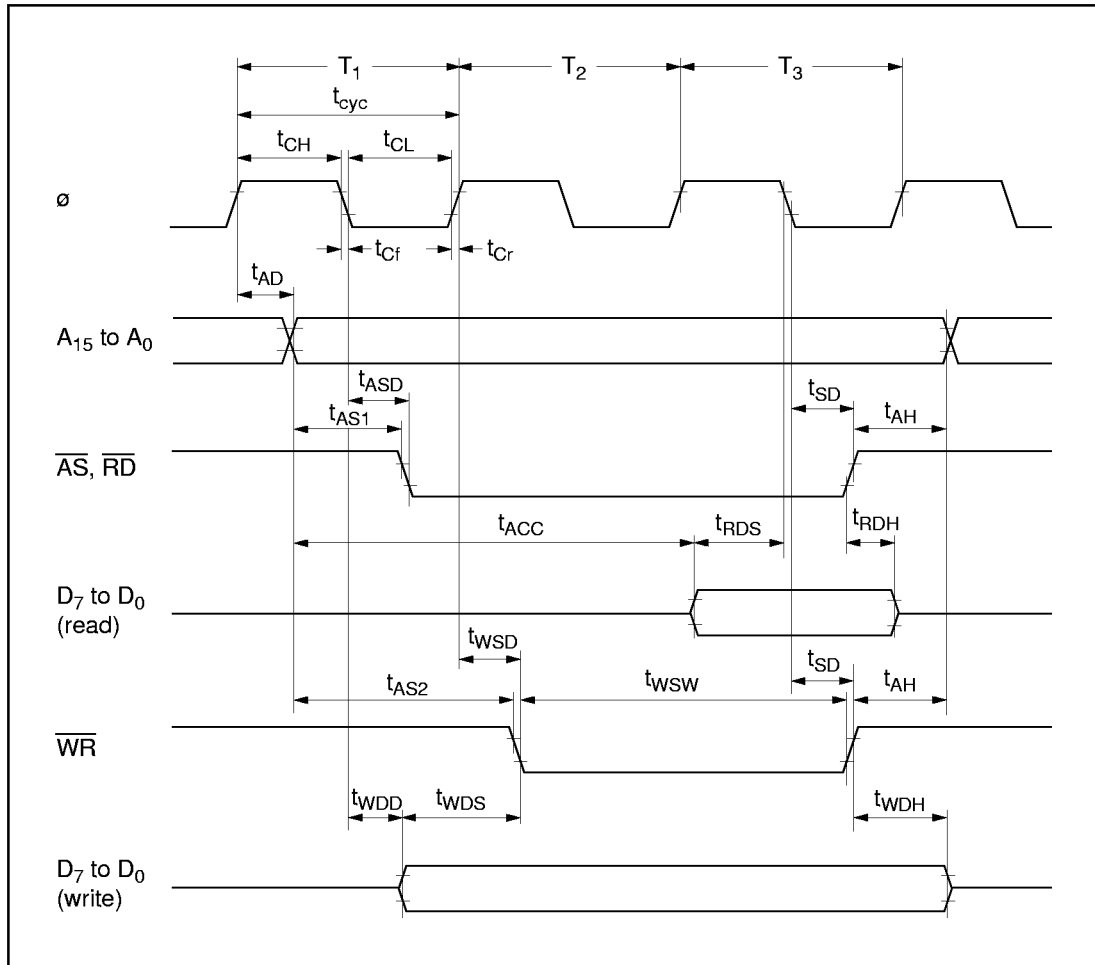


Figure 19-4 Basic Bus Cycle (without Wait States) in Expanded Modes

(2) Basic Bus Cycle (with 1 Wait State) in Expanded Modes

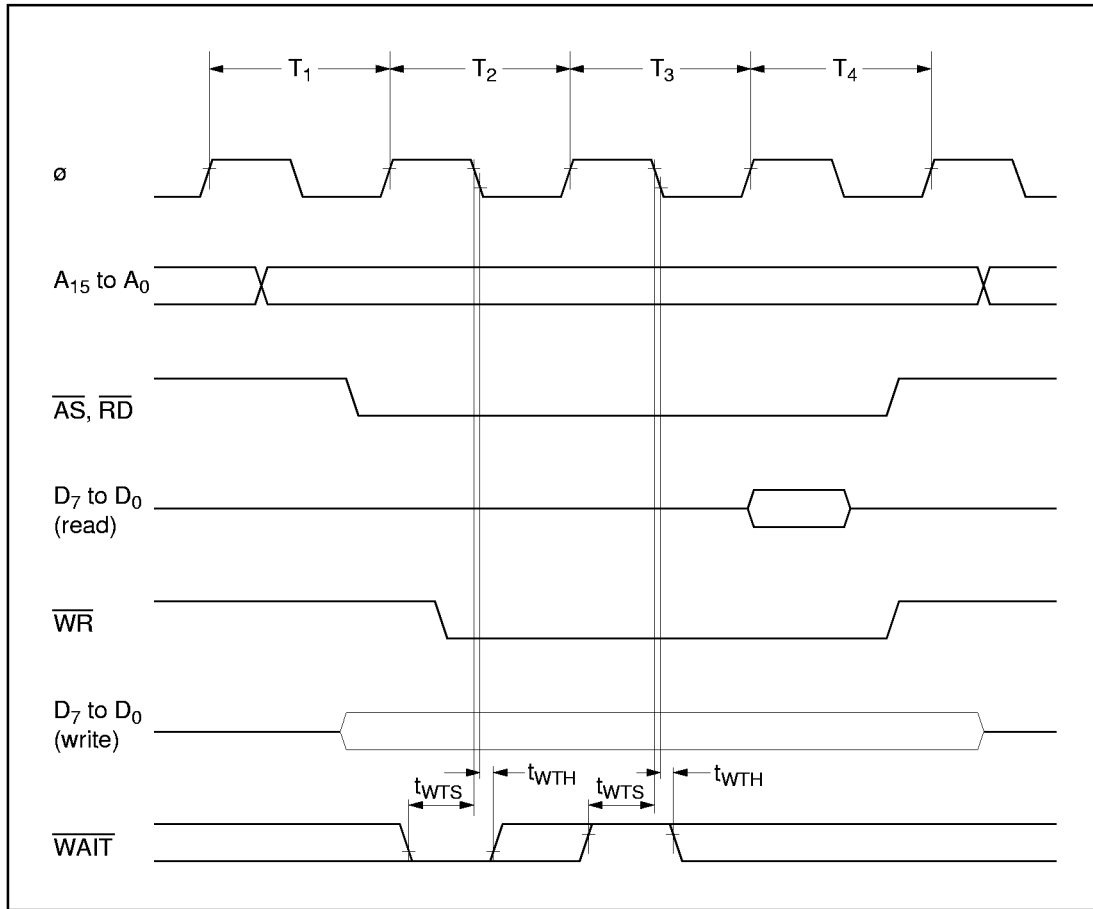


Figure 19-5 Basic Bus Cycle (with 1 Wait State) in Expanded Modes

19.3.2 Control Signal Timing

(1) Reset Input Timing

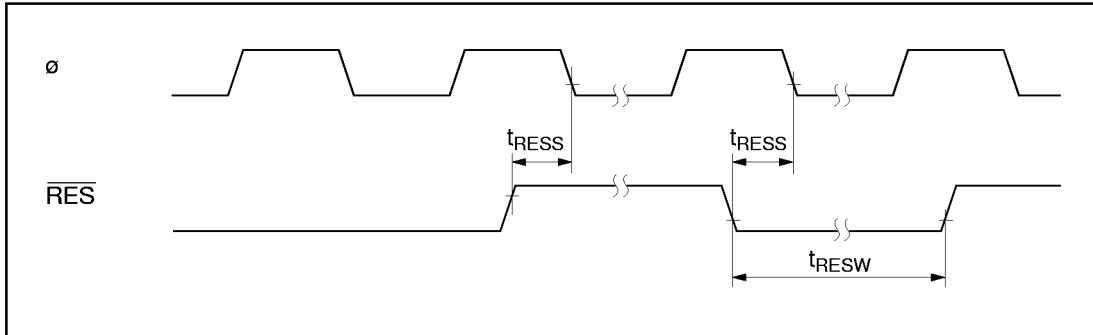


Figure 19-6 Reset Input Timing

(2) Interrupt Input Timing

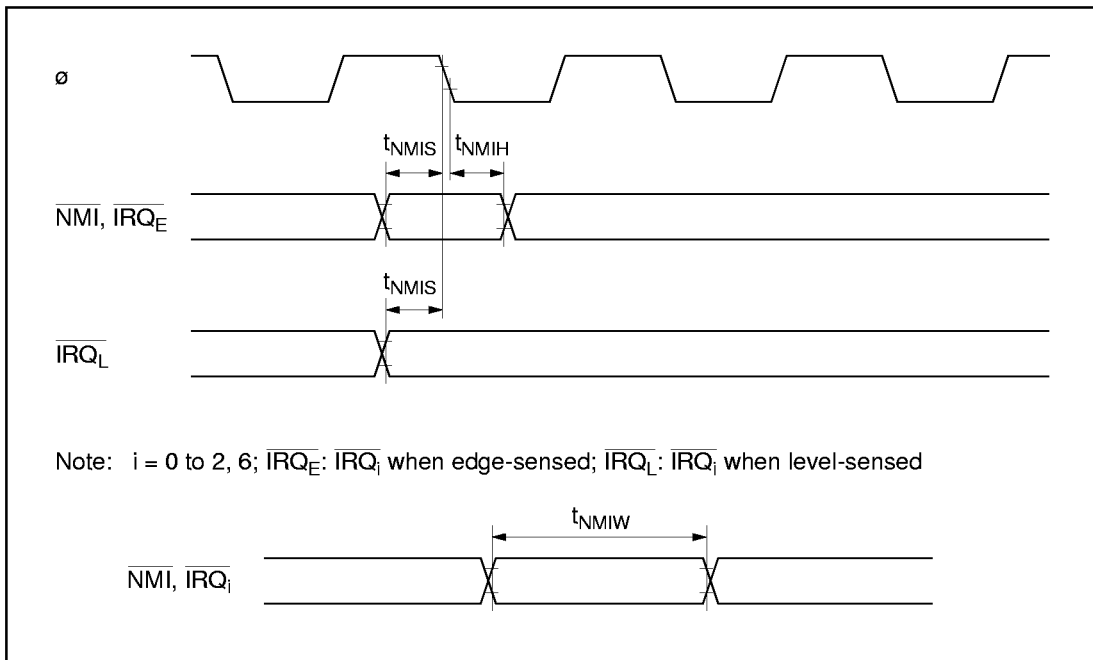


Figure 19-7 Interrupt Input Timing

(3) Clock Settling Timing

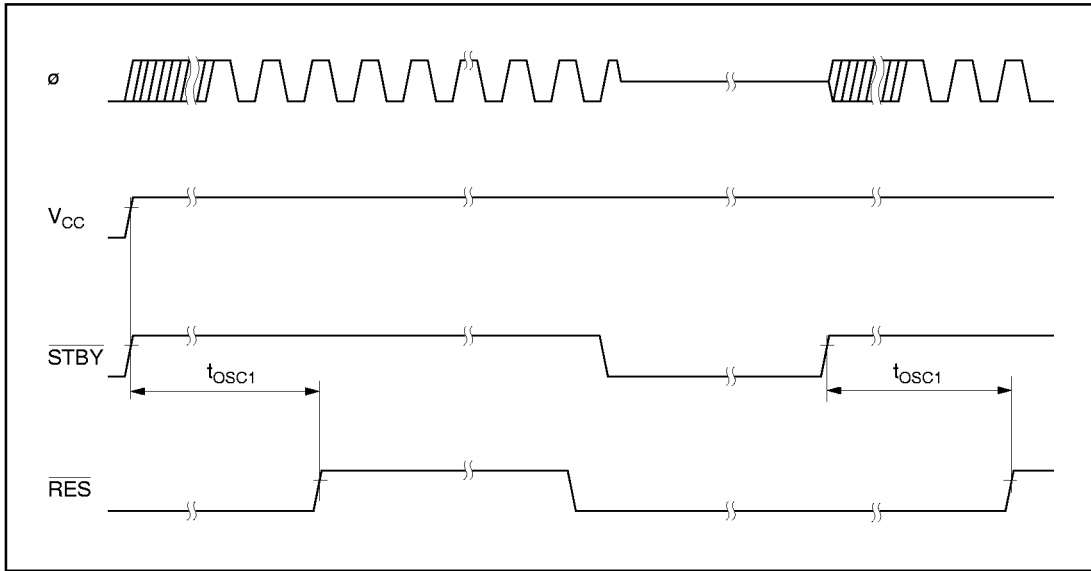


Figure 19-8 Clock Settling Timing

(4) Clock Settling Timing for Recovery from Software Standby Mode

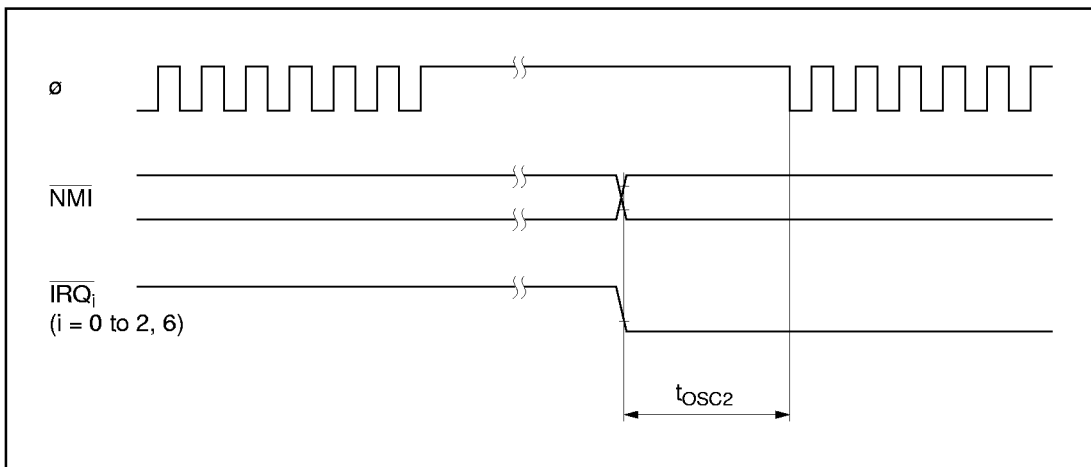


Figure 19-9 Clock Settling Timing for Recovery from Software Standby Mode

19.3.3 16-Bit Free-Running Timer Timing

(1) Free-Running Timer Input/Output Timing

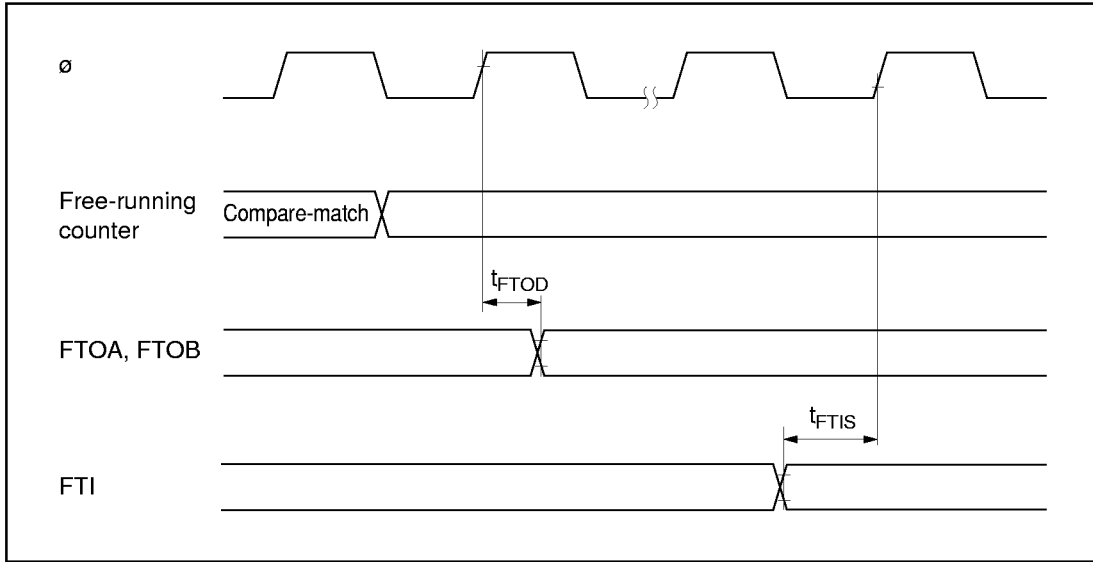


Figure 19-10 Free-Running Timer Input/Output Timing

(2) External Clock Input Timing for Free-Running Timer

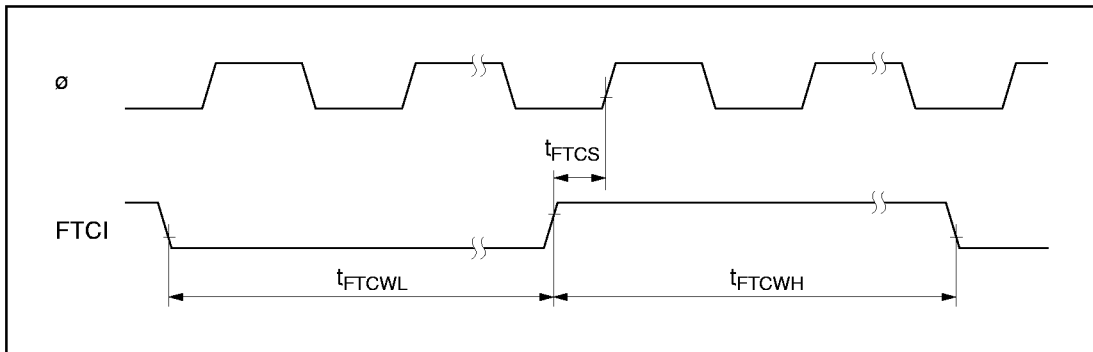


Figure 19-11 External Clock Input Timing for Free-Running Timer

19.3.4 8-Bit Timer Timing

(1) 8-Bit Timer Output Timing

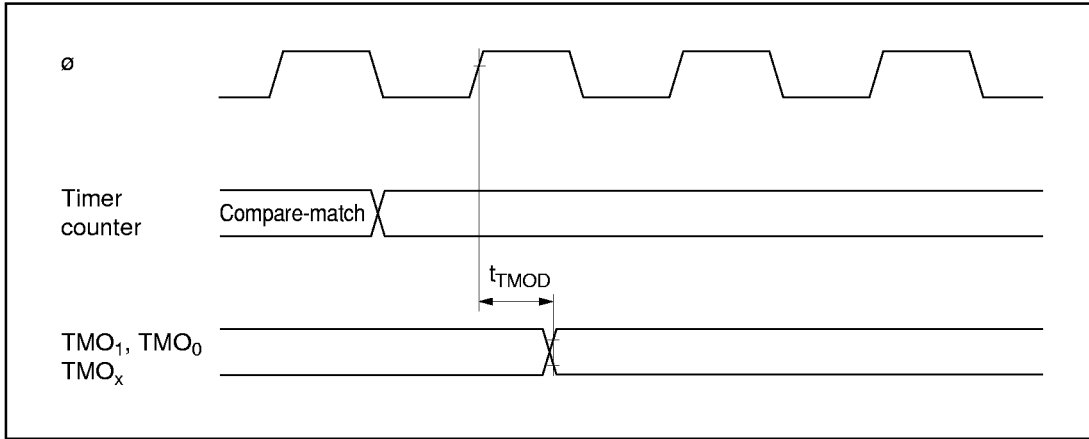


Figure 19-12 8-Bit Timer Output Timing

(2) 8-Bit Timer Clock Input Timing

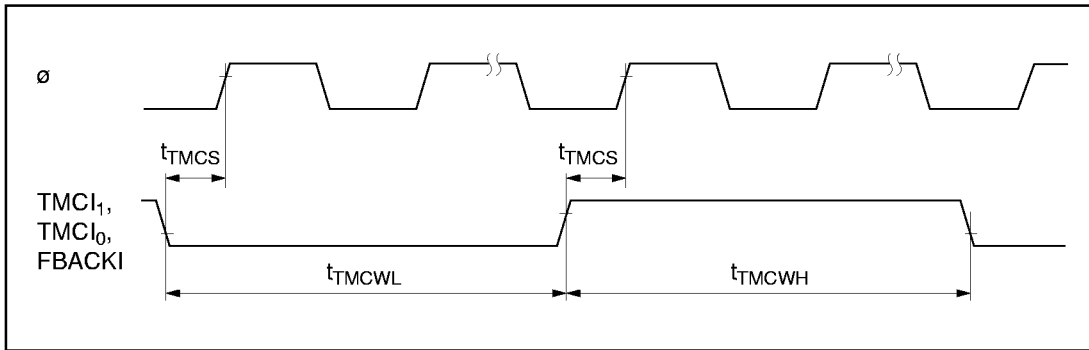


Figure 19-13 8-Bit Timer Clock Input Timing

(3) 8-Bit Timer Reset Input Timing

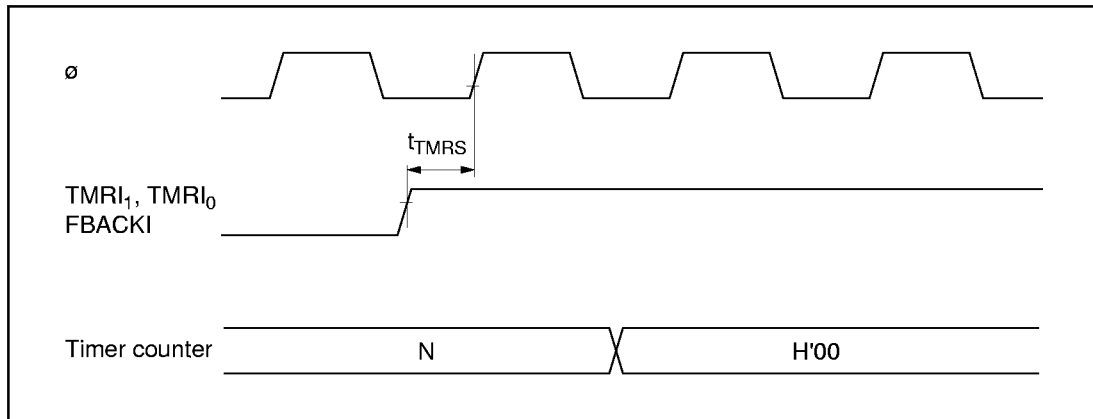


Figure 19-14 8-Bit Timer Reset Input Timing

19.3.5 Pulse Width Modulation Timer Output Timing

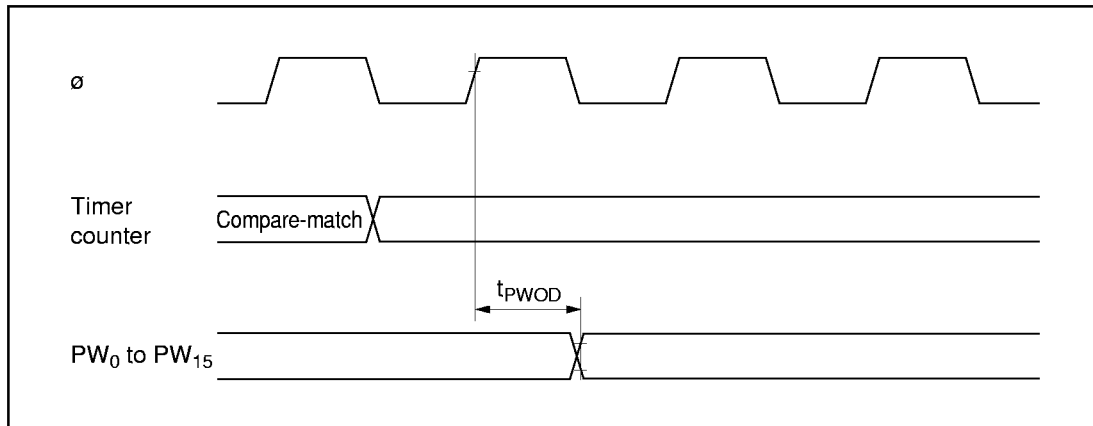


Figure 19-15 Pulse Width Modulation Timer Output Timing

19.3.6 Serial Communication Interface Timing

(1) SCI Input/Output Timing

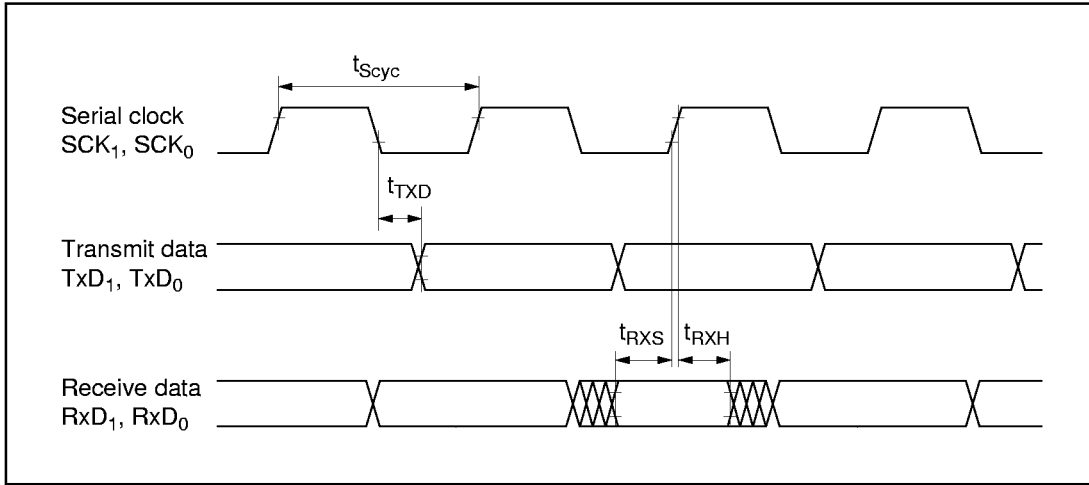


Figure 19-16 SCI Input/Output Timing (Synchronous Mode)

(2) SCI Input Clock Timing

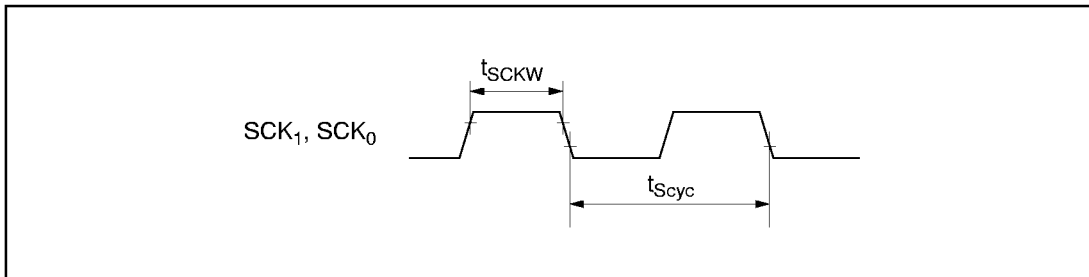


Figure 19-17 SCI Input Clock Timing

19.3.7 I/O Port Timing

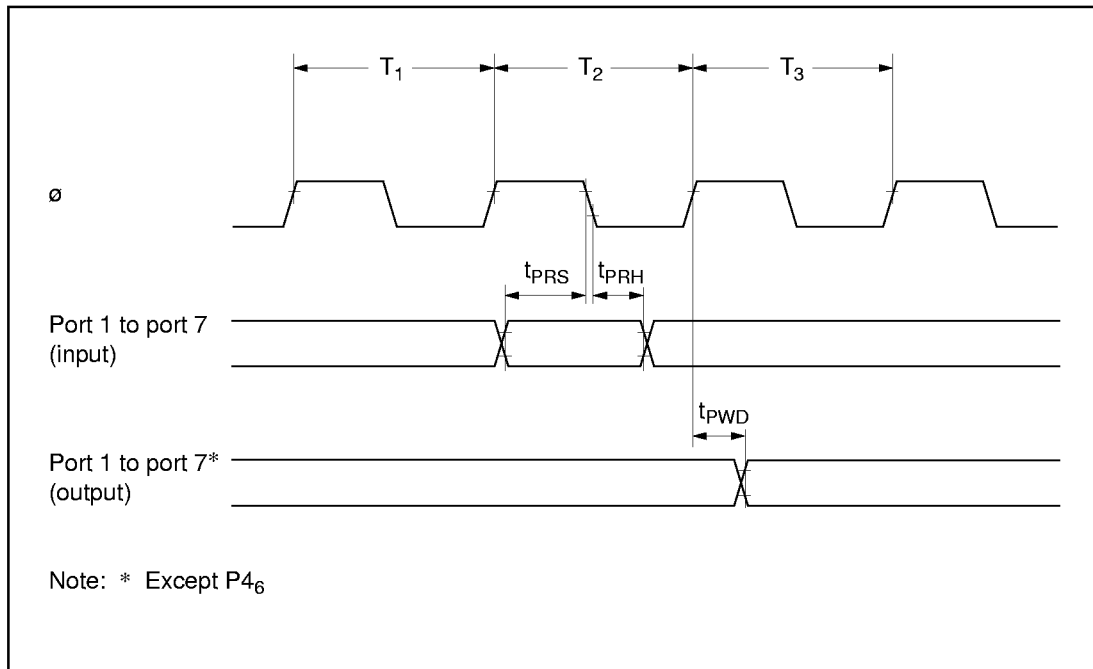


Figure 19-18 I/O Port Input/Output Timing

19.3.8 Host Interface Timing

(1) Host Interface Read Timing

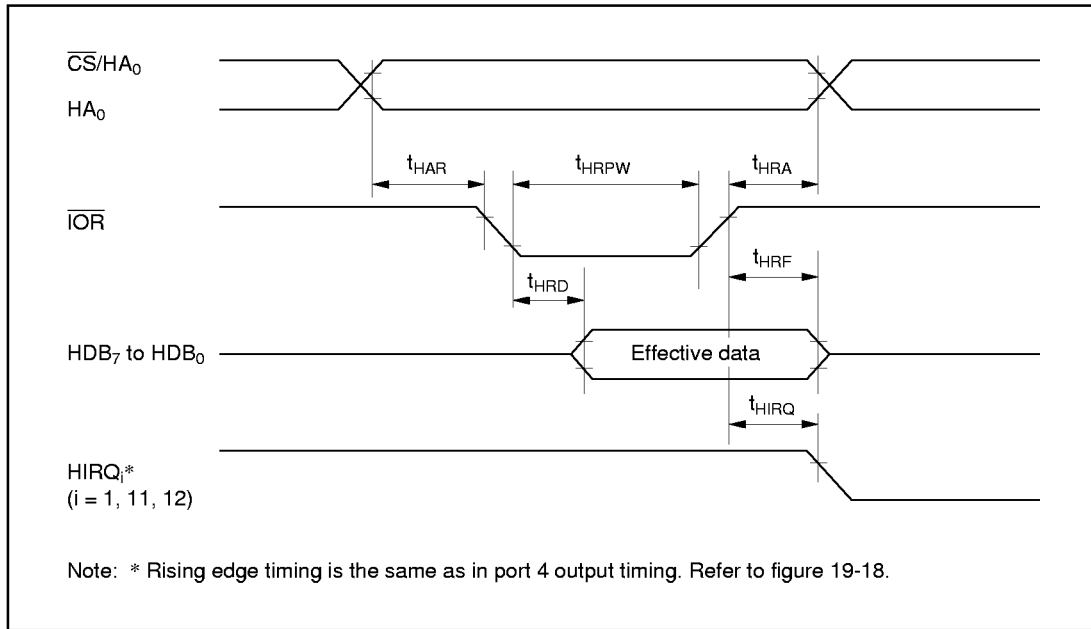


Figure 19-19 Host Interface Read Timing

(2) Host Interface Write Timing

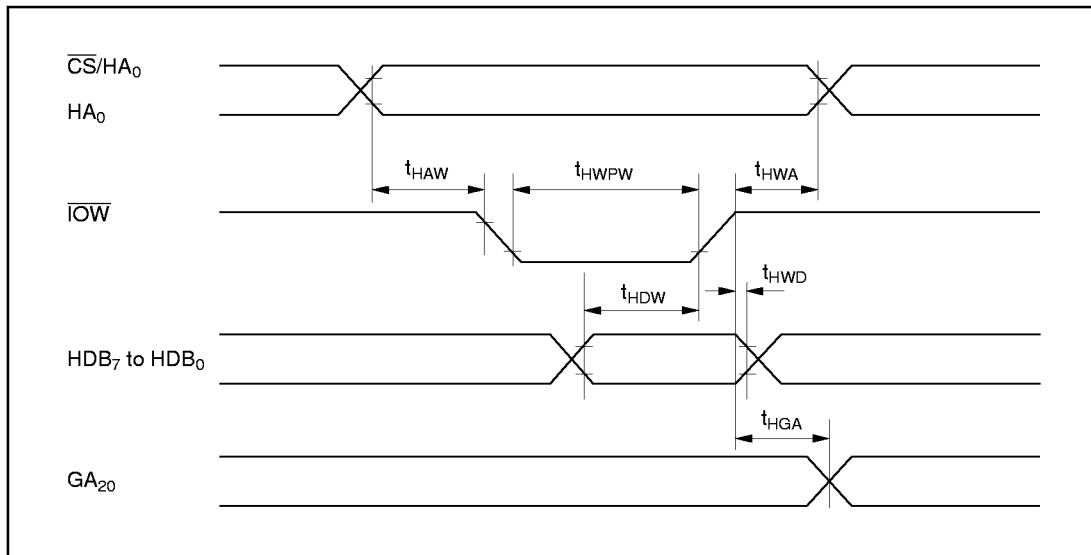


Figure 19-20 Host Interface Write Timing

19.3.9 I²C Bus Interface (Option) Timing

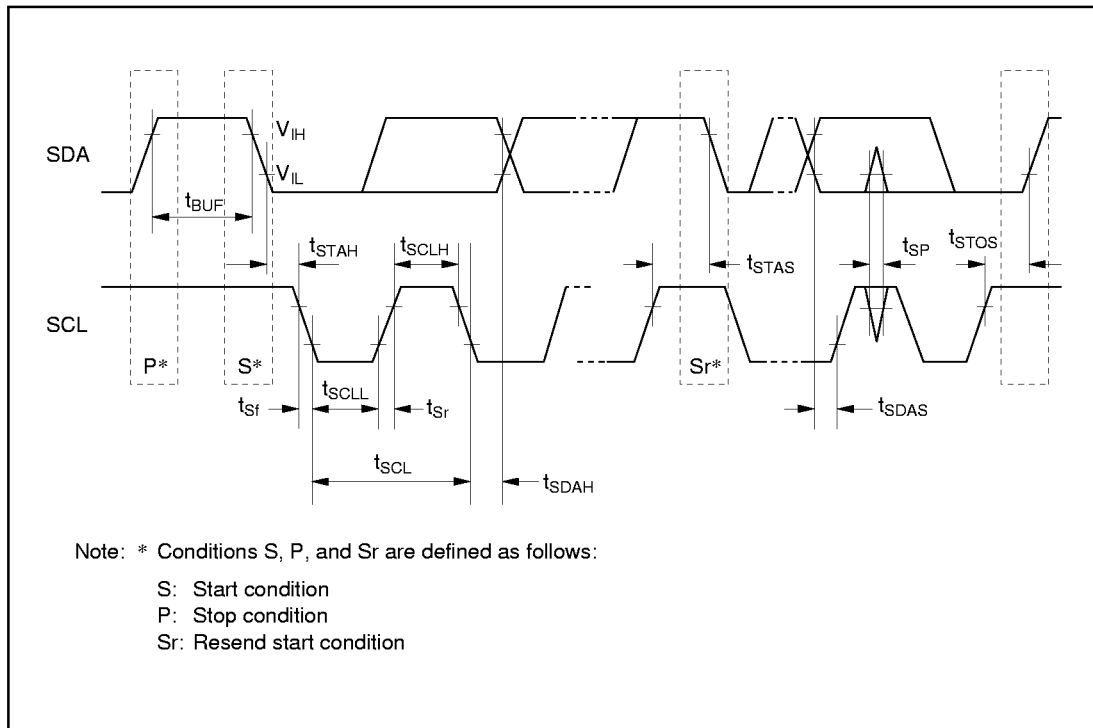


Figure 19-21 I²C Bus Interface Input/Output Timing

19.3.10 External Clock Output Timing

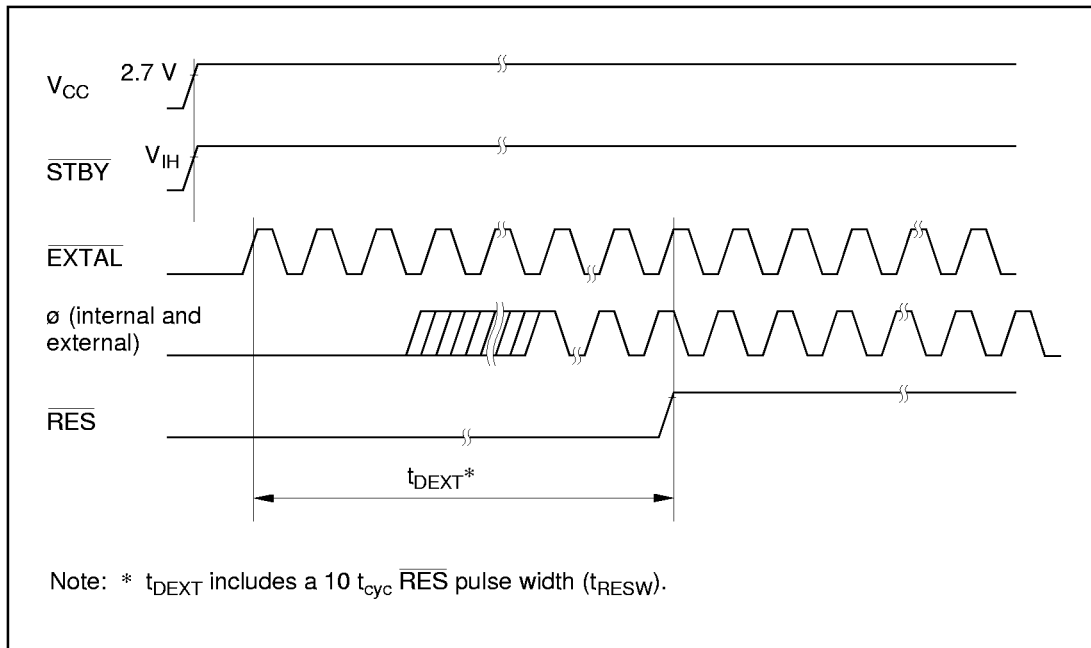


Figure 19-22 External Clock Output Settling Delay Timing