# NCV8402

# Self-Protected Low Side Driver with Temperature and Current Limit

NCV8402 is a three terminal protected Low−Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain−to−Gate clamping for overvoltage protection. This device offers protection and is suitable for harsh automotive environments.

### Features

- Short−Circuit Protection
- Thermal Shutdown with Automatic Restart
- Overvoltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- RoHs Compliant
- AEC−Q101 Qualified
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control
- These are Pb−Free Devices

### Typical Applications

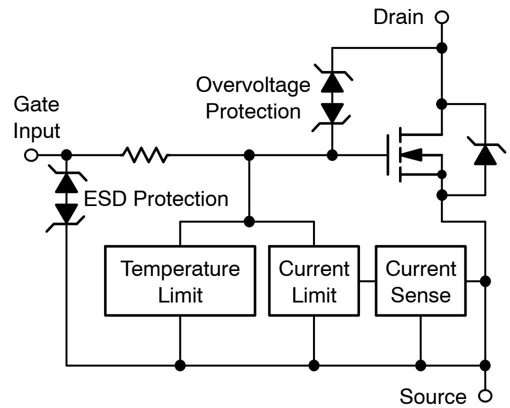
- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

**ON Semiconductor®**

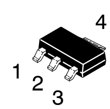
**http://onsemi.com**

| $V_{(BR)DSS}$ (Clamped) | $R_{DS(ON)}$ TYP | $I_D$ MAX |
|---|---|---|
| 42 V | 165 mΩ @ 10 V | 2.0 A* |

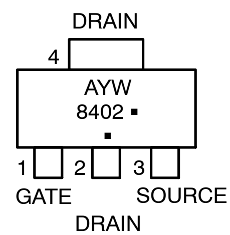
*Max current limit value is dependent on input condition.




**MARKING DIAGRAM**




**SOT−223**
**CASE 318E**
**STYLE 3**




| | |
|---|---|
| A | = Assembly Location |
| Y | = Year |
| W | = Work Week |
| 8402 | = Specific Device Code |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NCV8402STT1G | SOT−223 (Pb−Free) | 1000/Tape & Reel |
| NCV8402STT3G | SOT−223 (Pb−Free) | 4000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.





October, 2009 − Rev. 6

Publication Order Number:
**NCV8402/D**

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Drain−to−Source Voltage Internally Clamped | | $V_{DSS}$ | 42 | V |
| Drain−to−Gate Voltage Internally Clamped | ($R_G$ = 1.0 MΩ) | $V_{DGR}$ | 42 | V |
| Gate−to−Source Voltage | | $V_{GS}$ | ± 14 | V |
| Continuous Drain Current | | $I_D$ | Internally Limited | |
| Power Dissipation | @ $T_A$ = 25°C (Note 1)<br>@ $T_A$ = 25°C (Note 2)<br>@ $T_T$ = 25°C (Note 1) | $P_D$ | 1.1<br>1.7<br>8.9 | W |
| Thermal Resistance | Junction−to−Ambient Steady State (Note 1)<br>Junction−to−Ambient Steady State (Note 2)<br>Junction−to−Tab Steady State (Note 1) | $R_{\theta JA}$<br>$R_{\theta JA}$<br>$R_{\theta JT}$ | 114<br>72<br>14 | °C/W |
| Single Pulse Drain−to−Source Avalanche Energy<br>($V_{DD}$ = 32 V, $V_G$ = 5.0 V, $I_{PK}$ = 1.0 A, L = 300 mH, $R_{G(ext)}$ = 25 Ω) | | $E_{AS}$ | 150 | mJ |
| Load Dump Voltage | ($V_{GS}$ = 0 and 10 V, $R_I$ = 2.0 Ω, $R_L$ = 9.0 Ω, $t_d$ = 400 ms) | $V_{LD}$ | 87 | V |
| Operating Junction Temperature | | $T_J$ | −40 to 150 | °C |
| Storage Temperature | | $T_{stg}$ | −55 to 150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface−mounted onto min pad FR4 PCB, (2 oz. Cu, 0.06″ thick).
2. Surface−mounted onto 2″ sq. FR4 board (1″ sq., 1 oz. Cu, 0.06″ thick).

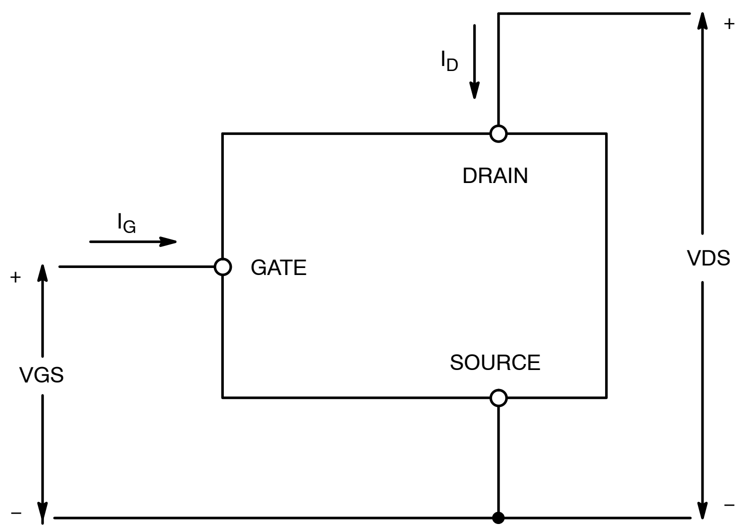



**Figure 1. Voltage and Current Convention**

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | Test Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain−to−Source Breakdown Voltage (Note 3) | $V_{GS}$ = 0 V, $I_D$ = 10 mA, $T_J$ = 25°C | $V_{(BR)DSS}$ | 42 | 46 | 55 | V |
| | $V_{GS}$ = 0 V, $I_D$ = 10 mA, $T_J$ = 150°C (Note 5) | | 40 | 45 | 55 | |
| Zero Gate Voltage Drain Current | $V_{GS}$ = 0 V, $V_{DS}$ = 32 V, $T_J$ = 25°C | $I_{DSS}$ | | 0.25 | 4.0 | μA |
| | $V_{GS}$ = 0 V, $V_{DS}$ = 32 V, $T_J$ = 150°C (Note 5) | | | 1.1 | 20 | |
| Gate Input Current | $V_{DS}$ = 0 V, $V_{GS}$ = 5.0 V | $I_{GSSF}$ | | 50 | 100 | μA |
| **ON CHARACTERISTICS** (Note 3) | | | | | | |
| Gate Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 150 μA | $V_{GS(th)}$ | 1.3 | 1.8 | 2.2 | V |
| Gate Threshold Temperature Coefficient | | $V_{GS(th)}/T_J$ | | 4.0 | | −mV/°C |
| Static Drain−to−Source On−Resistance | $V_{GS}$ = 10 V, $I_D$ = 1.7 A, $T_J$ = 25°C | $R_{DS(on)}$ | | 165 | 200 | mΩ |
| | $V_{GS}$ = 10 V, $I_D$ = 1.7 A, $T_J$ = 150°C (Note 5) | | | 305 | 400 | |
| | $V_{GS}$ = 5.0 V, $I_D$ = 1.7 A, $T_J$ = 25°C | | | 195 | 230 | |
| | $V_{GS}$ = 5.0 V, $I_D$ = 1.7 A, $T_J$ = 150°C (Note 5) | | | 360 | 460 | |
| | $V_{GS}$ = 5.0 V, $I_D$ = 0.5 A, $T_J$ = 25°C | | | 190 | 230 | |
| | $V_{GS}$ = 5.0 V, $I_D$ = 0.5 A, $T_J$ = 150°C (Note 5) | | | 350 | 460 | |
| Source−Drain Forward On Voltage | $V_{GS}$ = 0 V, $I_S$ = 7.0 A | $V_{SD}$ | | 1.0 | | V |
| **SWITCHING CHARACTERISTICS** (Note 5) | | | | | | |
| Turn−ON Time (10% $V_{IN}$ to 90% $I_D$) | $V_{GS}$ = 10 V, $V_{DD}$ = 12 V $I_D$ = 2.5 A, $R_L$ = 4.7 Ω | $t_{ON}$ | | 25 | | μs |
| Turn−OFF Time (90% $V_{IN}$ to 10% $I_D$) | | $t_{OFF}$ | | 120 | | |
| Slew−Rate ON (70% $V_{DS}$ to 50% $V_{DS}$) | $V_{GS}$ = 10 V, $V_{DD}$ = 12 V, $R_L$ = 4.7 Ω | $-dV_{DS}/dt_{ON}$ | | 0.8 | | V/μs |
| Slew−Rate OFF (50% $V_{DS}$ to 70% $V_{DS}$) | | $dV_{DS}/dt_{OFF}$ | | 0.3 | | |
| **SELF PROTECTION CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (Note 4) | | | | | | |
| Current Limit | $V_{DS}$ = 10 V, $V_{GS}$ = 5.0 V, $T_J$ = 25°C | $I_{LIM}$ | 3.7 | 4.3 | 5.0 | A |
| | $V_{DS}$ = 10 V, $V_{GS}$ = 5.0 V, $T_J$ = 150°C (Note 5) | | 2.3 | 3.0 | 3.7 | |
| | $V_{DS}$ = 10 V, $V_{GS}$ = 10 V, $T_J$ = 25°C | | 4.2 | 4.8 | 5.4 | |
| | $V_{DS}$ = 10 V, $V_{GS}$ = 10 V, $T_J$ = 150°C (Note 5) | | 2.7 | 3.6 | 4.5 | |
| Temperature Limit (Turn−off) | $V_{GS}$ = 5.0 V (Note 5) | $T_{LIM(off)}$ | 150 | 175 | 200 | °C |
| Thermal Hysteresis | $V_{GS}$ = 5.0 V | $\Delta T_{LIM(on)}$ | | 15 | | |
| Temperature Limit (Turn−off) | $V_{GS}$ = 10 V (Note 5) | $T_{LIM(off)}$ | 150 | 165 | 185 | |
| Thermal Hysteresis | $V_{GS}$ = 10 V | $\Delta T_{LIM(on)}$ | | 15 | | |
| **GATE INPUT CHARACTERISTICS** (Note 5) | | | | | | |
| Device ON Gate Input Current | $V_{GS}$ = 5 V $I_D$ = 1.0 A | $I_{GON}$ | | 50 | | μA |
| | $V_{GS}$ = 10 V $I_D$ = 1.0 A | | | 400 | | |
| Current Limit Gate Input Current | $V_{GS}$ = 5 V, $V_{DS}$ = 10 V | $I_{GCL}$ | | 0.05 | | mA |
| | $V_{GS}$ = 10 V, $V_{DS}$ = 10 V | | | 0.4 | | |
| Thermal Limit Fault Gate Input Current | $V_{GS}$ = 5 V, $V_{DS}$ = 10 V | $I_{GTL}$ | | 0.15 | | mA |
| | $V_{GS}$ = 10 V, $V_{DS}$ = 10 V | | | 0.7 | | |
| **ESD ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (Note 5) | | | | | | |
| Electro−Static Discharge Capability | Human Body Model (HBM) | ESD | 4000 | | | V |
| | Machine Model (MM) | | 400 | | | |

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Fault conditions are viewed as beyond the normal operating range of the part.
5. Not subject to production testing.

## TYPICAL PERFORMANCE CURVES

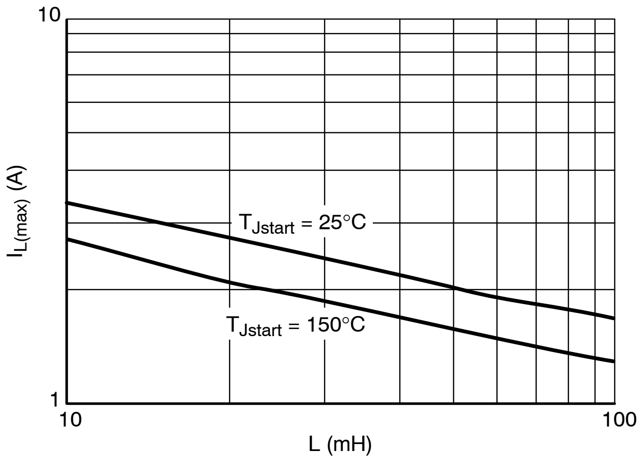



**Figure 2. Single Pulse Maximum Switch−off Current vs. Load Inductance**

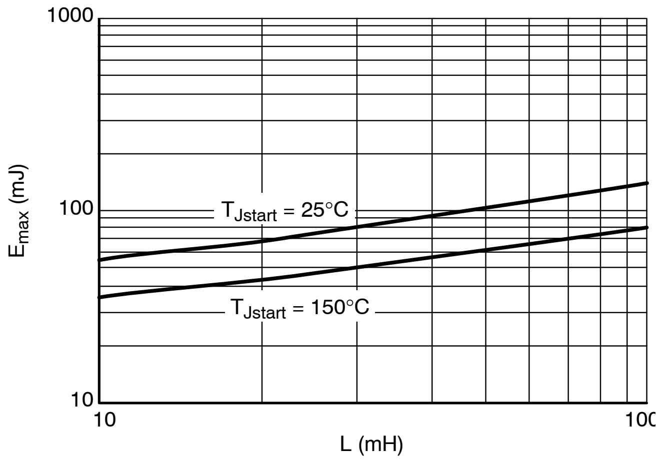



**Figure 3. Single Pulse Maximum Switching Energy vs. Load Inductance**

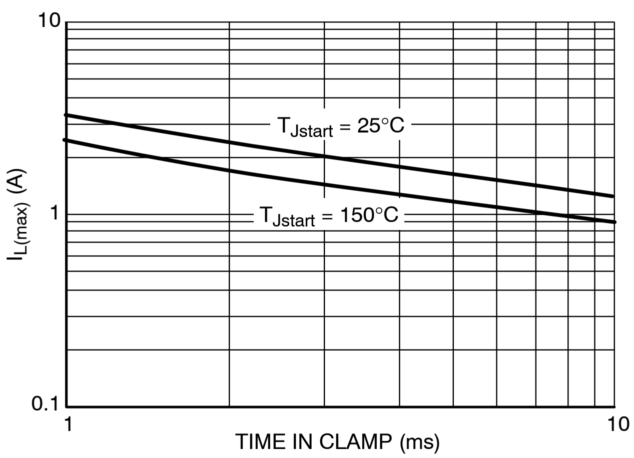



**Figure 4. Single Pulse Maximum Inductive Switch−off Current vs. Time in Clamp**

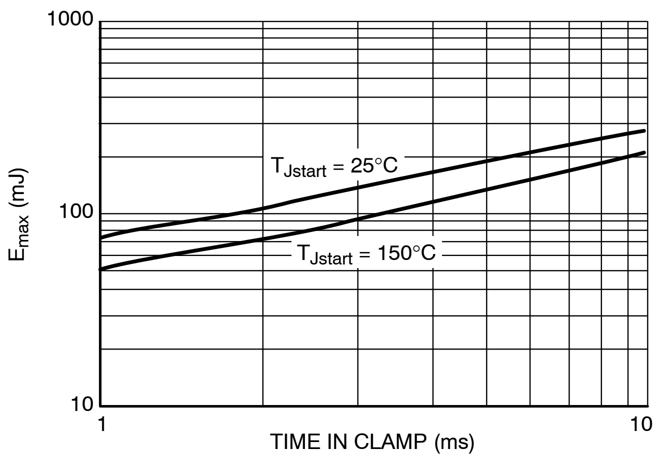



**Figure 5. Single Pulse Maximum Inductive Switching Energy vs. Time in Clamp**

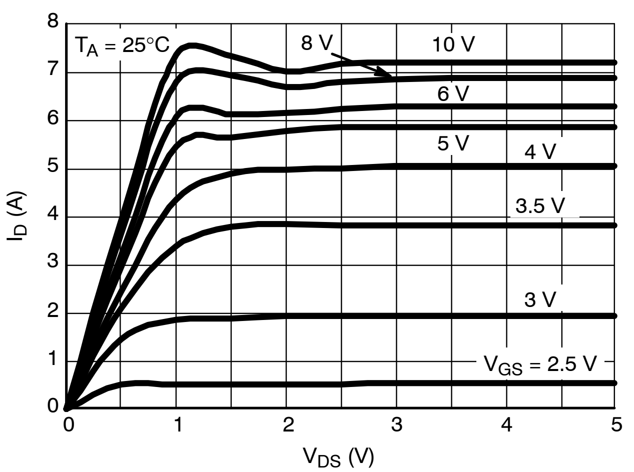



**Figure 6. On−state Output Characteristics**

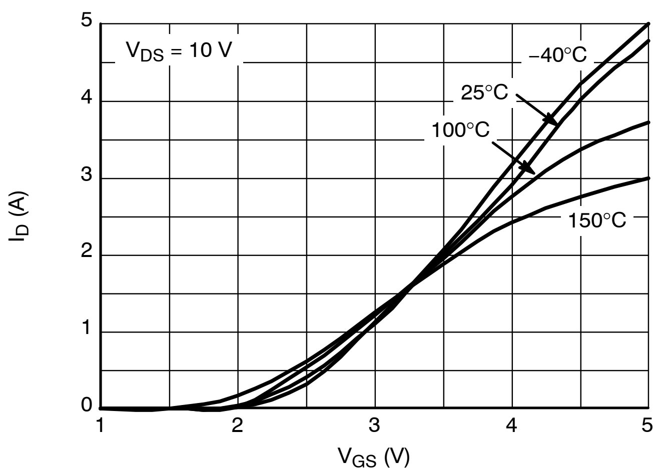



**Figure 7. Transfer Characteristics**

## TYPICAL PERFORMANCE CURVES

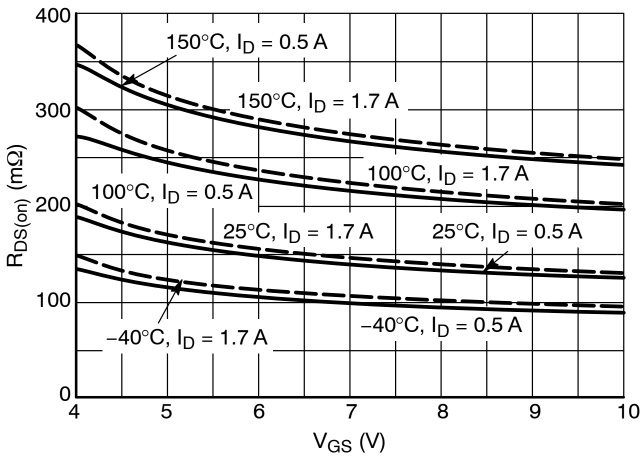



**Figure 8. $R_{DS(on)}$ vs. Gate−Source Voltage**

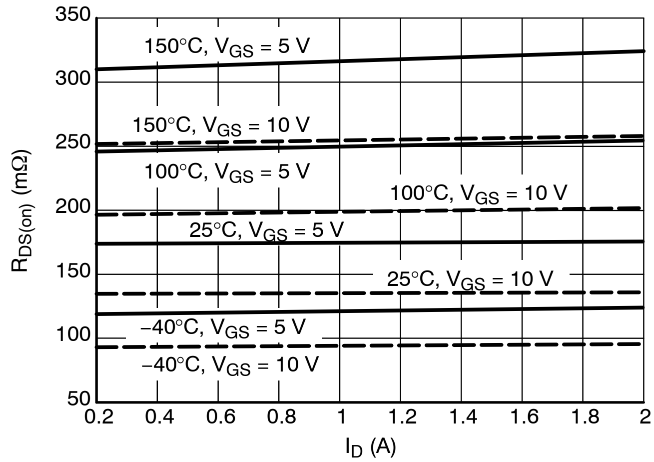



**Figure 9. $R_{DS(on)}$ vs. Drain Current**

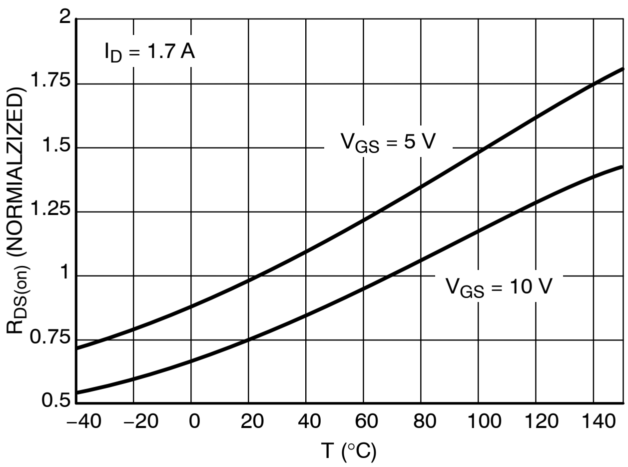



**Figure 10. Normalized $R_{DS(on)}$ vs. Temperature**

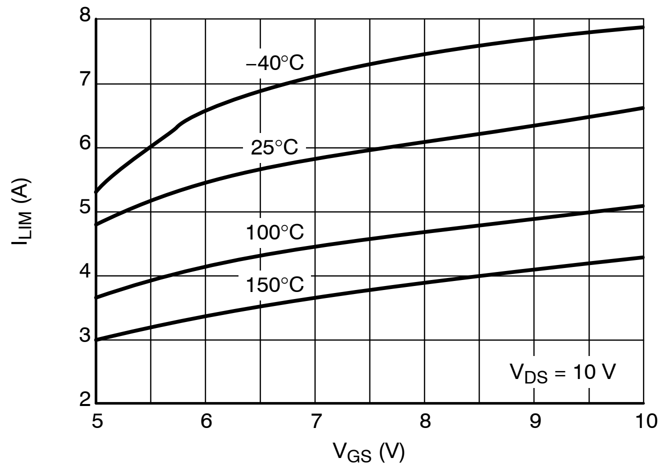



**Figure 11. Current Limit vs. Gate−Source Voltage**

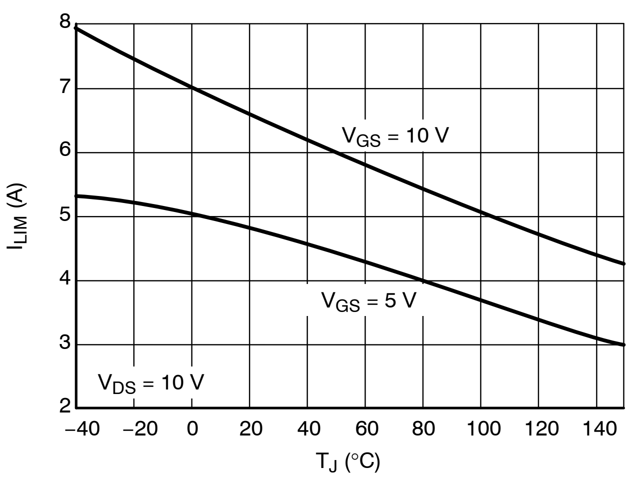



**Figure 12. Current Limit vs. Junction Temperature**

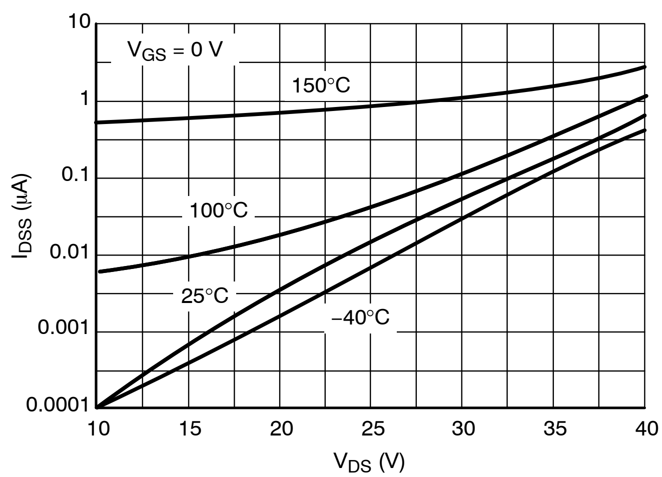



**Figure 13. Drain−to−Source Leakage Current**

## TYPICAL PERFORMANCE CURVES

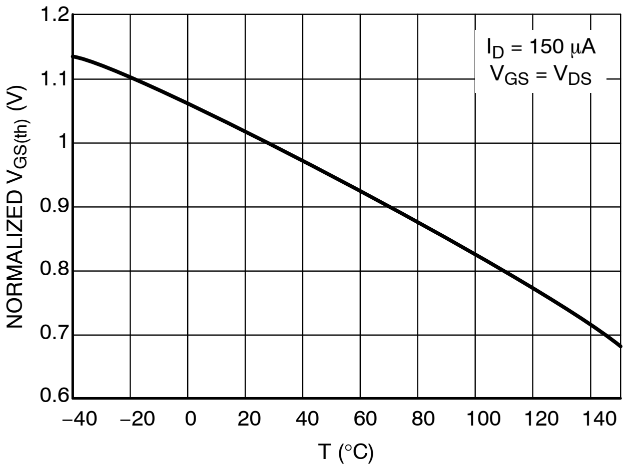



**Figure 14. Normalized Threshold Voltage vs. Temperature**

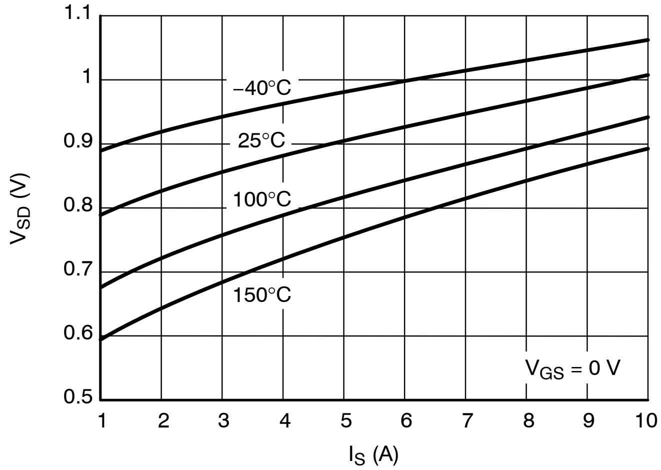



**Figure 15. Source−Drain Diode Forward Characteristics**

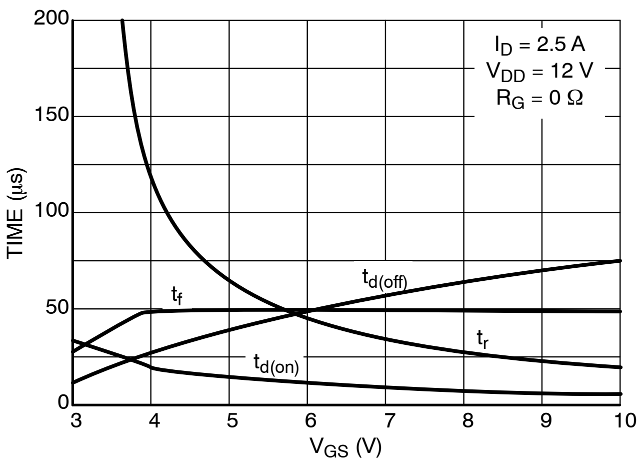



**Figure 16. Resistive Load Switching Time vs. Gate−Source Voltage**

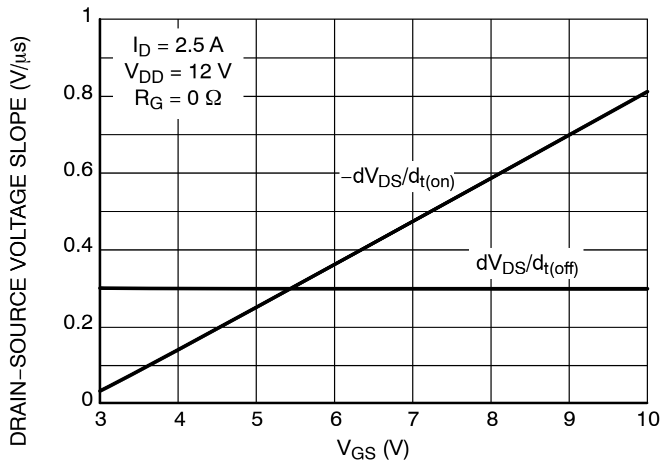



**Figure 17. Resistive Load Switching Drain−Source Voltage Slope vs. Gate−Source Voltage**

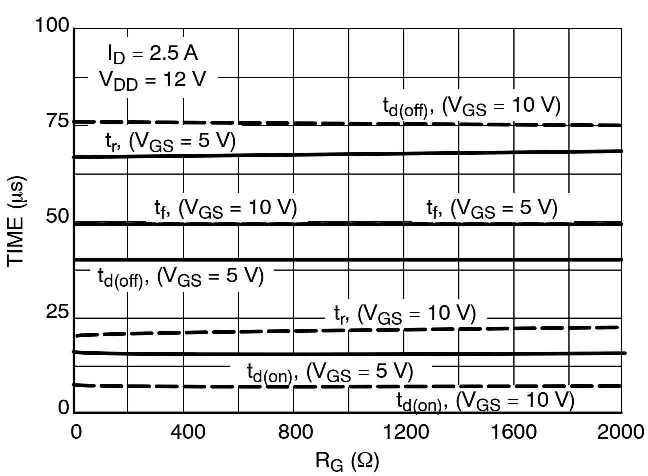



**Figure 18. Resistive Load Switching Time vs. Gate Resistance**

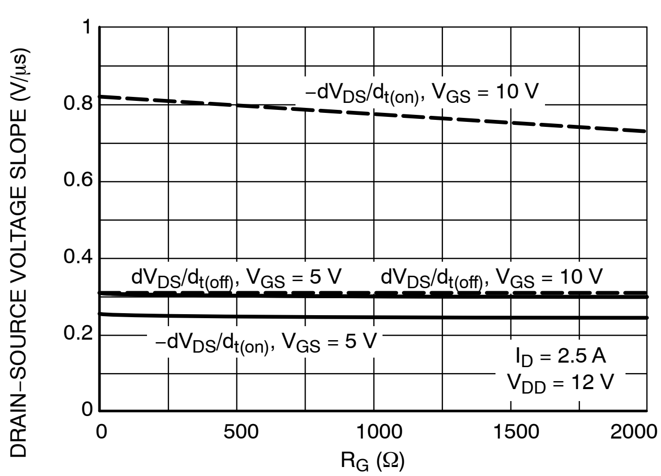



**Figure 19. Drain−Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance**

## TYPICAL PERFORMANCE CURVES

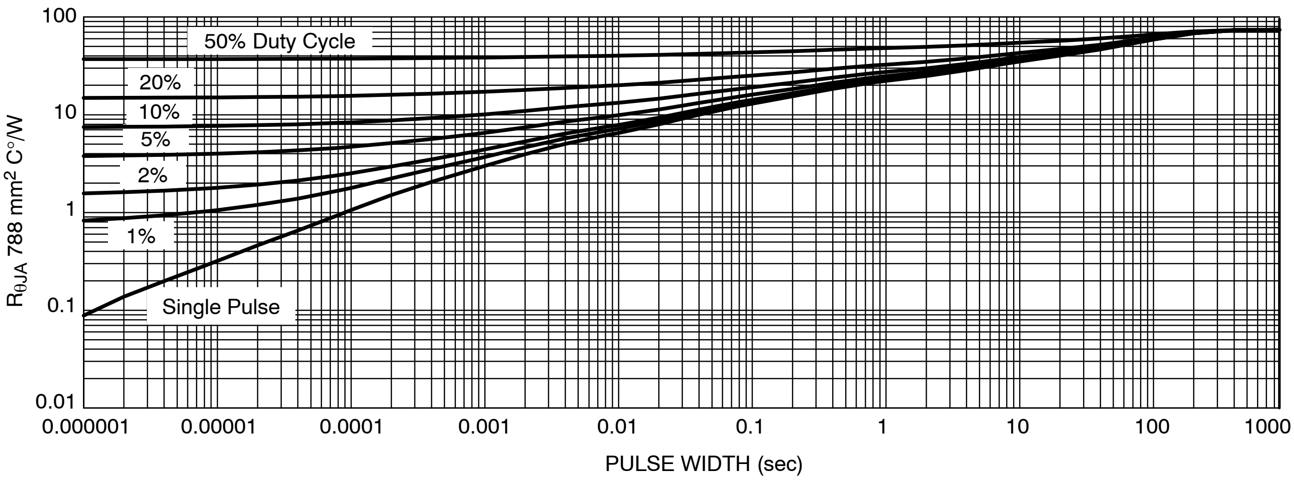



**Figure 20. Transient Thermal Resistance**

## TEST CIRCUITS AND WAVEFORMS

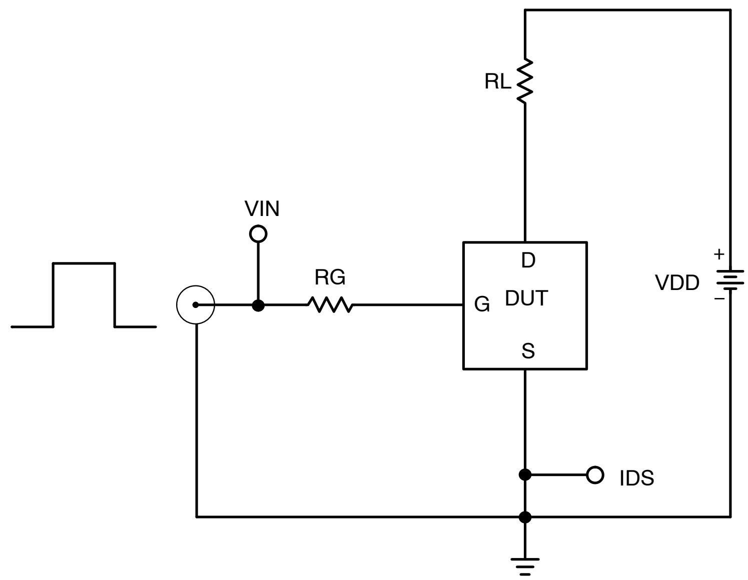



**Figure 21. Resistive Load Switching Test Circuit**

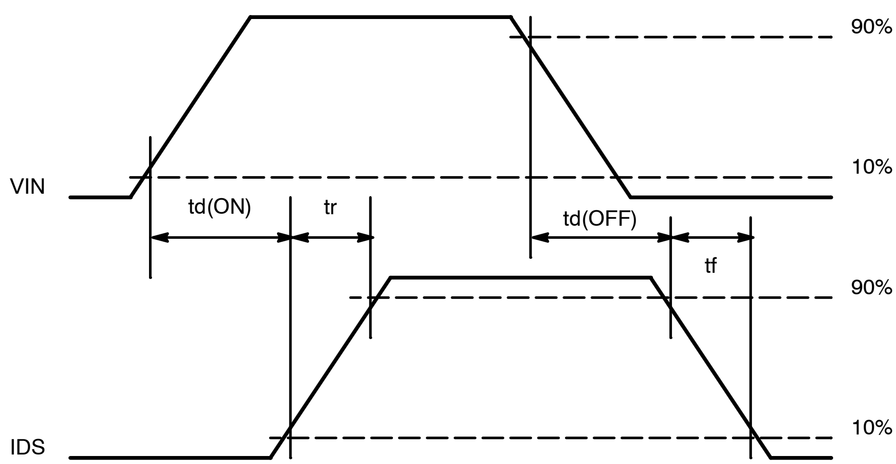



**Figure 22. Resistive Load Switching Waveforms**

## TEST CIRCUITS AND WAVEFORMS

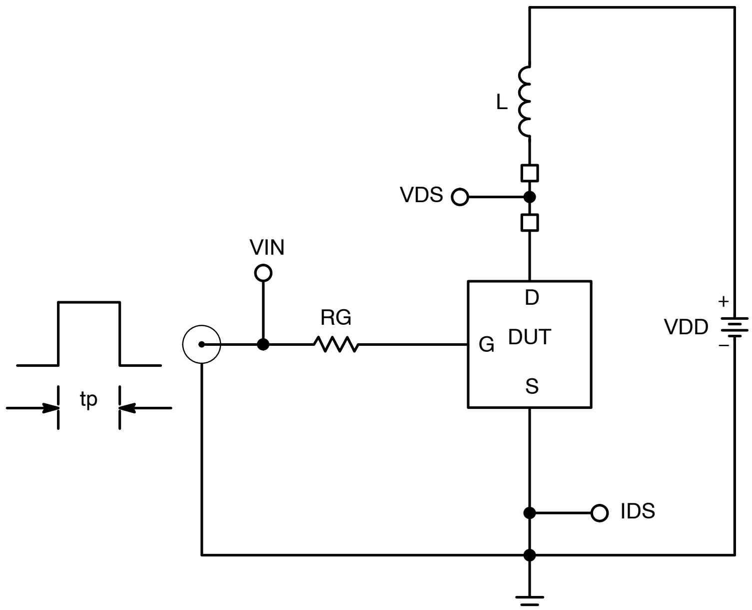



**Figure 23. Inductive Load Switching Test Circuit**

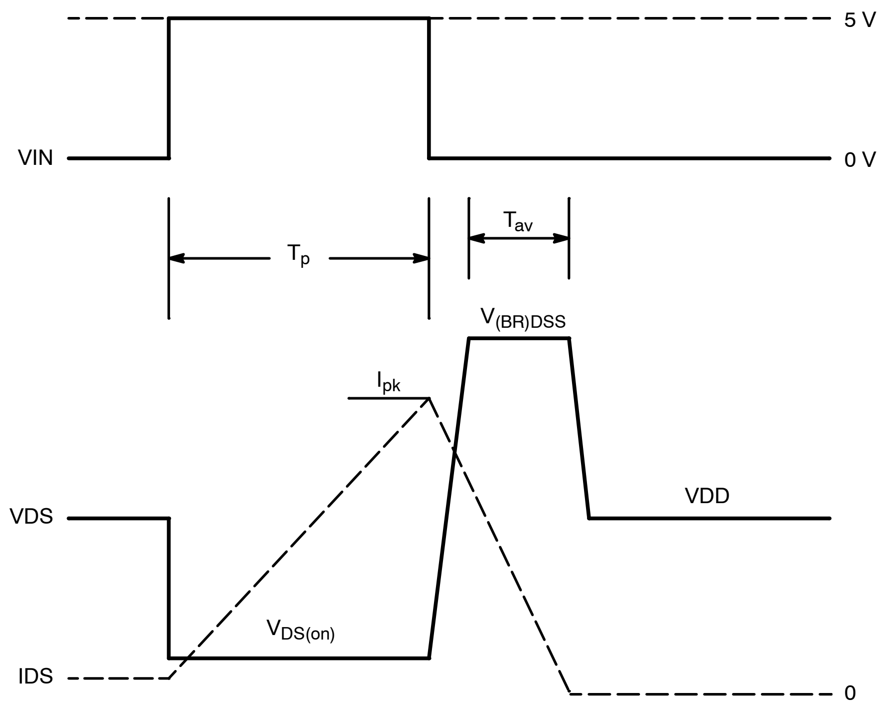
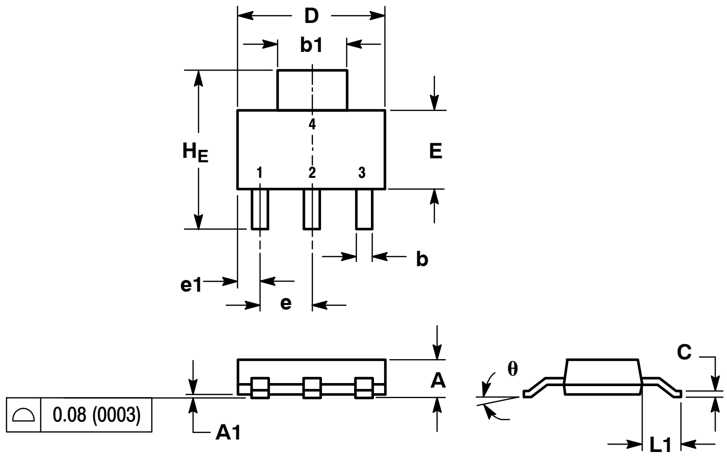



**Figure 24. Inductive Load Switching Waveforms**

## PACKAGE DIMENSIONS

**SOT−223 (TO−261)**
CASE 318E−04
ISSUE M

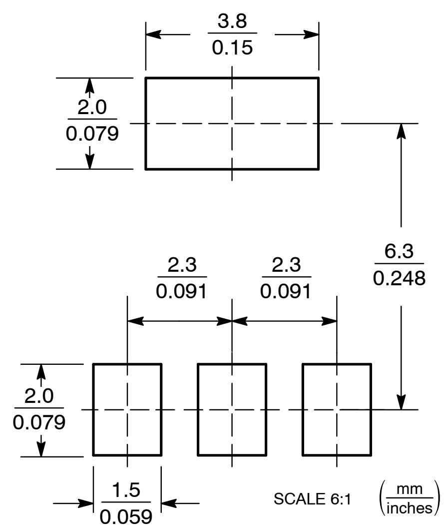



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| **DIM** | **MIN** | **NOM** | **MAX** | **MIN** | **NOM** | **MAX** |
| **A** | 1.50 | 1.63 | 1.75 | 0.060 | 0.064 | 0.068 |
| **A1** | 0.02 | 0.06 | 0.10 | 0.001 | 0.002 | 0.004 |
| **b** | 0.60 | 0.75 | 0.89 | 0.024 | 0.030 | 0.035 |
| **b1** | 2.90 | 3.06 | 3.20 | 0.115 | 0.121 | 0.126 |
| **c** | 0.24 | 0.29 | 0.35 | 0.009 | 0.012 | 0.014 |
| **D** | 6.30 | 6.50 | 6.70 | 0.249 | 0.256 | 0.263 |
| **E** | 3.30 | 3.50 | 3.70 | 0.130 | 0.138 | 0.145 |
| **e** | 2.20 | 2.30 | 2.40 | 0.087 | 0.091 | 0.094 |
| **e1** | 0.85 | 0.94 | 1.05 | 0.033 | 0.037 | 0.041 |
| **L1** | 1.50 | 1.75 | 2.00 | 0.060 | 0.069 | 0.078 |
| **$H_E$** | 6.70 | 7.00 | 7.30 | 0.264 | 0.276 | 0.287 |
| **θ** | 0° | − | 10° | 0° | − | 10° |

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

## SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT**:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
**Phone**: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
**Fax**: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
**Email**: orderlit@onsemi.com

**N. American Technical Support**: 800−282−9855 Toll Free USA/Canada
**Europe, Middle East and Africa Technical Support:**
Phone: 421 33 790 2910
**Japan Customer Focus Center**
Phone: 81−3−5773−3850

**ON Semiconductor Website**: **www.onsemi.com**

**Order Literature**: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative