

Single and Dual Single Supply Ultra-Low Noise, Ultra-Low Distortion, Rail-to-Rail Output, Op Amp

The ISL28190 and ISL28290 are tiny single and dual ultra-low noise, ultra-low distortion operational amplifiers. Fully specified to operated down to +3V single supply. These amplifiers have outputs that swing rail-to-rail, and an input common mode voltage that extends below ground (ground sensing).

The ISL28190 and ISL28290 are unity gain stable with an input referred voltage noise of $1\text{nV}/\sqrt{\text{Hz}}$. Both parts feature 0.00017% THD+N @ 1kHz.

The ISL28190 is available in the space-saving 6 Ld μ TDFN (1.6mmx1.6mm) and 6 Ld SOT-23 packages. The ISL28290 is available in the 10 Ld μ TQFN (1.8mmx1.4mm) and 10 Ld MSOP packages. All devices are guaranteed over -40°C to $+125^{\circ}\text{C}$.

Ordering Information

PART NUMBER	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
ISL28190FHZ-T7* (Note 1)	GABH	6 Ld SOT-23	MDP0038
ISL28190FRUZ-T7* (Note 2)	M7	6 Ld μ TDFN	L6.1.6x1.6A
ISL28290FUZ (Note 1)	8290Z	10 Ld MSOP	MDP0043
ISL28290FUZ-T7* (Note 1)	8290Z	10 Ld MSOP	MDP0043
ISL28290FRUZ-T7* (Note 2)	E	10 Ld μ TQFN	L10.1.8x1.4A
ISL28290FBZ (Note 1)	28290 FBZ	8 Ld SOIC	MDP0027
ISL28290FBZ-T7* (Note 1)	28290 FBZ	8 Ld SOIC	MDP0027
ISL28290EVAL1Z	Evaluation Board		

*Please refer to TB347 for details on reel specifications.

NOTES:

- These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

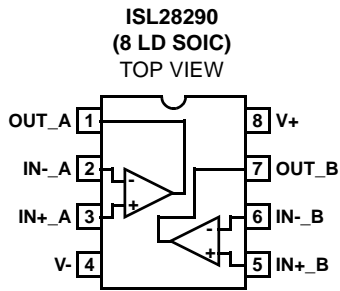
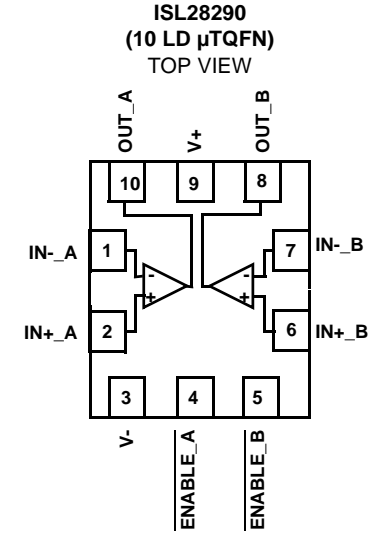
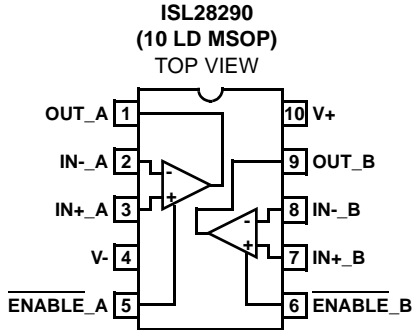
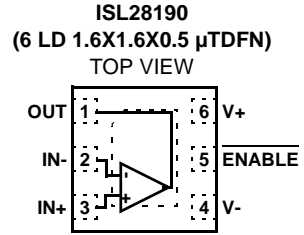
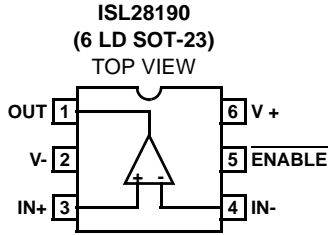
Features

- $1\text{nV}/\sqrt{\text{Hz}}$ input voltage noise
- 1kHz THD+N typical 0.00017% at $2V_{P-P}$ V_{OUT}
- Harmonic Distortion -87dBc, -90dBc, $f_o = 1\text{MHz}$
- 170MHz -3dB bandwidth
- $50\text{V}/\mu\text{s}$ slew rate
- 700 μV maximum offset voltage
- 10 μA typical input bias current
- 103dB typical CMRR
- 3V to 5.5V single supply voltage range
- Rail-to-rail output
- Ground sensing
- Enable pin (not available in the 8 Ld SOIC package option)
- Pb-free (RoHS compliant)

Applications

- Low noise signal processing
- Low noise microphones/preamplifiers
- ADC buffers
- DAC output amplifiers
- Digital scales
- Strain gauges/sensor amplifiers
- Radio systems
- Portable equipment
- Infrared detectors

Pinouts



ISL28190, ISL28290

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage	5.5V
Supply Turn On Voltage Slew Rate	1V/μs
Differential Input Current	5mA
Differential Input Voltage	0.5V
Input Voltage	V ₋ - 0.5V to V ₊ + 0.5V
ESD Tolerance	
Human Body Model	.3kV
Machine Model	.300V
Charged Device Model	1200V

Thermal Information

Thermal Resistance (typical, Note 3)	θ _{JA} (°C/W)
6 Ld SOT-23 Package	230
6 Ld μTDFN Package	125
10 Ld MSOP Package	150
10 Ld μTQFN Package	180
8 Ld SOIC Package	125
Ambient Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature	+125°C
Pb-free Reflow Profile	see link below
	http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

- θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: T_J = T_C = T_A

Electrical Specifications V₊ = 5.0V, V₋ = GND, R_L = Open, R_F = 1kΩ, A_V = -1 unless otherwise specified. Parameters are per amplifier. Typical values are at V₊ = 5V, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C, temperature data established by characterization.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNIT
DC SPECIFICATIONS						
V _{OS}	Input Offset Voltage		-1100	240	700 900	μV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Drift vs Temperature	See Figure 21		1.9		μV/°C
I _{IO}	Input Offset Current			40	500 900	nA
I _B	Input Bias Current			10	16 18	μA
V _{CM}	Common-Mode Voltage Range		0		3.8	V
CMRR	Common-Mode Rejection Ratio	V _{CM} = 0V to 3.8V	78	103		dB
PSRR	Power Supply Rejection Ratio	V _S = 3V to 5V	74	80		dB
A _{VOL}	Large Signal Voltage Gain	V _O = 0.5V to 4V, R _L = 1kΩ	94 90	102		dB
V _{OUT}	Maximum Output Voltage Swing	Output low, R _L = 1kΩ		20	50 80	mV
		Output high, R _L = 1kΩ, V ₊ = 5V	4.95 4.92	4.97		V
I _{S,ON}	Supply Current per Channel, Enabled			8.5	11 13	mA
I _{S,OFF}	Supply Current, Disabled			26	35 52	μA
I _{O+}	Short-Circuit Output Current	R _L = 10Ω	95 90	144		mA
I _{O-}	Short-Circuit Output Current	R _L = 10Ω	95 90	135		mA
V _{SUPPLY}	Supply Operating Range	V ₊ to V ₋	3		5.5	V
V _{ENH}	EN High Level	Referred to V ₋	2			V

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Electrical Specifications $V_+ = 5.0V$, $V_- = GND$, $R_L = \text{Open}$, $R_F = 1k\Omega$, $A_V = -1$ unless otherwise specified. Parameters are per amplifier. Typical values are at $V_+ = 5V$, $T_A = +25^\circ C$. **Boldface limits apply over the operating temperature range, $-40^\circ C$ to $+125^\circ C$, temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNIT
$\overline{V_{ENL}}$	\overline{EN} Low Level	Referred to V_-			0.8	V
$\overline{I_{ENH}}$	\overline{EN} Pin Input High Current	$\overline{V_{EN}} = V_+$		0.8	1.2 1.4	μA
$\overline{I_{ENL}}$	\overline{EN} Pin Input Low Current	$\overline{V_{EN}} = V_-$		20	80 100	nA
AC SPECIFICATIONS						
GBW	-3dB Unity Gain Bandwidth	$R_F = 0\Omega$, $C_L = 20pF$, $A_V = 1$, $R_L = 10k\Omega$		170		MHz
THD+N	Total Harmonic Distortion + Noise	$f = 1kHz$, $V_{OUT} = 2V_{P-P}$, $A_V = +1$, $R_L = 10k\Omega$		0.00017		%
HD (1MHz)	2nd Harmonic Distortion	$V_{OUT} = 2V_{P-P}$, $A_V = 1$		-87		dBc
	3rd Harmonic Distortion			-90		dBc
ISO	Off-state Isolation $f_O = 100kHz$	$A_V = +1$; $V_{IN} = 100mV_{P-P}$; $R_F = 0\Omega$, $C_L = 20pF$, $A_V = 1$, $R_L = 10k\Omega$		-38		dB
X-TALK ISL28290	Channel-to-Channel Crosstalk $f_O = 100kHz$	$V_S = \pm 2.5V$; $A_V = +1$; $V_{IN} = 1V_{P-P}$, $R_F = 0\Omega$, $C_L = 20pF$, $A_V = 1$, $R_L = 10k\Omega$		-105		dB
PSRR	Power Supply Rejection Ratio $f_O = 100kHz$	$V_S = \pm 2.5V$; $A_V = +1$; $V_{SOURCE} = 1V_{P-P}$, $R_F = 0\Omega$, $C_L = 20pF$, $A_V = 1$, $R_L = 10k\Omega$		-70		dB
CMRR	Common Mode Rejection Ratio $f_O = 100kHz$	$V_S = \pm 2.5V$; $A_V = +1$; $V_{CM} = 1V_{P-P}$, $R_F = 0\Omega$, $C_L = 20pF$, $A_V = 1$, $R_L = 10k\Omega$		-65		dB
e_n	Input Referred Voltage Noise	$f_O = 1kHz$		1		nV/ \sqrt{Hz}
i_n	Input Referred Current Noise	$f_O = 10kHz$		2.1		pA/ \sqrt{Hz}
TRANSIENT RESPONSE						
SR	Slew Rate		30 25	50		V/ μs
t_{pd}	Propagation Delay 10% V_{IN} - 10% V_{OUT}	$A_V = 1$, $V_{OUT} = 100mV_{P-P}$, $R_F = 0\Omega$, $C_L = 1.2pF$		1.0		ns
t_r , t_f , Small Signal	Rise Time, t_r 10% to 90%	$A_V = +1$, $V_{OUT} = 0.1V_{P-P}$, $R_F = 0\Omega$, $C_L = 1.2pF$		3.3		ns
	Fall Time, t_f 10% to 90%			6.3		ns
t_r , t_f Large Signal	Rise Time, t_r 10% to 90%	$A_V = +2$, $V_{OUT} = 1V_{P-P}$, $R_F = R_G = 499\Omega$, $R_L = 10k\Omega$, $C_L = 1.2pF$		44		ns
	Fall Time, t_f 10% to 90%			51		ns
	Rise Time, t_r 10% to 90%	$A_V = +2$, $V_{OUT} = 4.7V_{P-P}$, $R_F = R_G = 499\Omega$, $R_L = 10k\Omega$, $C_L = 1.2pF$		190		ns
	Fall Time, t_f 10% to 90%			187		ns
t_s	Settling Time to 0.1% 90% V_{OUT} to 0.1% V_{OUT}	$A_V = 1$, $V_{OUT} = 1V_{P-P}$, $R_F = 0\Omega$, $C_L = 1.2pF$		45		ns
t_{EN}	ENABLE to Output Turn-on Delay Time; 10% \overline{EN} - 10% V_{OUT}	$A_V = 1$, $V_{OUT} = 1V_{DC}$, $R_L = 10k\Omega$, $C_L = 1.2pF$		330		ns
	ENABLE to Output Turn-off Delay Time; 10% \overline{EN} - 10% V_{OUT}	$A_V = 1$, $V_{OUT} = 0V_{DC}$, $R_L = 10k\Omega$, $C_L = 1.2pF$		50		ns

NOTE:

- Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

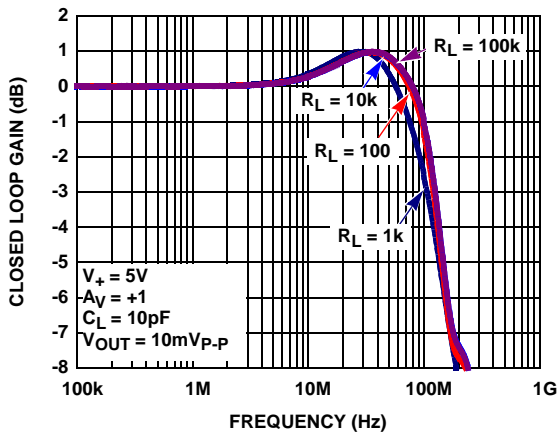


FIGURE 1. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD}

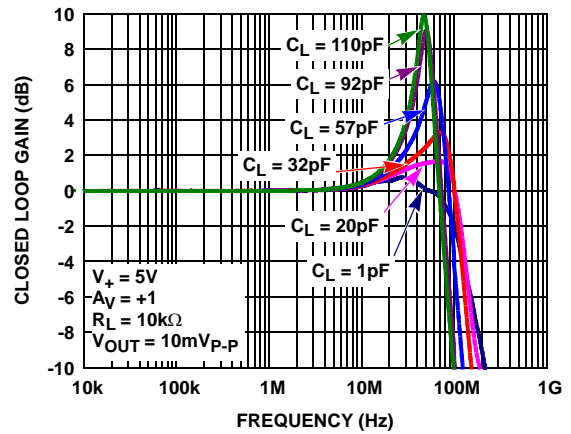


FIGURE 2. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD}

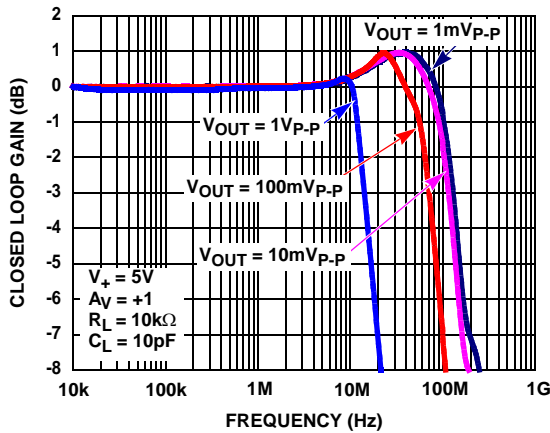


FIGURE 3. -3dB BANDWIDTH vs V_{OUT}

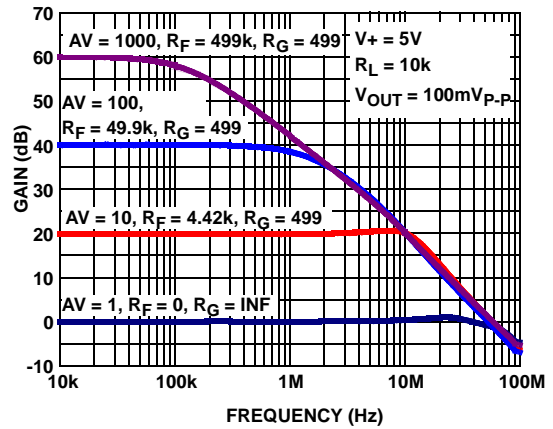


FIGURE 4. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

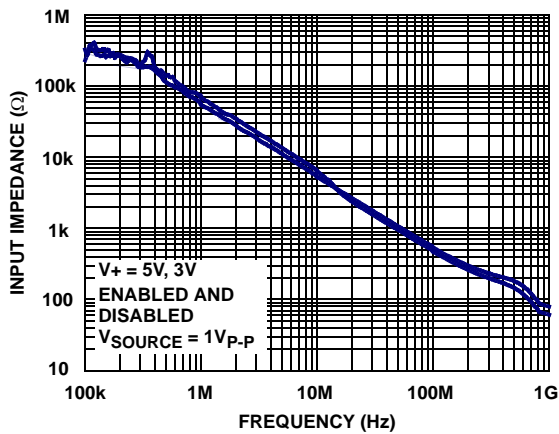


FIGURE 5. INPUT IMPEDANCE vs FREQUENCY

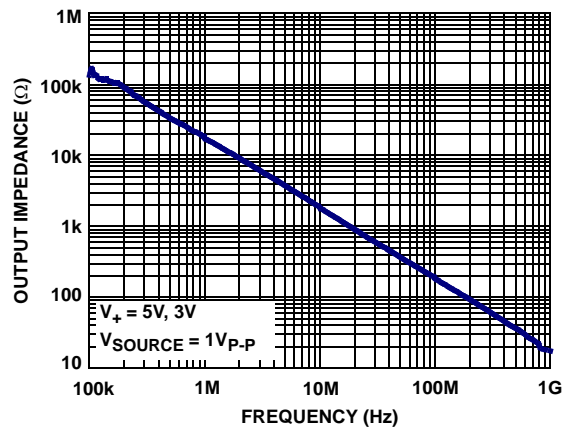


FIGURE 6. DISABLED OUTPUT IMPEDANCE vs FREQUENCY

Typical Performance Curves (Continued)

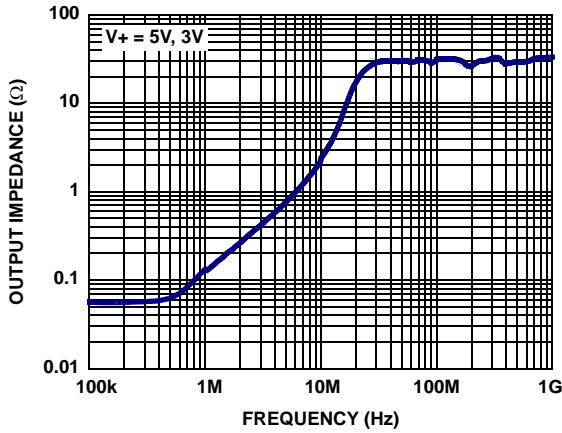


FIGURE 7. ENABLED OUTPUT IMPEDANCE vs FREQUENCY

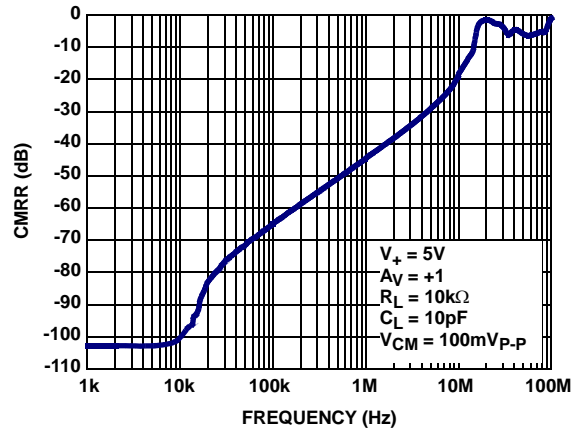


FIGURE 8. CMRR vs FREQUENCY

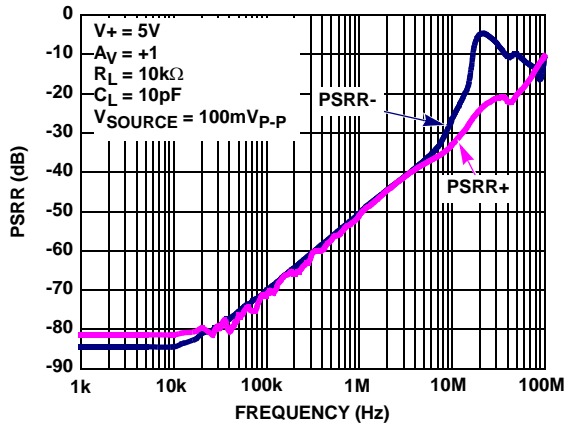


FIGURE 9. PSRR vs FREQUENCY

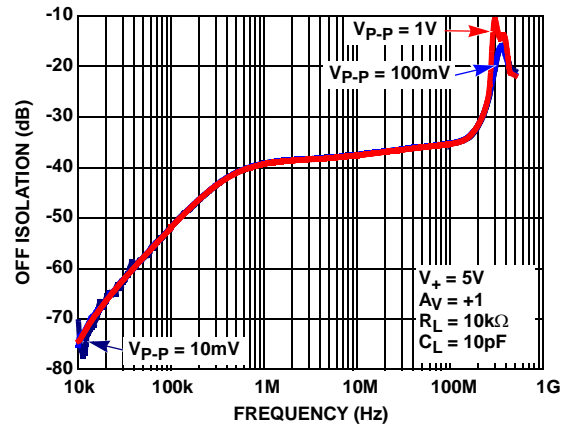


FIGURE 10. OFF ISOLATION vs FREQUENCY

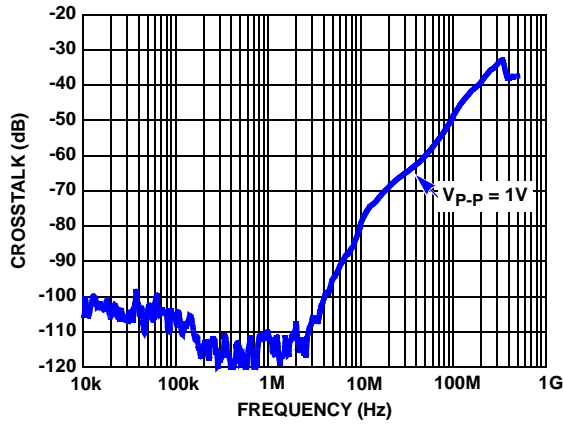


FIGURE 11. CHANNEL-TO-CHANNEL CROSSTALK vs FREQUENCY

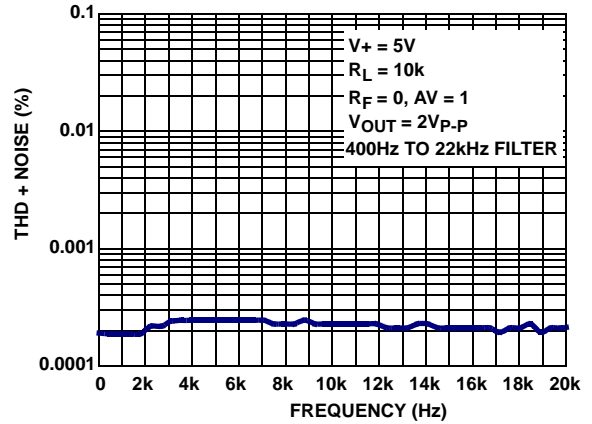


FIGURE 12. THD+N vs FREQUENCY

Typical Performance Curves (Continued)

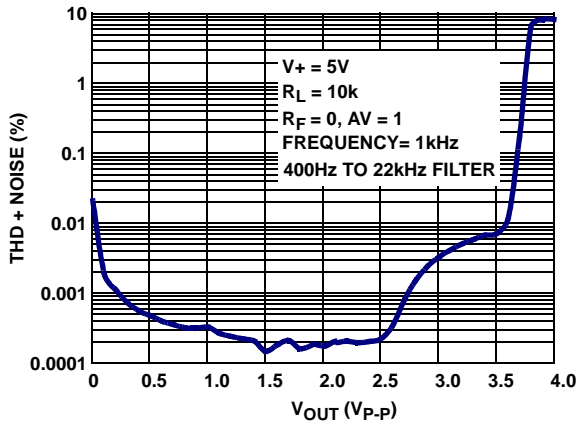


FIGURE 13. THD+N @ 1kHz vs V_{OUT}

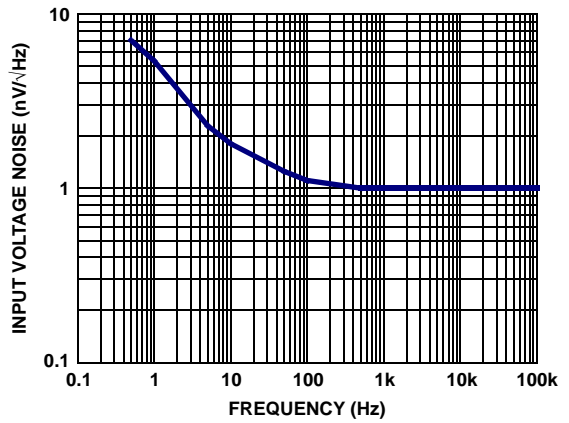


FIGURE 14. INPUT REFERRED NOISE VOLTAGE vs FREQUENCY

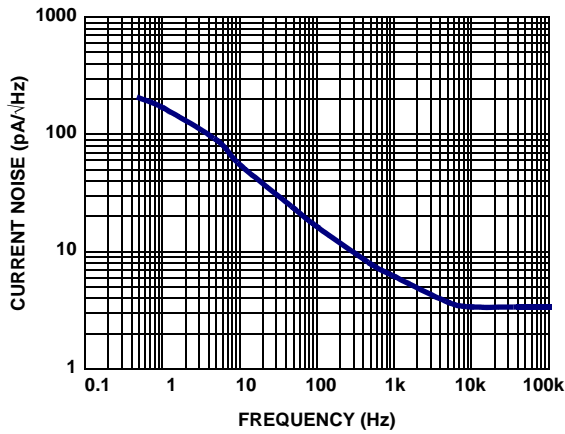


FIGURE 15. INPUT REFERRED NOISE CURRENT vs FREQUENCY

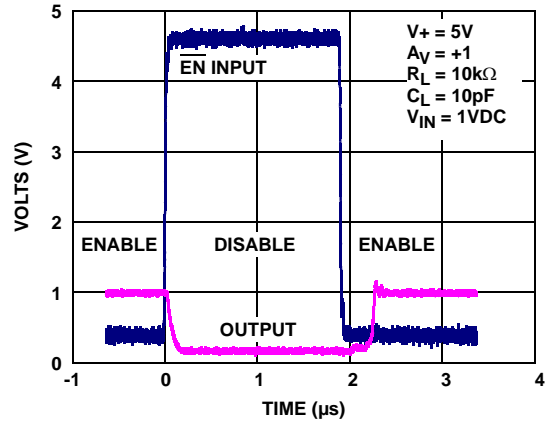


FIGURE 16. ENABLE/DISABLE TIMING

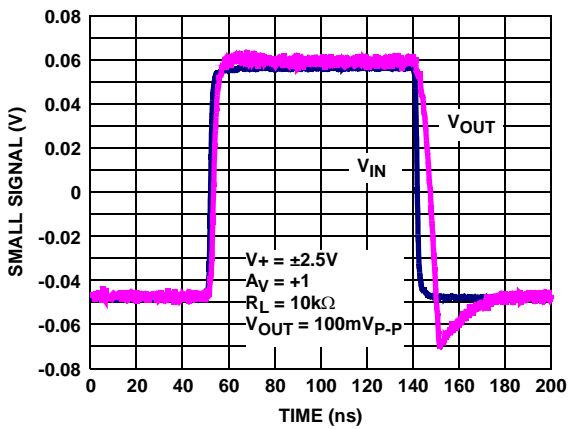


FIGURE 17. SMALL SIGNAL STEP RESPONSE

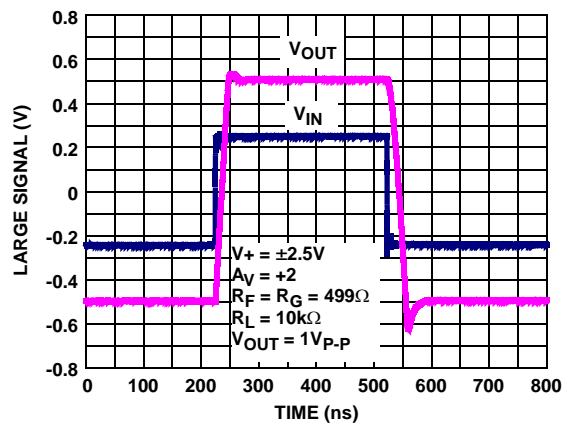


FIGURE 18. LARGE SIGNAL (1V) STEP RESPONSE

Typical Performance Curves (Continued)

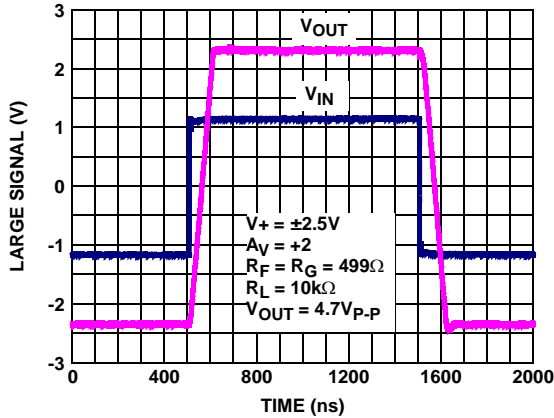


FIGURE 19. LARGE SIGNAL (4.7V) STEP RESPONSE

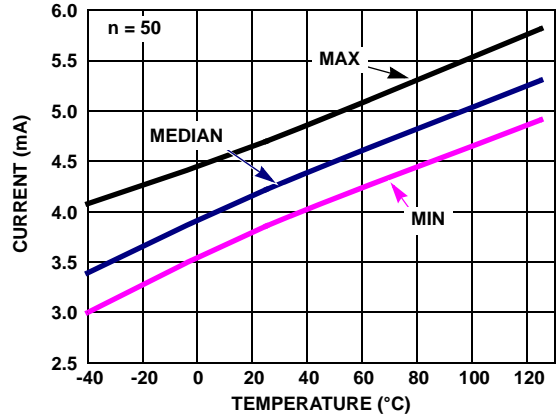


FIGURE 20. SUPPLY CURRENT vs TEMPERATURE, $V_S = \pm 2.5V$ ENABLED, $R_L = \text{INF}$

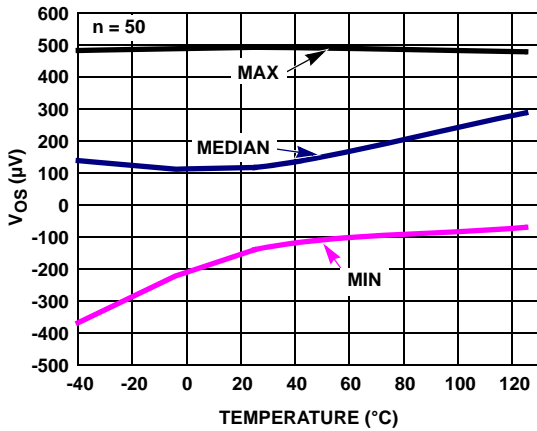


FIGURE 21. V_{OS} vs TEMPERATURE $V_S = \pm 2.5V$

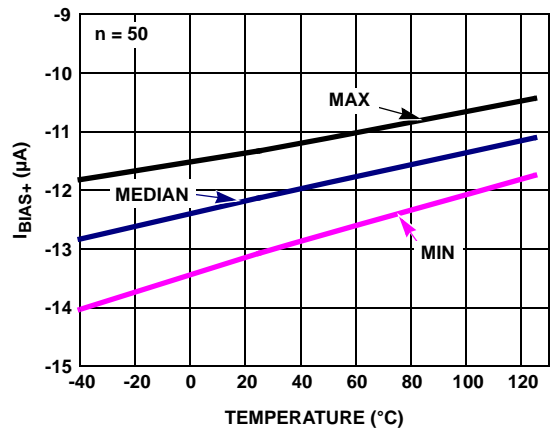


FIGURE 22. I_{BIAS+} vs TEMPERATURE $V_S = \pm 2.5V$

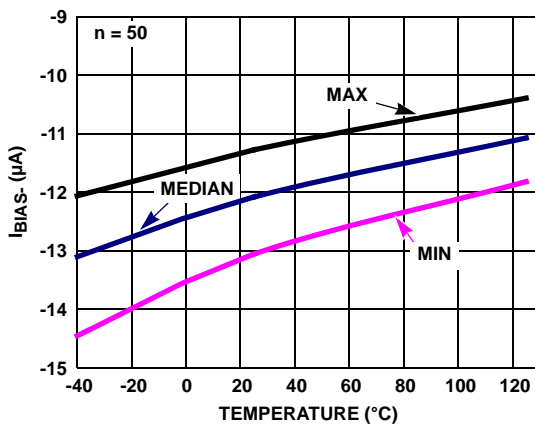


FIGURE 23. I_{BIAS-} vs TEMPERATURE $V_S = \pm 2.5V$

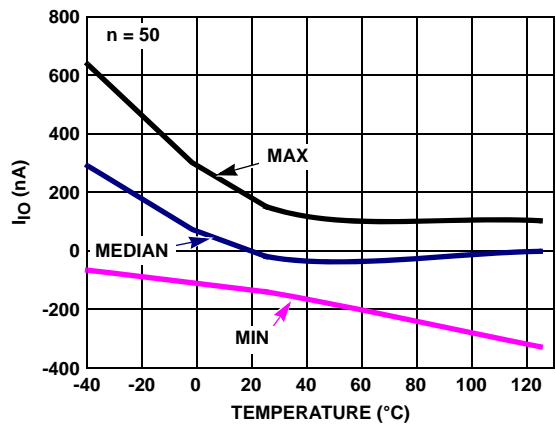


FIGURE 24. I_{IO} vs TEMPERATURE $V_S = \pm 2.5V$

Typical Performance Curves (Continued)

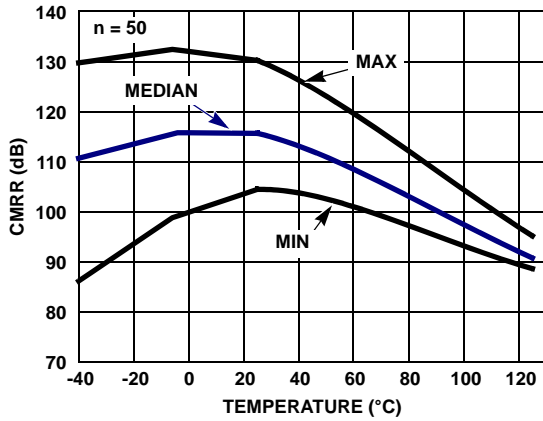


FIGURE 25. CMRR vs TEMPERATURE, VCM = 3.8V, VS = ±2.5V

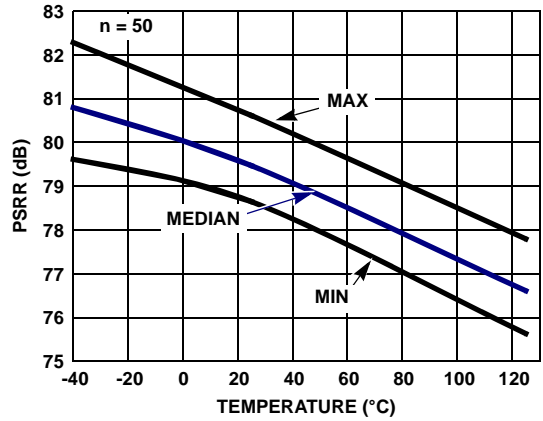


FIGURE 26. PSRR vs TEMPERATURE ±1.5V TO ±2.5V

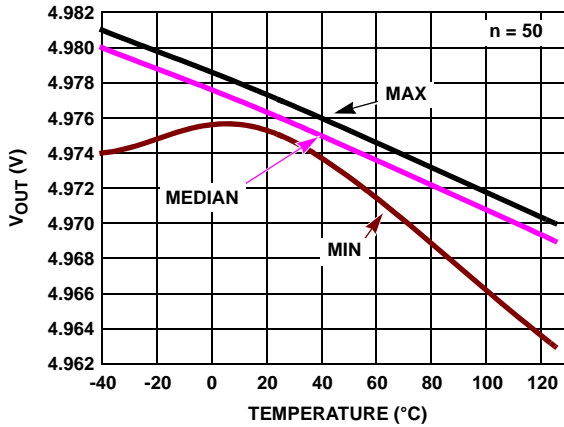


FIGURE 27. POSITIVE VOUT vs TEMPERATURE RL = 1k, VS = ±2.5V

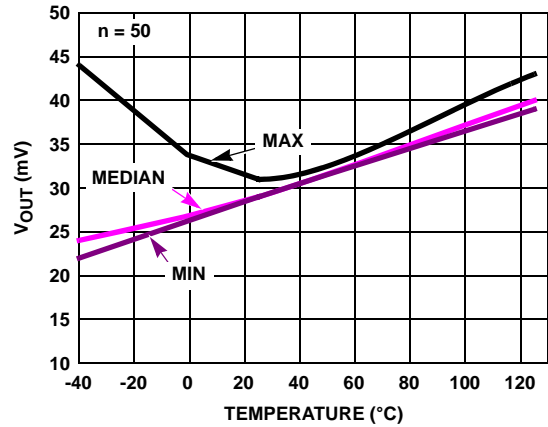
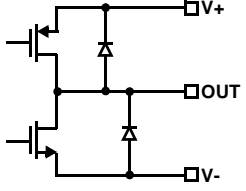
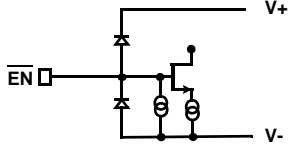


FIGURE 28. NEGATIVE VOUT vs TEMPERATURE RL = 1k, VS = ±2.5V

Pin Descriptions

ISL28190 (6 Ld SOT-23)	ISL28190 (6 Ld μTDFN)	ISL28290 (10 Ld MSOP)	ISL28290 (10 Ld μTQFN)	ISL28290 (8 Ld SOIC)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
4	2	2 (A) 8 (B)	1 (A) 7 (B)	2 (A) 6 (B)	IN- IN-_A IN-_B	Inverting input	 Circuit 1
3	3	3 (A) 7 (B)	2 (A) 6 (B)	3 (A) 5 (B)	IN+ IN+_A IN+_B	Non-inverting input	(See Circuit 1)
2	4	4	3	4	V-	Negative supply	

Pin Descriptions (Continued)

ISL28190 (6 Ld SOT-23)	ISL28190 (6 Ld μ TDFN)	ISL28290 (10 Ld MSOP)	ISL28290 (10 Ld μ TQFN)	ISL28290 (8 Ld SOIC)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
1	1	1 (A) 9 (B)	10 (A) 8 (B)	1 (A) 7 (B)	OUT OUT_A OUT_B	Output	 Circuit 2
6	6	10	9	8	V+	Positive supply	
5	5	5 (A) 6 (B)	4 (A) 5 (B)	N/A	$\overline{\text{EN}}$ $\overline{\text{EN}}_A$ $\overline{\text{EN}}_B$	Enable BAR pin internal pull-down; Logic "1" selects the disabled state; Logic "0" selects the enabled state.	 Circuit 3

Applications Information

Product Description

The ISL28190 and ISL28290 are voltage feedback operational amplifiers designed for communication and imaging applications requiring low distortion, very low voltage and current noise. Both parts feature high bandwidth while drawing moderately low supply current. The ISL28190 and ISL28290 use a classical voltage-feedback topology, which allows them to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier.

Enable/Power-Down

The ISL28190 and ISL28290 amplifiers are disabled by applying a voltage greater than 2V to the $\overline{\text{EN}}$ pin, with respect to the V- pin. In this condition, the output(s) will be in a high impedance state and the amplifier(s) current will be reduced to 13 μ A/Amp. By disabling the part, multiple parts can be connected together as a MUX. The outputs are tied together in parallel and a channel can be selected by the $\overline{\text{EN}}$ pin. The $\overline{\text{EN}}$ pin also has an internal pull-down. If left open, the $\overline{\text{EN}}$ pin will pull to the negative rail and the device will be enabled by default.

Input Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. Both parts have additional back-to-back diodes across the input terminals (as shown in Figure 29). In pulse applications where the input Slew Rate exceeds the Slew Rate of the amplifier, the possibility exists for the input protection diodes to become forward biased. This can cause excessive input current and distortion at the outputs. If overdriving the inputs is necessary, the external input current must never exceed 5mA. An

external series resistor may be used to limit the current, as shown in Figure 29.

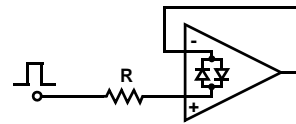


FIGURE 29. LIMITING THE INPUT CURRENT TO LESS THAN 5mA

Using Only One Channel

The ISL28290 is a Dual channel op amp. If the application only requires one channel when using the ISL28290, the user must configure the unused channel to prevent it from oscillating. Oscillation can occur if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the negative input and ground the positive input (as shown in Figure 30).

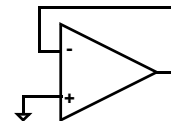


FIGURE 30. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Low impedance ground plane construction is essential. Surface mount components are recommended, but if leaded components are used, lead lengths should be as short as possible. The power supply pins must be well bypassed to

reduce the risk of oscillation. The combination of a 4.7µF tantalum capacitor in parallel with a 0.01µF capacitor has been shown to work well when placed at each supply pin.

For good AC performance, parasitic capacitance should be kept to a minimum, especially at the inverting input. When ground plane construction is used, it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of additional series inductance. Use of sockets, particularly for the SO package, should be avoided if possible. Sockets add parasitic inductance and capacitance, which will result in additional peaking and overshoot.

Current Limiting

The ISL28190 and ISL28290 have no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device. This is why output short circuit current is specified and tested with $R_L = 10\Omega$.

Power Dissipation

It is possible to exceed the +125°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related as follows:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} \times PD_{MAXTOTAL}) \quad (EQ. 1)$$

where:

- $PD_{MAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated as follows:

$$PD_{MAX} = 2 \times V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad (EQ. 2)$$

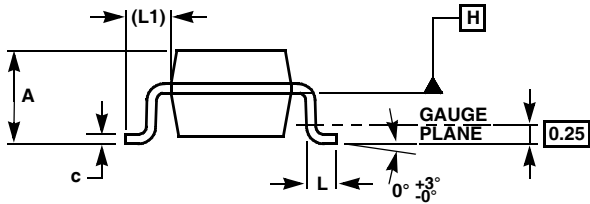
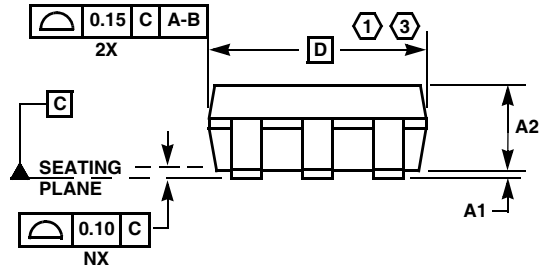
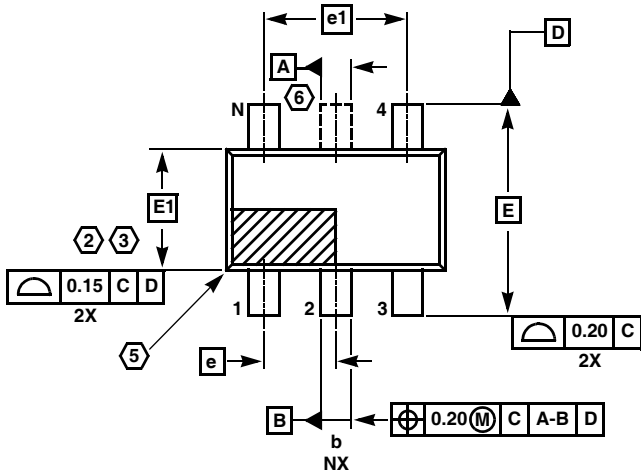
where T_{MAX} = Maximum ambient temperature

- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Supply voltage
- I_{MAX} = Maximum supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

SOT-23 Package Family

MDP0038

SOT-23 PACKAGE FAMILY



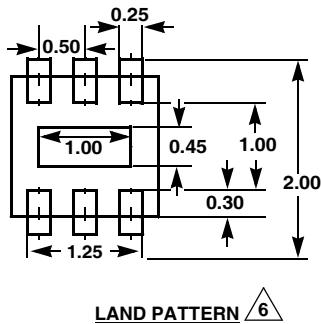
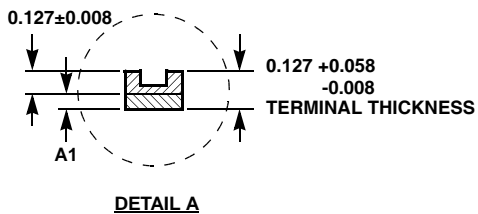
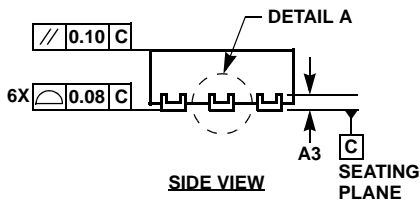
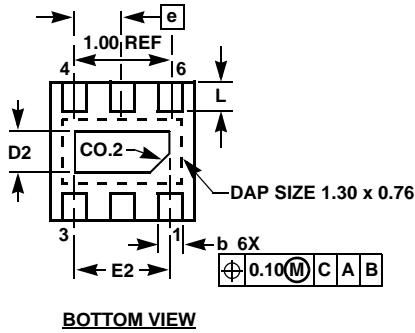
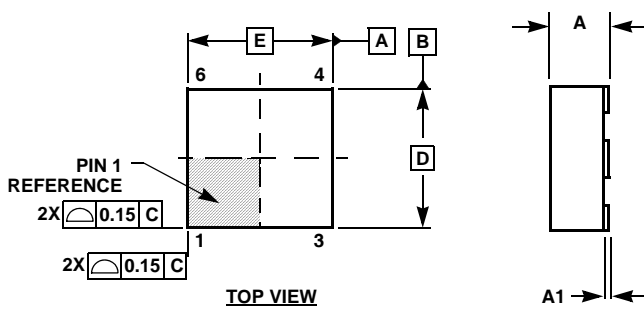
SYMBOL	MILLIMETERS		TOLERANCE
	SOT23-5	SOT23-6	
A	1.45	1.45	MAX
A1	0.10	0.10	±0.05
A2	1.14	1.14	±0.15
b	0.40	0.40	±0.05
c	0.14	0.14	±0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	±0.10
L1	0.60	0.60	Reference
N	5	6	Reference

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).

Ultra Thin Dual Flat No-Lead Plastic Package (UTDFN)



L6.1.6x1.6A

6 LEAD ULTRA THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

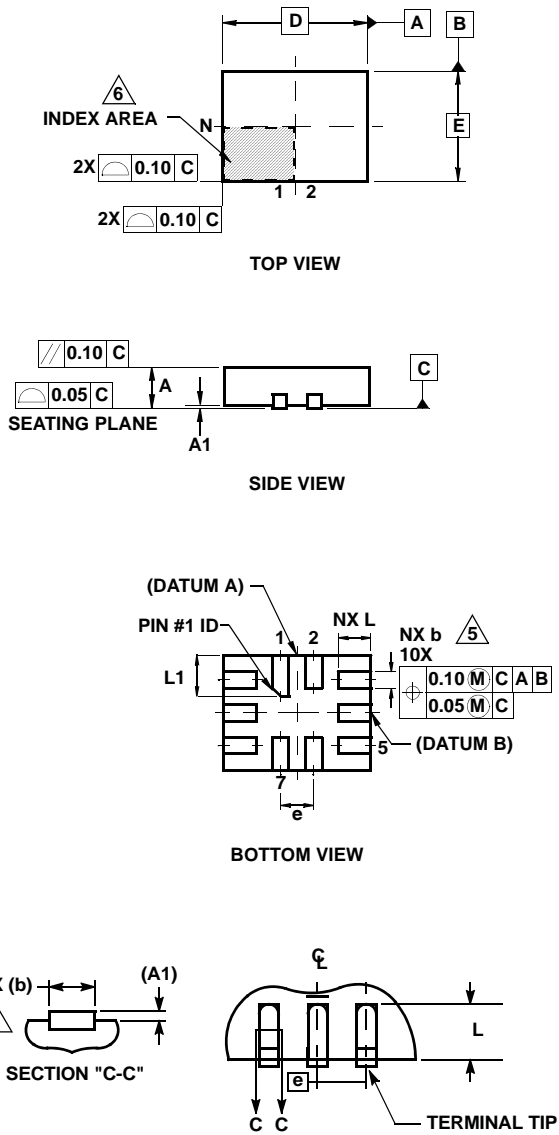
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3	0.127 REF			-
b	0.15	0.20	0.25	-
D	1.55	1.60	1.65	4
D2	0.40	0.45	0.50	-
E	1.55	1.60	1.65	4
E2	0.95	1.00	1.05	-
e	0.50 BSC			-
L	0.25	0.30	0.35	-

Rev. 1 6/06

NOTES:

1. Dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall not exceed 0.08mm.
3. Warpage shall not exceed 0.10mm.
4. Package length/package width are considered as special characteristics.
5. JEDEC Reference MO-229.
6. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.

Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)



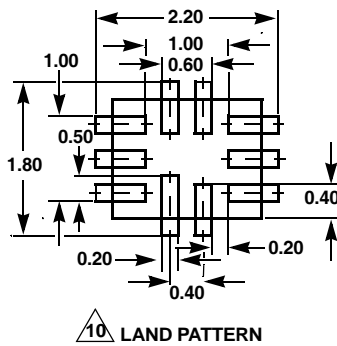
L10.1.8x1.4A
10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3	0.127 REF			-
b	0.15	0.20	0.25	5
D	1.75	1.80	1.85	-
E	1.35	1.40	1.45	-
e	0.40 BSC			-
L	0.35	0.40	0.45	-
L1	0.45	0.50	0.55	-
N	10			2
Nd	2			3
Ne	3			3
θ	0	-	12	4

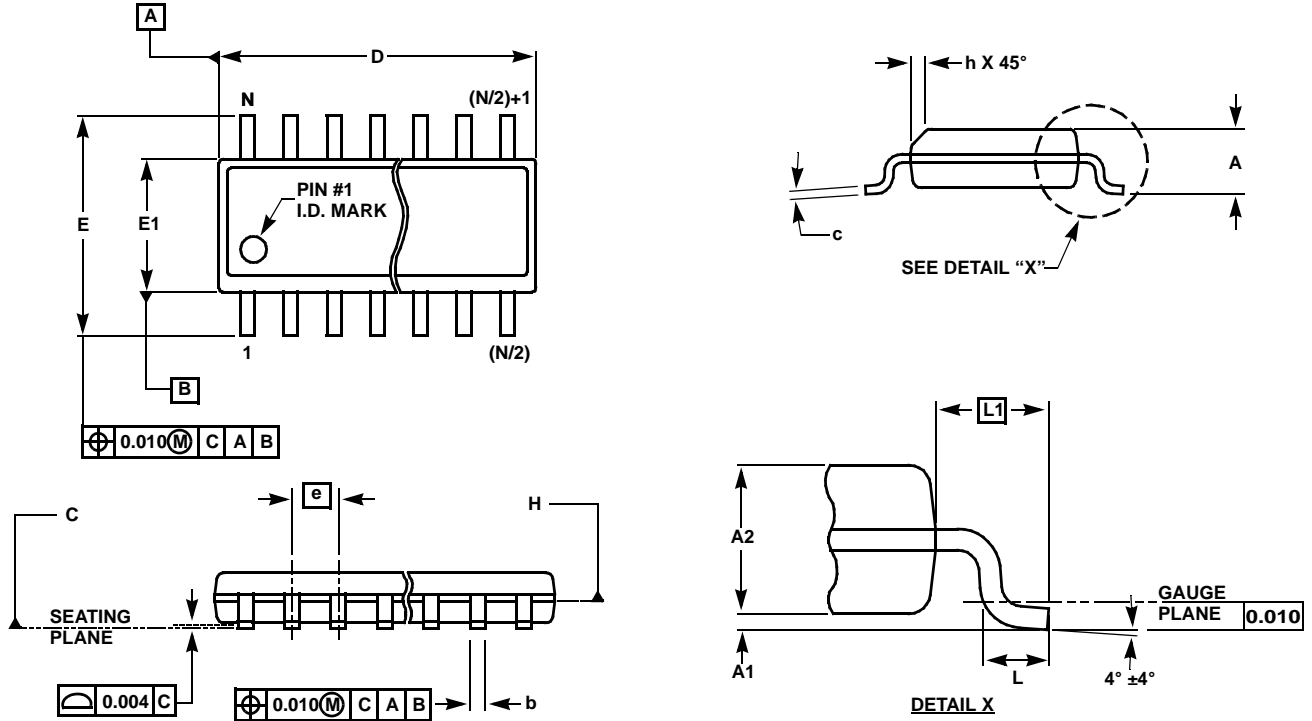
Rev. 3 6/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. JEDEC Reference MO-255.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.



Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

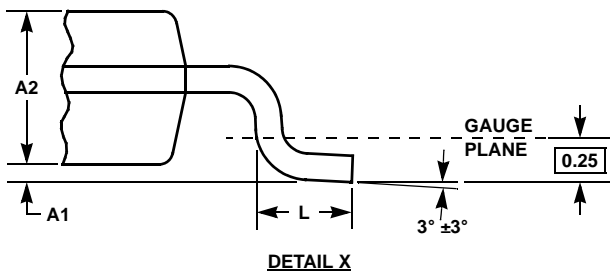
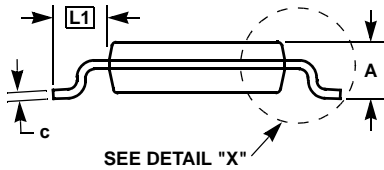
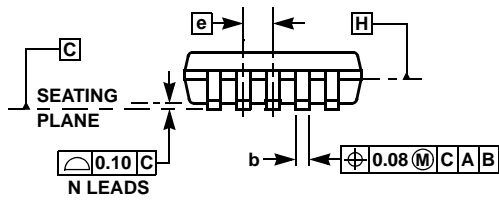
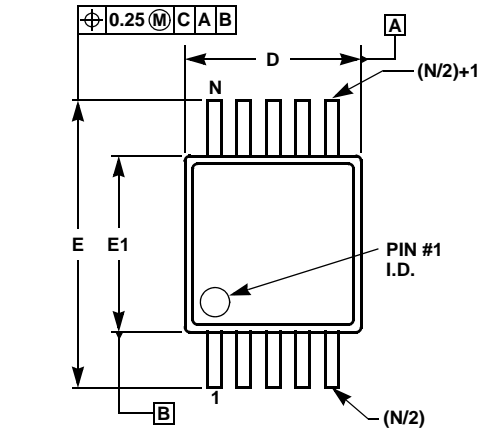
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	± 0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	± 0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	± 0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	± 0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	± 0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	± 0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	± 0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	± 0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Mini SO Package Family (MSOP)



MDP0043

MINI SO PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	MSOP8	MSOP10		
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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