FAIRCHILD SEMICONDUCTOR®

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FAN5182
Adjustable Output 1, 2, or 3-Phase Synchronous Buck Controller

Features

- Selectable 1-, 2-, or 3-phase operation at up to 1MHz per phase
- ±2% Worst-case differential sensing error over temperature
- Externally adjustable 0.8V to 5V output from a 12V supply
- Logic-level PWM outputs for interface to external high-power drivers
- Active current balancing between all phases
- Built-in power-good/crowbar functions
- Programmable over current protection with adjustable latch-off delay

Applications

- Auxiliary supplies
- DDR memory supplies
- Point-of-load supplies

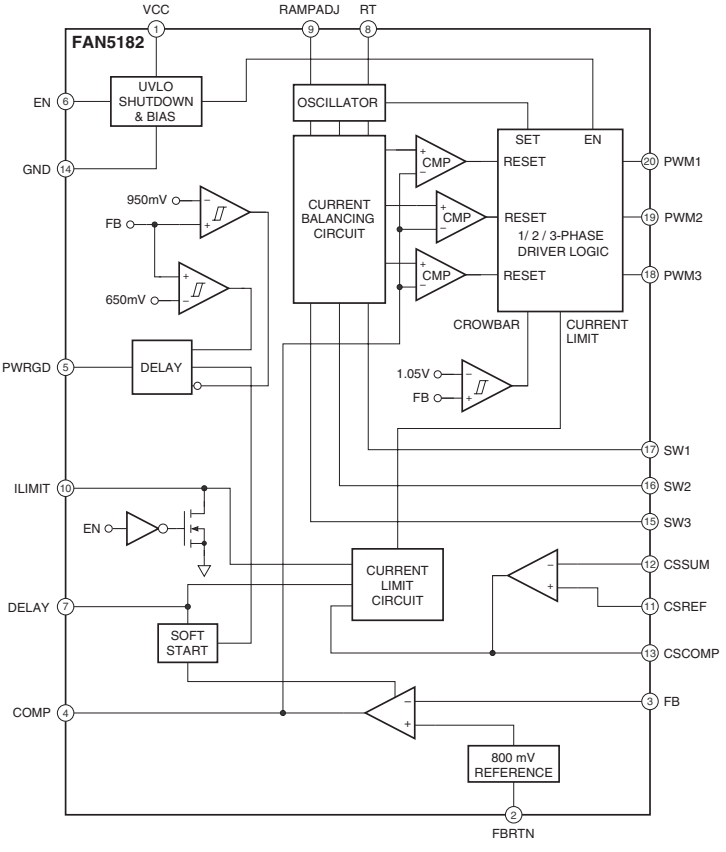
Description

The FAN5182 is a highly efficient multi-phase synchronous buck switching regulator controller optimized for converting a 12V main supply into a high-current low voltage supply for use in point-of-load (POL) applications. It uses a multi-loop PWM architecture to drive the logic-level outputs at a programmable switching frequency that can be optimized for regulator size and efficiency. The phase relationship of the output signals can be programmed to provide 1, 2, or 3-phase operation, allowing for construction of up to three complementary interleaved buck switching stages.

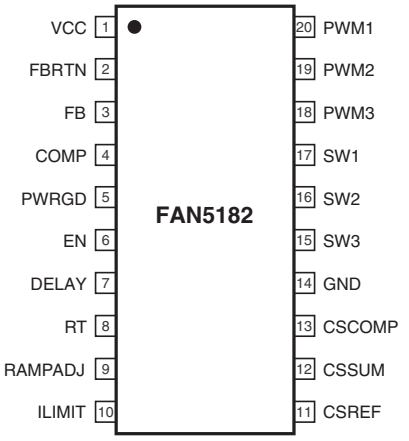
The FAN5182 also provides accurate and reliable over-current protection and adjustable current limiting.

FAN5182 is specified over the commercial temperature range of 0°C to +85°C and is available in a 20-lead QSOP package.

Block Diagram



Pin Assignment



QSOP-20L

Pin Description

Pin #	Pin Name	Pin Description
1	VCC	Supply Voltage for the Device.
2	FBRTN	Feedback Return. Voltage error amplifier reference for remote sensing of the output voltage.
3	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage. An external resistor divider between the output and FBRTN connected to this pin sets the output voltage. This pin is also the reference point for the power good and crowbar comparators.
4	COMP	Error Amplifier Output and Compensation Pin.
5	PWRGD	Power Good Output. Open-drain output that signals when the output voltage is outside the proper operating range.
6	EN	Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs and pulls the PWRGD output low.
7	DELAY	Soft-Start Delay and Current Limit Latch-Off Delay Setting Input. An external resistor and capacitor connected between this pin and GND set the soft-start ramp-up time and the overcurrent latch-off delay time.
8	RT	Frequency Setting Resistor Input. An external resistor connected between this pin and GND sets the oscillator frequency of the device.
9	RAMPADJ	PWM Ramp Current Input. An external resistor from the converter input voltage to this pin sets the internal PWM ramp.
10	ILIMIT	Current Limit Setpoint/Enable Output. An external resistor connected from this pin to GND sets the current limit threshold of the converter. This pin is actively pulled low when the FAN5182 EN input is low, or when VCC is below its UVLO threshold, to signal to the driver IC that the driver high-side and low-side outputs should go low.
11	CSREF	Current Sense Reference Voltage Input. The voltage on this pin is used as the reference for the current sense amplifier. This pin should be connected to the common point of the output inductors.
12	CSSUM	Current Sense Summing Node. External resistors from each switch node to this pin sum the average inductor currents together to measure the total output current.
13	CSCOMP	Current Sense Compensation Point. A resistor and a capacitor from this pin to CSSUM determine the gain of the current sense amplifier.
14	GND	Ground. All internal biasing and the logic output signals of the device are referenced to this ground.
15–17	SW3 To SW1	Current Balance Inputs. These are inputs for measuring the current level in each phase. The SW pins of unused phases should be left open.
18–20	PWM3 To PWM1	Logic-Level PWM Outputs. Each output is connected to the input of an external MOSFET driver such as the FAN5009. Connecting the PWM3 output to GND causes that phase to turn off, allowing the FAN5182 to operate as a 1- or 2-phase controller.

Absolute Maximum Ratings (Note 1)

Parameter	Min.	Max.	Unit
VCC	-0.3	+15	V
FBRTN	-0.3	+0.3	V
EN, DELAY, ILIMIT, RT, PWM1-PWM3, COMP	-0.3	5.5	V
SW1-SW3	-5	+25	V
All Other Inputs and Outputs	-0.3	VCC + 0.3	V
Operating Junction Temperature, T_J	0	+125	°C
Storage Temperature	-65	+150	°C
Lead Soldering Temperature (10 seconds)		300	°C
Lead Infrared Temperature (15 seconds)		260	°C
Thermal Resistance Junction-to-Case, (θ_{JC})		38	°C/W
Thermal Resistance Junction-to- Ambient, (θ_{JA}) (Note 2)		90	°C/W

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Supply Voltage Range	10.8	12	13.2	V
Operating Ambient Temperature	0		+85	°C

Notes:

1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified all other voltages are referenced to GND.
2. Junction to ambient thermal resistance, θ_{JA}, is a strong function of PCB material, board thickness, thickness and number of copper planes, number of via used, diameter of via used, available copper surface, and attached heat sink characteristics. Measured with the device mounted on a board of FR-4 material, 0.063” thickness, no copper plane and zero airflow.

Electrical Characteristics

V_{CC} = 12V, FBRTN = GND. ● Indicates specifications over operating ambient temperature range. (Note 1)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
OSCILLATOR							
Frequency Range	f_{OSC}		●	0.25		3	MHz
Frequency Variation	f_{PHASE}	R_T = 332kΩ, 3-phase T_A = 25°C, R_T = 154kΩ, 3-phase T_A = 25°C, R_T = 100kΩ, 3-phase	●	155	200 400 600	245	kHz
Output Voltage	V_{RT}	R_T = 100kΩ to GND			2.0		V
RAMPADJ Output Voltage	$V_{RAMPADJ}$	RAMPADJ - FB - 2KΩ x $I_{RAMPADJ}$ (with $I_{RAMPADJ}$ set to 20 µA)	●	-50		+50	mV
RAMPADJ Input Current Range (Note 2)	$I_{RAMPADJ}$			0		100	µA
VOLTAGE ERROR AMPLIFIER							
Output Voltage Low						0.3	V
Output Voltage High				3.1			V
Accuracy	V_{FB}	Referenced to FBRTN	●	784	800	816	mV
Input Bias Current	I_{FB}	FB = 800mV	●	-4	±1	+4	µA
Line Regulation	ΔV_{FB}	V_{CC} = 10V to 14V			0.05		%
FBRTN Current	I_{FBRTN}		●		100	140	µA
Output Current	$I_{O(ERR)}$	FB forced to V_{OUT} - 3%			500		µA
DC Gain (Note 2)					87		dB
Gain Bandwidth Product (Note 2)	$G_{BW(ERR)}$	COMP = FB			20		MHz
Slew Rate (Note 2)		C_{COMP} = 10pF			10		V/µs
CURRENT SENSE AMPLIFIER							
Offset Voltage	$V_{OS(CSA)}$	CSSUM-CSREF (See Figure 1.)	●	-5.5		+5.5	mV
Input Bias Current	$I_{BIAS(CSSUM)}$		●	-50		+50	nA
DC Gain (Note 2)					70		dB
Gain Bandwidth Product (Note 2)	$GBW_{(CSA)}$				10		MHz
Slew Rate (Note 2)		C_{CSCOMP} = 10pF			10		V/µs
Input Common-Mode Range		CSSUM & CSREF		0		V_{CC}-2.5	V
Output Voltage Low						0.1	V
Output Voltage High				V_{CC}-2.5			V
Output Current	I_{CSCOMP}				500		µA
CURRENT BALANCE CIRCUIT							
Common-Mode Range (Note 2)	$V_{SW(X)CM}$			-600		+200	mV
Input Resistance	$R_{SW(X)}$	SW(X) = 0V	●	20	30	40	kΩ
Input Current	$I_{SW(X)}$	SW(X) = 0V	●	4	7	10	µA
Input Current Matching	$\Delta I_{SW(X)}$	SW(X) = 0V	●	-7		+7	%
CURRENT LIMIT COMPARATOR							
Output Voltage: Normal Mode	$V_{ILIMIT(NM)}$	EN > 2V, R_{ILIMIT} = 250kΩ	●	2.9	3	3.1	V
Output Voltage: Shutdown Mode	$V_{ILIMIT(SD)}$	EN < 0.8V, I_{ILIMIT} = -100µA	●			400	mV
Output Current: Normal Mode	$I_{ILIMIT(NM)}$	EN > 2V, R_{ILIMIT} = 250kΩ			12		µA
Maximum Output Current			●	60			µA

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Current Limit Threshold Voltage	V_{CL}	V_{CSREF} - V_{CSCOMP}, R_{ILIMIT} = 250kΩ		105	125	145	mV
Current Limit Setting Ratio		V_{CL}/I_{ILIMIT}			10.4		mV/µA
DELAY Normal Mode Voltage	$V_{DELAY(NM)}$	R_{DELAY} = 250kΩ		2.9	3	3.1	V
DELAY Overcurrent Threshold	$V_{DELAY(OC)}$	R_{DELAY} = 250kΩ		1.7	1.8	1.9	V
Latch-Off Delay Time (Note 2)	t_{DELAY}	R_{DELAY} = 250kΩ, C_{DELAY} = 12nF			1.5		ms
SOFT-START							
Output Current, Soft-Start Mode	$I_{DELAY(SS)}$	During startup, DELAY < 2.4V	●	15	20	25	µA
Soft-Start Delay Time (Note 2)	$t_{DELAY(SS)}$	R_{DELAY} = 250kΩ, C_{DELAY} = 12nF			500		µs
ENABLE INPUT							
Input Low Voltage	$V_{IL(EN)}$		●			0.8	V
Input High Voltage	$V_{IH(EN)}$		●	2.0			V
Input Hysteresis Voltage					100		mV
Input Current	$I_{IN(EN)}$		●	-1		+1	µA
POWER GOOD COMPARATOR							
Undervoltage Threshold	$V_{PWRGD(UV)}$	Relative to FBRTN	●	600	660	720	mV
Overvoltage Threshold	$V_{PWRGD(OV)}$	Relative to FBRTN	●	880	940	1000	mV
Ouput Low Voltage	$V_{OL(PWRGD)}$	$I_{PWRGD(SINK)}$ = 4mA	●		225	400	mV
Power Good Delay Time					200		ns
Crowbar Trip Point	$V_{CROWBAR}$	Relative to FBRTN	●	0.970	1.05	1.105	V
Crowbar Reset Point		Relative to FBRTN	●	550	650	750	mV
Crowbar Delay Point (Note 2)	$t_{CROWBAR}$	Overvoltage to PWM going low			400		ns
PWM OUTPUTS							
Output Low Voltage	$V_{OL(PWM)}$	$I_{PWM(SINK)}$ = 400µA	●		160	500	mV
Output High Voltage	$V_{OH(PWM)}$	$I_{PWM(SOURCE)}$ = -400µA	●	4.0	5		V
SUPPLY							
DC Supply Current			●		5	10	mA
UVLO THreshold Voltage	V_{UVLO}	V_{CC} rising	●	6.5	6.9	7.3	V
UVLO Hysteresis			●	0.7	0.9	1.1	V

Notes:
1. All limits at operating temperature extremes are guaranteed by design, characterization and statistical quality control.
2. Guaranteed by design, not tested in production.

Test Circuit

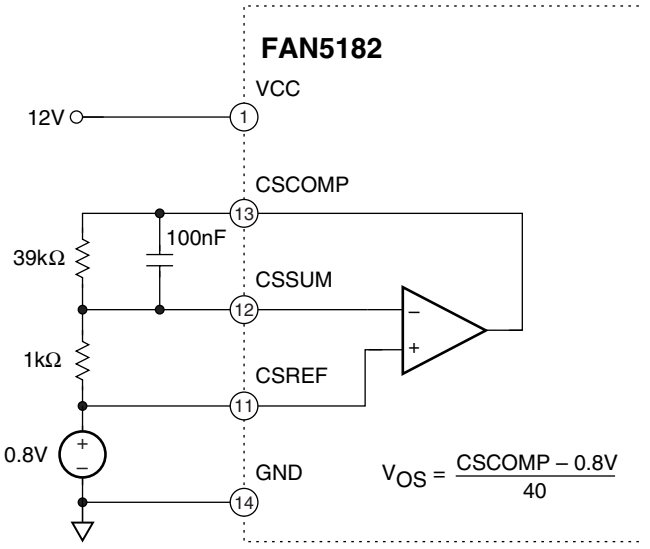


Figure 1. Current Sense Amplifier V_{OS}

Typical Characteristics

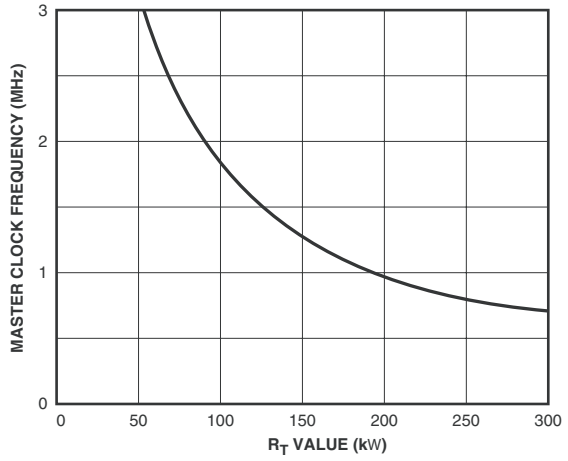


Figure 2. Master Clock Frequency

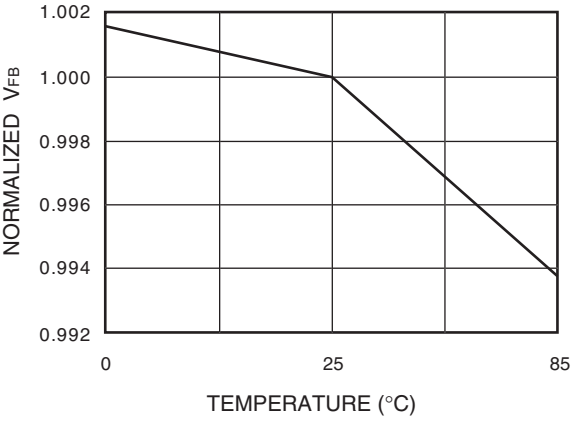


Figure 4. Normalized V_{FB} vs. Temperature

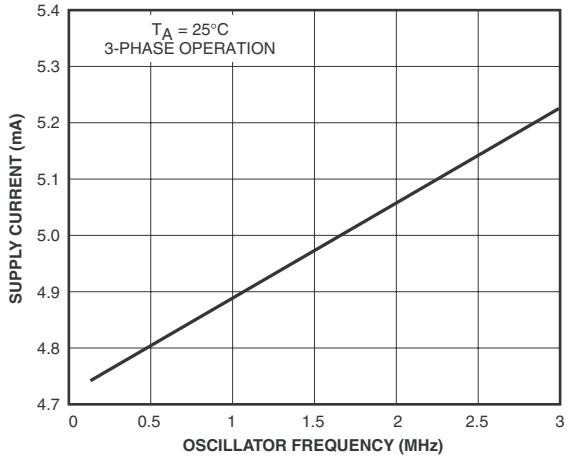


Figure 3. Supply Current vs. Osc. Frequency

Application Circuit

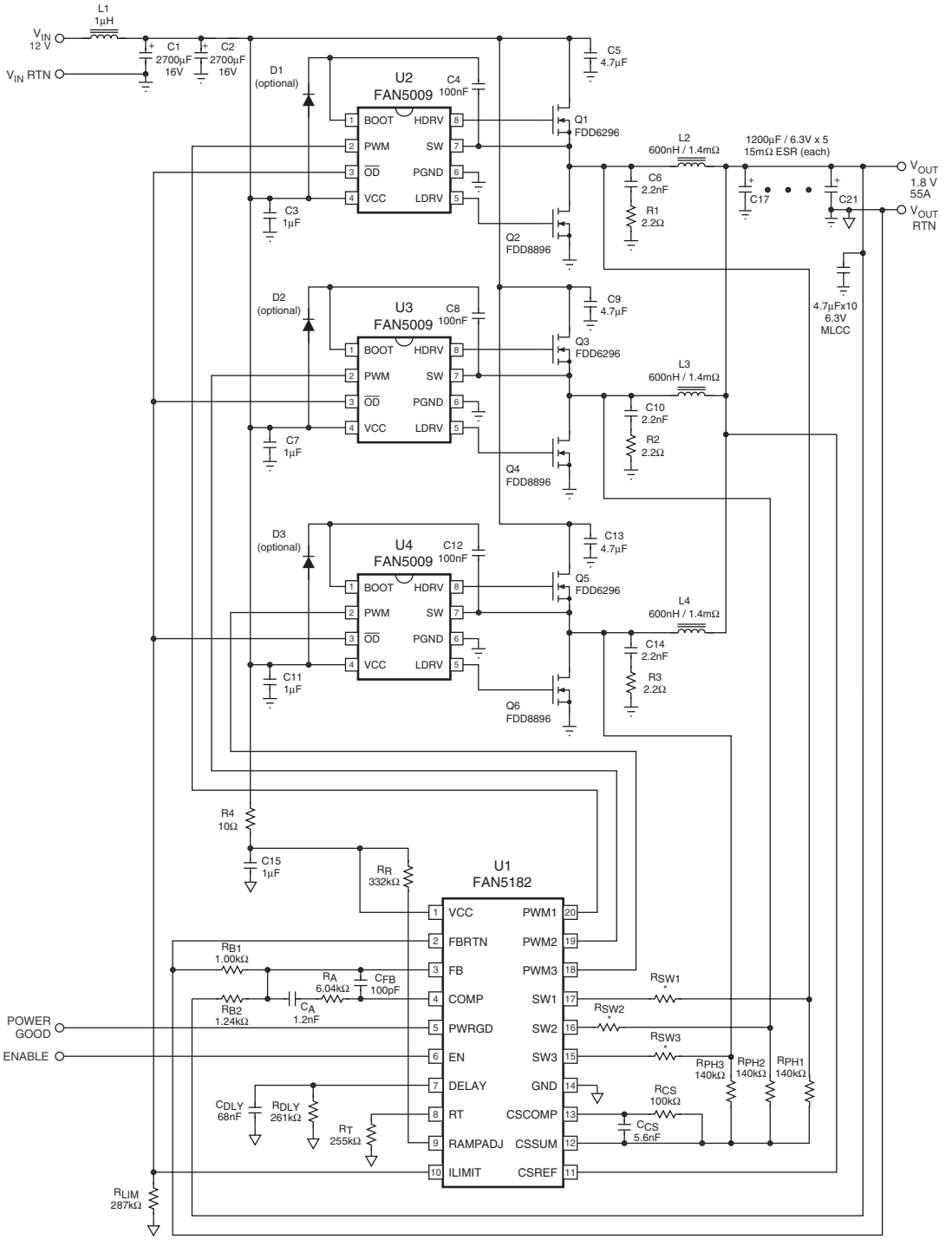


Figure 5. 1.8V, 55A Application Circuit

(Consult Fairchild Sales for an updated version of the Application Circuit)

Theory of Operation

The FAN5182 combines a multi-loop, fixed frequency PWM control with multi-phase logic outputs for use in 1-, 2-, and 3-phase synchronous buck point-of-load power supplies. Multi-phase operation is important for producing the high current and low voltage demanded by auxiliary supplies in desktop computers, workstations, and servers. Handling high current in a single-phase converter places high thermal stress on components such as inductors and MOSFETs, therefore is not preferred.

The multi-loop control of the FAN5182 ensures a stable, high performance topology for:

- Balancing current and thermal between/among phases
- Fast response at the lowest possible switching frequency and output decoupling
- Reducing switching losses due to low frequency operation
- Tight line and load regulation
- Reducing output ripple due to multiphase cancellation
- Better noise immunity to facilitate PCB layout

Start-up Sequence

During start-up, the number of operational phases and their phase relationship are determined by the internal circuitry that monitors the PWM outputs. Normally, the FAN5182 operates as a 3-phase PWM controller. Grounding the PWM3 pin programs for 1- or 2-phase operation.

When the FAN5182 is enabled, the controller outputs a voltage on PWM3 which is approximately 675mV. An internal comparator checks this pin's voltage versus a threshold of 300mV. If the PWM3 pin is grounded, it is below the threshold and the phase 3 is disabled. The output resistance of the PWM pin is approximately 5kΩ during this detection period. Any external pull-down resistance connected to the PWM pin should not be less than 25kΩ to ensure proper operation. PWM1 and PWM2 are disabled during the phase detection interval, which occurs during the first two clock cycles of the internal oscillator. After this time, if the PWM3 output is not grounded, the 5kΩ resistance is disconnected and PWM3 switches between 0V and 5V. If the PWM3 output is grounded, the controller will operate in 1 and/or 2-phase.

The PWMs output logic-level signals in order to interface with external gate drivers such as the FAN5009. Since each phase is able to operate close to 100% duty cycle, more than one PWM output can be on at the same time.

Master Clock Frequency

The clock frequency of the FAN5182 is set by an external resistor connected from the RT pin to ground. The frequency setting follows the graph shown in Figure 2. To determine the frequency per phase, divide the clock frequency by the number of phases in use. One exception is single phase operation, in which the clock frequency is set to be twice the single phase frequency.

Output Voltage Differential Sensing

The FAN5182 uses a differential low offset voltage error amplifier to maintain ±2% differential sensing accuracy over temperature. The output voltage is sensed between the FB and FBRTN pins. The power supply output connects to the FB pin through a resistor divider, and the FBRTN pin should be connected directly to the remote sense ground. The internal precision reference is referenced to FBRTN, which has a typical current of 100µA to allow accurate remote sensing. The internal error amplifier compares the precision reference to the FB pin to regulate the output voltage.

Output Current Sensing

The FAN5182 uses a current sense amplifier (CSA) to monitor the total output current for current limit detection. Sensing the load current at the output gives the total average current being delivered to the load, which is an inherently more accurate method than peak current detection or sampling the current across a sense element, such as the low-side MOSFET. This amplifier can be configured several ways depending on the objectives of the system design:

- Output inductor DCR sensing without a thermistor for lowest cost
- Output inductor DCR sensing with a thermistor for improved accuracy and moderate cost
- Discrete resistor sensing for the best accuracy

The positive input of the CSA is connected to the CSREF pin, and the CSREF is tied to the power supply output. The inverting input of the CSA, CSSUM, is the summing node of load current sense through sensing elements (such as the switch node side of the output inductors). The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier, and a filter capacitor is placed in parallel with this resistor. The gain of the amplifier is programmable by adjusting the feedback resistor. The current information is then given as the difference between CSREF and CSCOMP. This difference signal is then used as a differential input for the current limit comparator.

To provide the best accuracy for sensing current, the CSA is designed to have low input offset voltage. The CSA gain is determined by external resistors, so that it can be set very accurately.

Current Control Loop and Thermal Balance

The FAN5182 adopts low side MOSFET R_{DSON} sensing for phase current balance. The sensed individual phase current is combined with a fixed internal ramp, then compared with the common voltage error amplifier output to balance phase current. This current balance information is independent of the average output current information used for current limit described previously.

The magnitude of the internal ramp can be set to optimize transient response of the system. It also tracks the supply voltage for better line regulation and transient response. A resistor connected from the power supply input to the RAMPADJ pin determines the slope of the internal PWM ramp. Resistors R_{SW1} through R_{SW3} (see Figure 5) can be used for adjusting phase current balance. It's recommended to put placeholders for these resistors during the initial PCB layout, so that phase current balance fine adjustments can be made on bench if necessary.

To increase the current in any given phase, make R_{SW} for that phase larger (make $R_{SW} = 0\Omega$ for the hottest phase as the starting point). Increasing R_{SW} to 500Ω could typically make a substantial increase in this particular phase current. Increase each R_{SW} value by small amounts to optimize phase current balance, starting with the coolest phase first.

Voltage Control Loop

A high gain-bandwidth voltage error amplifier is used for the voltage control loop. The non-inverting input of the error amplifier is derived from the internal 800mV reference. The output of the error amplifier, the COMP pin sets the termination voltage for the internal PWM ramps plus sensed phase current.

The inverting input (FB) is tied to the center point of a resistor divider from the output voltage sense point. The closed loop compensation is realized through the compensator networks connecting to the FB and COMP pins.

Soft Start

The soft-start rise time of the output voltage is set by a parallel capacitor and resistor between the DELAY pin and ground. The resistor capacitor (RC) time constant also determines the current limit latch off delay time as explained in the following section. In UVLO or when EN is logic low, the DELAY pin is held to ground. After the UVLO threshold is reached and EN is in logic high state, the DELAY capacitor is charged with an internal 20µA current source. The output voltage follows the ramping voltage on the DELAY pin to limit the inrush current. The soft-start time depends on the value of C_{DLY}, with a secondary effect from R_{DLY}.

If either EN is logic low or V_{CC} drops below UVLO, the DELAY capacitor resets to ground, and is ready for another soft-start cycle.

Figure 6. Typical Startup Waveforms shows a typical soft-start sequence for the FAN5182.

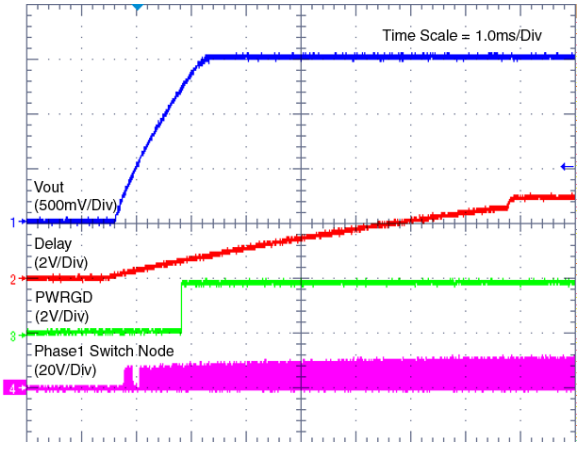


Figure 6. Typical Startup Waveforms

Current Limit and Latch-off Protection

The FAN5182 compares a programmable current limit set point to the voltage from the output of the current sense amplifier. The level of current limit is set with the resistor from the ILIMIT pin to ground. During normal operation, the voltage on ILIMIT is 3V. The current through the external resistor is internally scaled to give a current limit threshold of 10.4mV/µA. If the difference in voltage between CSREF and CSCOMP rises above the current limit threshold, the internal current limit amplifier controls the COMP voltage to maintain the power supply output current at the over current level.

After the limit is reached, the 3V pull-up voltage source on the DELAY pin is disconnected, and the external DELAY capacitor discharges through the external resistor. A comparator monitors the DELAY pin voltage and shuts off the controller when the voltage drops below 1.8V. The current limit latch-off delay time is therefore set by the RC time constant discharging the DELAY voltage from 3V to 1.8V. Typical over-current latch-off waveforms are shown in Figure 7.

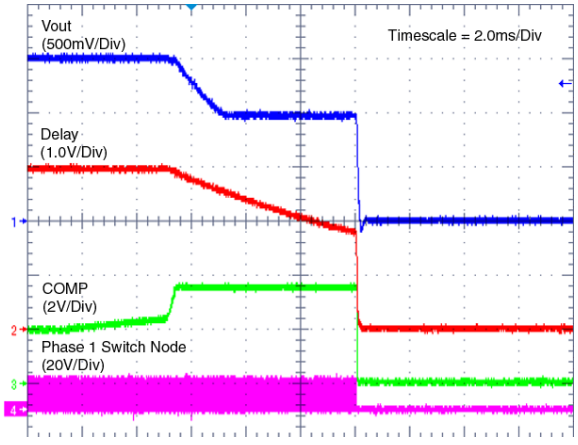


Figure 7. Over-current Latch-off Waveforms

The controller continues to switch all phases during the latch-off delay time. If the over-current condition is removed before the 1.8V DELAY threshold being reached, the controller will resume its normal operation. The over current recovery characteristic also depends on the state of PWRGD. If the output voltage is within the PWRGD window during over current, the controller resumes normal operation once over current condition being removed. However, if over current causes the output voltage to drop below the PWRGD threshold, a soft-start cycle will be initiated.

The latch-off function can be reset by either removing and reapplying V_{CC} to the FAN5182 or by pulling the EN pin low for short time. To disable the over current latch-off function, the external resistor connecting between the DELAY pin and ground should be removed, and a high value resistor (>1MΩ) should be connected from the DELAY pin to VCC. This prevents the DELAY capacitor from discharging, so the 1.8V threshold can never be reached. This pull-up resistor has some impact to the soft-start time, because the current through this pull-up resistor adds additional current to the internal 20µA soft-start current.

During start-up when the output voltage is below 200mV, a secondary current limit is activated. This is necessary because the voltage swing of CSCOMP cannot go below ground. This secondary current limit clamps the COMP voltage to 2V.

An inherent per phase current limit protects individual phase if one or more phases cease to function because of a faulty component. This limit is based on the maximum normal mode COMP voltage.

Power Good Monitoring

The power good comparator monitors the output voltage via the FB pin. The PWRGD pin is an open-drain output whose high level (when connected to a pull-up resistor) indicates that the output voltage is within the nominal limits specified in the electrical characteristic table. PWRGD goes low if the output voltage is outside of this specified range or whenever the EN pin is pulled low. Figure 8. shows the PWRGD response when the input power supply is switched off.

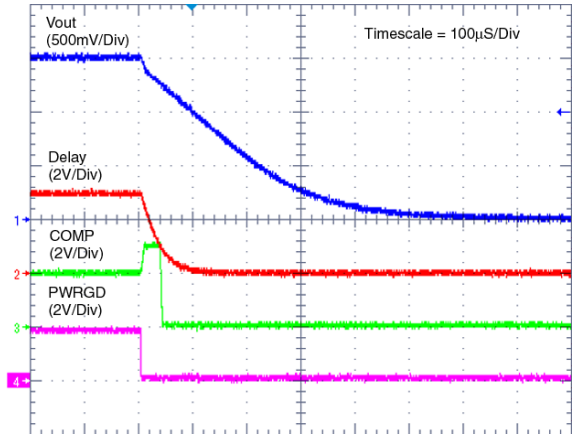


Figure 8. Shutdown Waveforms

As part of the protection for the load and output components of the supply, the PWM outputs are driven low (turning on the low-side MOSFETs) when the output voltage exceeds the crowbar trip point. This crowbar action stops once the output voltage falls below the reset threshold of approximately 650mV.

Turning on the low-side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output over voltage is due to a short in the high-side MOSFET, this crowbar action can trip the input supply over current protection or blow the input fuse, protecting the load from being damaged.

Enable and UVLO

For the FAN5182 to begin switching, the input supply (V_{CC}) to the controller must be higher than the UVLO threshold, and the EN pin must be higher than its logic threshold. If UVLO is less than the threshold or the EN pin is logic low, the FAN5182 is disabled. This holds the PWM outputs at ground, shorts the DELAY capacitor to ground, and holds the I_{LIMIT} pin at ground.

In the application circuit, the I_{LIMIT} pin should be connected to the OD pins of the FAN5009 drivers. Grounding the I_{LIMIT} pin will disable the drivers such that both HDRV and LDRV are holding low. This feature is important in preventing fast discharge of the output capacitors when the controller shuts off. If the driver outputs are not being disabled, a negative output voltage can be generated due to high current being discharged from the output capacitors through the inductors.

Application Information

Design parameters for a typical high current point-of-load dc/dc buck converter shown in Figure 5 are as follows:

- Input voltage (V_{IN}) = 12V
- Output voltage (V_{OUT}) = 1.8V
- Duty cycle (D) = 0.15
- Output current I_O = 55A
- Maximum output current (I_{LIM}) = 110A
- Number of phases (n) = 3
- Switching frequency per phase (f_{SW}) = 250kHz

Setting the Clock Frequency

The FAN5182 uses a fixed-frequency control architecture. The frequency is set by an external timing resistor (R_T). The clock frequency and the number of phases determine the switching frequency per phase, which relates directly to switching losses and the sizes of the inductors and the input and output capacitors. With n = 3 for three phases, a clock frequency of 750kHz sets the switching frequency (f_{SW}) of each phase to 250kHz, which represents a practical trade-off between the switching losses and the sizes of the output filter components.

Equation 1 shows that to achieve a 750kHz oscillator frequency, the correct value for R_T is 255kΩ. Alternatively, the value for R_T can be calculated using

$$R_T = \frac{1}{n \times f_{SW} \times 4.7\text{pF}} - 27\text{k}\Omega \quad (1)$$

$$R_T = \frac{1}{3 \times 250\text{kHz} \times 4.7\text{pF}} - 27\text{k}\Omega = 256\text{k}\Omega$$

where 4.7pF and 27kΩ are internal IC component values. For good initial accuracy and frequency stability, a 1% resistor is recommended. The closest standard 1% value for this design is 255kΩ.

Soft-Start and Current Limit Latch-off Delay Time

Because the soft start and current limit latch-off delay functions share the DELAY pin, these two parameters must be considered together. The first step is to set C_{DLY} for the soft-start ramp. This ramp is generated with a 20µA internal current source. The value of R_{DLY} has a second-order impact on the soft-start time because it sinks part of the current source to ground. However, as long as R_{DLY} is kept greater than 200kΩ, this effect is minor.

The value for C_{DLY} can be approximated using:

$$C_{DLY} = \left(20\mu\text{A} - \frac{V_{REF}}{2 \times R_{DLY}}\right) \times \frac{t_{SS}}{V_{REF}} \quad (2)$$

where t_{SS} is the desired soft-start time. Assuming an R_{DLY} of 390kΩ and a desired soft-start time of 3ms, C_{DLY} is 71nF. The closest standard value for C_{DLY} is 68nF. Once C_{DLY} is chosen, R_{DLY} can be calculated for the current limit latch-off time using:

$$R_{DLY} = \frac{1.96 \times t_{DELAY}}{C_{DLY}} \quad (3)$$

If the result for R_{DLY} is less than 200kΩ, a smaller soft-start time should be considered by recalculating the equation for C_{DLY}, or a longer latch-off time should be used. R_{DLY} should never be less than 200kΩ. In this example, a delay time of 9ms results in R_{DLY} = 259kΩ. The closest standard 1% value is 261kΩ.

Inductor Selection

The inductance determines the ripple current in the inductor. Small inductance leads to high ripple current, which increases the output ripple voltage and conduction losses in the MOSFETs, and vise versa. In any multiphase converters, it's recommended to design the peak-peak inductor ripple current to be less than 50% of the maximum inductor dc current.

Equation 4 shows the relationship among the inductance, oscillator frequency, and peak-peak ripple current.

$$I_R = \frac{V_{OUT} \times (1 - D)}{f_{SW} \times L} \quad (4)$$

Equation 5 can be used to determine the minimum inductance based on a given output ripple voltage.

$$L \geq \frac{V_{OUT} \times R_x \times (1 - (n \times D))}{f_{SW} \times V_{RIPPLE}} \quad (5)$$

where R_X is the ESR of output bulk capacitors.

Solving Equation 5 for a 20mV peak-to-peak output ripple voltage and 3mΩ R_X yields

$$L \geq \frac{1.8\text{V} \times 3\text{m}\Omega \times (1 - (3 \times 0.15))}{250\text{kHz} \times 20\text{mV}} = 594\text{nH}$$

If the resulting ripple voltage is too low, the inductance can be reduced until the desired ripple voltage is achieved. In this example, a 600nH inductor is a good starting point that produces a calculated ripple current of 6.6A. The inductor should not saturate at the peak current of 21.6A, and should be able to handle the total power dissipation created by the copper and core loss.

Another important factor in the inductor design is the DCR, which is used for measuring the phase current. A large DCR can cause excessive power losses, whereas too small DCR can increases measurement error. For this design, a DCR of 1.4mΩ was chosen.

Designing an Inductor

Once the inductance and DCR are known, the next step is to either design an inductor or find a suitable standard inductor if one exists. Inductor design starts with choosing appropriate core material. Some candidate materials that have low core loss at high frequencies are powder cores (e.g. Kool-Mµ® from Magnetics, Inc., or from Micrometals) and gapped soft ferrite cores (e.g. 3F3 or 3F4 from Philips). Powdered iron cores have higher core loss, and are used for low cost applications.

The best choice for a core geometry is a closed-loop type, such as a potentiometer core, a PQ/U/E core, or a toroid core.

Some useful references for magnetics design are

- Magnetic Designer Software
- Intusoft (www.intusoft.com)
- Designing Magnetic Components for High-Frequency DC-DC Converters, by William T. McLyman, Kg Magnetics, Inc., ISBN 1883107008

Selecting a Standard Inductor

The following power inductor manufacturers can provide design consultation and deliver power inductors optimized for high power applications upon request.

- Coilcraft

  (847) 639-6400

  www.coilcraft.com

- Coiltronics

  (561) 752-5000

  www.coiltronics.com

- Sumida Electric Company

  (510) 668-0660

  www.sumida.com

- Vishay Intertechnology

  (402) 563-6866

  www.vishay.com

Output Current Sense

The output current can be measured by summing the voltage across each inductor and passing the signal through a low-pass filter. The CS amplifier is configured with resistors $R_{PH(X)}$ (for summing the voltage), and R_{CS} and C_{CS} (for the low-pass filter). The output current I_O is set by the following equations:

$$I_O = \frac{R_{PH(x)}}{R_{CS}} \times \frac{V_{DRP}}{R_L} \quad (6)$$

$$C_{CS} \geq \frac{L}{R_L \times R_{CS}} \quad (7)$$

where:

R_L is the DCR of the output inductors.

V_{DRP} is the voltage drop from CSCOMP to CSREF.

When load current reaches its limit, V_{DRP} is at its maximum (V_{DRPMAX}). V_{DRPMAX} can be in the range of 100mV to 200mV. In this example, it is 110mV.

One has the flexibility of choosing either R_{CS} or $R_{PH(X)}$. It is recommended to select R_{CS} equal to 100kΩ, and then solve for $R_{PH(X)}$ by rearranging Equation 6.

$$R_{PH(x)} = R_L \times R_{CS} \times \frac{I_{LIM}}{V_{DRPMAX}}$$

$$R_{PH(x)} = 1.4\text{m}\Omega \times 100\text{k}\Omega \times \frac{110\text{A}}{110\text{mV}} = 140\text{k}\Omega$$

Next, use Equation 7 to solve for C_{CS}.

$$C_{CS} \geq \frac{600\text{nH}}{1.4\text{m}\Omega \times 100\text{k}\Omega} \geq 4.29\text{nF}$$

Choose the closest standard value that is greater than the result given by Equation 7. This example uses a C_{CS} value of 5.6nF.

Output Voltage

FAN5182 has an internal FBRTN referred 800mV voltage reference (V_{REF}). The output voltage can be set by using a voltage divider consists of resistors R_{B1} and R_{B2}:

$$V_{OUT} = \frac{(R_{B1} + R_{B2})}{R_{B1}} \times V_{REF} \quad (8)$$

Rearranging Equation 8 to solve R_{B2} and assuming a 1%, 1kΩ resistor for R_{B1} yields

$$R_{B2} = \frac{V_{OUT} - V_{\text{REF}}}{V_{\text{REF}}} \times R_{B1}$$

$$R_{B2} = \frac{1.8\text{V} - 0.8\text{V}}{0.8\text{V}} \times 1\text{k}\Omega = 1.25\text{k}\Omega$$

The closest standard 1% resistor value for R_{B2} is 1.24kΩ.

Power MOSFETs

For this example, one high-side and one low-side N-channel power MOSFETs per phase have been selected. The main selection parameters for power MOSFETs are $V_{GS(TH)}$, Q_G, C_{ISS}, C_{RSS}, and $R_{DS(ON)}$. The minimum gate drive voltage (the supply voltage to the FAN5009) dictates whether standard threshold or logic-level threshold MOSFETs can be used. With V_{GATE} ~10V, logic-level threshold MOSFETs ($V_{GS(TH)}$ < 2.5V) are recommended.

The maximum output current (I_O) determines the $R_{DS(ON)}$ requirement for the low-side (synchronous) MOSFETs. With good current balance among phases, the current in each low-side MOSFET is the output current divided by the total number of low-side MOSFETs (n_{SF}). Since conduction loss is dominant in low-side MOSFET, the following expression can represent total power dissipation in each synchronous MOSFET in terms of the ripple current per phase (I_R) and the total output current (I_O):

$$P_{SF} = (1 - D) \times \left[\left(\frac{I_O}{n_{SF}} \right)^2 + \frac{1}{12} \times \left(\frac{n \times I_R}{n_{SF}} \right)^2 \right] \times R_{DS(SF)} \quad (9)$$

Knowing the maximum output current and the maximum allowed power dissipation, one can determine the required $R_{DS(ON)}$ for the MOSFET. For example, D-PAK MOSFETs operating up to ambient temperature of 50°C, a safe limit for P_{SF} is around 1W to 1.5W at 120°C junction temperature. Therefore, in this example, $R_{DS(SF)}$ (per MOSFET) < 7.5mΩ. This $R_{DS(SF)}$ is typically measured at junction temperature of about 120°C In this example, we select a lower-side MOSFET with 4.8mΩ at 120°C.

Another important consideration for choosing the synchronous MOSFET is the input capacitance and feedback capacitance. The ratio of feedback to input capacitance must be small (less than 10% is recommended) in order to preventing accidentally turning on the synchronous MOSFETs when the switch node goes high.

Also, the time to switch the synchronous MOSFETs off should not exceed the non-overlap dead time of the MOSFET driver (40ns typical for the FAN5009). The output impedance of the driver is approximately 2Ω, and the typical MOSFET input gate resistances are about 1Ω to 2Ω. Therefore, the total gate capacitance should be less than 6000pF. In the event there are two MOSFETs in parallel, the input capacitance for each synchronous MOSFET should be limited to 3000pF.

The high-side (main) MOSFET power dissipation consists of two elements: conduction and switching losses. The switching loss is related to the main MOSFET's turn on and off time, and the current and voltage being switched. Based on the main

MOSFET's switching speed (rise and fall time that the gate driver can offer) and MOSFET input capacitance, the following expression provides approximate switching loss for each main MOSFET:

$$P_{S(MF)} = 2 \times f_{SW} \times \frac{V_{CC} \times I_O}{n_{MF}} \times R_G \times \frac{n_{MF}}{n} \times C_{ISS} \quad (10)$$

where:

n_{MF} is the total number of main MOSFETs.

R_G is the total gate resistance (2Ω for the FAN5009 and about 1Ω for typical logic level n-channel MOSFETs, total R_G = 3Ω).

C_{ISS} is the input capacitance of the main MOSFET.

Note that adding more main MOSFETs (n_{MF}) does not help to lower the switching loss for each main MOSFET, it can only reduces conduction loss. The most efficient way to reduce switching loss is to use low gate charge / capacitance devices.

The conduction loss of the main MOSFET is given by the following equation:

$$P_{C(MF)} = D \times \left[\left(\frac{I_O}{n_{MF}} \right)^2 + \frac{1}{12} \times \left(\frac{n \times I_R}{n_{MF}} \right)^2 \right] \times R_{DS(MF)} \quad (11)$$

where $R_{DS(MF)}$ is the on resistance of the main MOSFET.

Typically, for main MOSFETs, a low gate charge (C_{ISS}) device is preferred, but low gate charge MOSFETs usually have higher on resistance. Select a device that meets total power dissipation around 1.5W for a single D-PAK MOSFET.

In this example, a FDD6296 is selected as the main MOSFET (three total; n_{MF} = 3), with a C_{ISS} = 1440pF, and $R_{DS(MF)}$ = 9mΩ (at T_J = 120°C), and a FDD8896 is selected as the synchronous MOSFET (three total; n_{SF} = 3), with C_{ISS} = 2525pF and $R_{DS(SF)}$ = 5.4mΩ (at T_J = 120°C). The synchronous MOSFET C_{ISS} is less than 6000pF. Solving for the power dissipation per MOSFET at I_O = 55A and I_R = 6.6A yields 1.56W for each synchronous MOSFET and 1.29W for each main MOSFET. These numbers comply with the power dissipation limit of around 1.5W per MOSFET.

One more item that needs to be considered is the power dissipation in the driver for each phase. The gate drive loss is described in terms of the Q_G for the MOSFETs, and is given by the following equation

$$P_{DRV} = \left[\frac{f_{SW}}{n} \times (n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GSF}) + I_{CC} \right] \times V_{CC} \quad (12)$$

where:

Q_{GMF} is the total gate charge for each main MOSFET.

Q_{GSF} is the total gate charge for each synchronous MOSFET.

$I_{CC} \times V_{CC}$ in equation (12) represents the driver's standby power dissipation. For the FAN5009, the maximum dissipation should be less than 400mW. In this example, with I_{CC} = 5mA, Q_{GMF} = 25nC, and Q_{GSF} = 50nC, there is 285mW in each driver, which is below the 400mW dissipation limit. See the "Thermal Information" table in the FAN5009 datasheet for more details.

Ramp Resistor Selection

The ramp resistor (R_R) is used for setting the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of phase current balance, stability, and transient response. The following expression is used to determine the optimum value:

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS(ON)(SF)} \times C_R} \quad (13)$$

$$R_R = \frac{0.2 \times 600\text{nH}}{3 \times 5 \times 4.8\text{m}\Omega \times 5\text{pF}} = 333\text{k}\Omega$$

where:

A_R is the internal ramp amplifier gain.

A_D is the current balancing amplifier gain.

$R_{DS(ON)(SF)}$ is the equivalent low-side MOSFET on resistance.

C_R is the internal ramp capacitor value.

The closest standard 1% resistor value is 332kΩ.. The internal ramp voltage magnitude can be calculated by using

$$V_R = \frac{(V_{IN} - V_{REF}) \times A_R \times D}{(R_R + 2K\Omega) \times C_R \times f_{SW}} \quad (14)$$

$$V_R = \frac{(12 - 0.8) \times 0.2 \times 0.15}{(332\text{k}\Omega + 2\text{k}\Omega) \times 5\text{pF} \times 250\text{kHz}} = 805\text{mV}$$

The size of the internal ramp can be made larger or smaller. If it is made larger, stability and transient response improve, but thermal balance degrades. Likewise, if the ramp is made smaller, thermal balance improves but transient response and stability degrade. The factor of three in the denominator of Equation 13 sets a ramp size with optimal balance for good stability, transient response, and thermal balance.

Current Limit Setpoint

The current limit threshold of the FAN5182 is set with a 3V source (V_{LIM}) across R_{LIM} with a gain of 10.4 mV/µA (A_{LIM}). R_{LIM} can be found using

$$R_{LIM} = \frac{A_{LIM} \times V_{LIM}}{V_{DRPMAX}} \quad (15)$$

If R_{LIM} is greater than 500kΩ, the actual current limit threshold may be lower than the intended value. Hence some adjustment for R_{LIM} may be neeeed. Here, I_{LIM} is the average current limit for the output of the supply. In this example, using the V_{DRPMAX} value of 110mV from Equations 6 and 7 and choosing a peak current limit of 110A for I_{LIM} results in R_{LIM} = 284kΩ, for which 287kΩ is chosen as the nearest 1% value.

The per phase current limit described earlier is determined by

$$I_{PHLIM} \cong \frac{V_{COMP(MAX)} - V_R - V_{BIAS}}{A_D \times R_{DS(MAX)}} + \frac{I_R}{2} \quad (16)$$

Close Loop Compensation Design

Optimum compensation of the FAN5182 assures the best possible load regulation and transient response of the regulator. The target of the compensation design is to achieve reasonably high control bandwidth with sufficient phase and gain margin.

The power stage of the synchronous buck converter consists of two poles and one zero. A two-pole, one-zero compensator of the voltage error amplifier is adequate for proper compensation, if the output bulk capacitors are electrolytic types (low ESR zero). Equations 17 to 19 are able to yield an approximate starting point for the design. To further optimize the design, some bench adjustments may be necessary

$$C_A = \frac{C_X \times R_X}{4 \times R_{B2}} \times \left(\frac{n \times R_X}{\left(\frac{V_R}{V_{OUT}} \times R_L \right) + (A_D \times R_{DS})} \right) \quad (17)$$

$$R_A = \frac{4 \times R_{B2}}{n \times C_x \times R_x} \times \left(\frac{L \times V_R}{R_x \times V_{OUT}} - \frac{A_D \times R_{DS}}{2 \times f_{SW} \times R_x} \right) \quad (18)$$

$$C_{FB} = \frac{1}{2 \times n \times f_{SW} \times R_A} \quad (19)$$

If C_X is 6000µF (five 1200µF capacitors in parallel) with an equivalent ESR of 3mΩ, the equations above give the following compensation values:

C_A = 1.33nF

R_A = 6.05kΩ

C_{FB} = 110pF

Selecting the nearest standard value for each of these component yields C_A = 1.2nF, R_A = 6.04kΩ, and C_{FB} = 100pF.

As mentioned above, this compensation design scheme is typically good for applications using electrolytic type capacitors, where the capacitor ESR zero can roughly cancel one of the power stage poles. However, for all ceramic capacitor types of applications, since the capacitor ESR zero can be very high, a three-pole, two-zero compensator has to be used.

A complete Mathcad control design program is available from Fairchild upon request.

Input Capacitor Selection and Input Current di/dt Reduction

In continuous inductor current mode, the source current of the high-side MOSFET is approximately a square wave with a duty ratio equal to $n \times V_{OUT}/V_{IN}$ and an amplitude of one-nth the maximum output current. To prevent large voltage variation, a low ESR input capacitor, sized for the maximum rms current, must be used. The maximum rms capacitor current is given by

$$I_{CRMS} = D \times I_O \times \sqrt{\frac{1}{n \times D} - 1} \quad (20)$$

$$I_{CRMS} = 0.15 \times 55\text{A} \times \sqrt{\frac{1}{3 \times 0.15} - 1} = 9.1\text{A}$$

Note that manufacturers often specify capacitor ripple current rating based on only 2,000 hours of life. Therefore, it is advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may be placed in parallel to meet size or height requirements in the design. In this example, the input capacitor bank is formed by two 2,700µF, 16V aluminum electrolytic capacitors and three 4.7µF ceramic capacitors.

To reduce the input current di/dt to a level below the system requirement, in this example 0.1A/µs, an additional small inductor (L > 370nH @ 10A) can be inserted between the converter and the supply bus. This inductor serves as a filter between the converter and the primary power source.

Inductor DCR Temperature Correction

With the inductor's DCR being used as the sense element, one needs to compensate for temperature changes in the inductor's winding if a highly accurate current limit setpoint is desired. Fortunately, copper has a well-known temperature coefficient (TC) of 0.39%/°C.

If R_{CS} is designed to have an opposite and equal percentage of change in resistance to that of the inductor wire, it cancels the temperature variation of the inductor's DCR. Due to the nonlinear nature of NTC thermistors, resistors R_{CS1} and R_{CS2} are needed. See Figure 9. for instructions on how to linearize the NTC and produce the desired temperature coefficient.

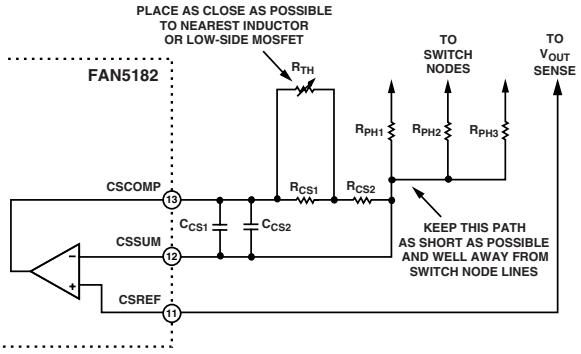


Figure 9. Temperature Compensation Circuit Values

Follow the procedures and expressions shown below for calculation of R_{CS1}, R_{CS2}, and R_{TH} (the thermistor value at 25°C) based on a given R_{CS} value.

1. Select an NTC according to type and value. Because we do not have a value yet, start with a thermistor with a value close to R_{CS}. The NTC should also have an initial tolerance of better than 5%.
2. Based on the NTC type, find its relative resistance value at two temperatures. The temperatures that work well are 50°C and 90°C. These resistance values are called A ($R_{TH(50°C)}/R_{TH(25°C)}$) and B ($R_{TH(90°C)}/R_{TH(25°C)}$). Note that the NTC's relative value is always 1 at 25°C.
3. Find the relative value of R_{CS} required for each of these temperatures. This is based on the percentage of change needed, which in this example is initially 0.39%/°C. These are called r1 (1/(1 + TC × (T_1 - 25))) and r2 (1/(1 + TC × (T_2 - 25))), where TC = 0.0039 for copper. T_1 = 50°C and T_2 = 90°C are chosen. From this, one can calculate that r1 = 0.9112 and r2 = 0.7978.

4. Compute the relative values for R_{CS1}, R_{CS2}, and R_{TH} using

$$r_{CS2} = \frac{(A-B)\times r_1 \times r_2 - A\times(1-B)\times r_2 + B\times(1-A)\times r_1}{A\times(1-B)\times r_1 - B\times(1-A)\times r_2 - (A-B)} \quad (21)$$

$$r_{CS1} = \frac{(1-A)}{\left(\frac{1}{1-r_{CS2}}\right) - \left(\frac{A}{r_1 - r_{CS2}}\right)} \quad (22)$$

$$r_{TH} = \frac{1}{\left(\frac{1}{1-r_{CS2}}\right) - \left(\frac{1}{r_{CS1}}\right)} \quad (23)$$

5. Calculate $R_{TH} = r_{TH} \infty R_{CS}$, then select the closest value of thermistor available. Also, compute a scaling factor *k* based on the ratio of the actual thermistor value used relative to the computed one:

$$k = \frac{R_{TH(ACTUAL))}}{R_{TH(CALCULATED)}} \quad (24)$$

6. Calculate values for R_{CS1} and R_{CS2} using

$$R_{CS1} = R_{CS}\times k \times r_{CS1} \quad (25)$$

$$R_{CS2} = R_{CS}\times((1-k) + (k\times r_{CS2})) \quad (26)$$

PCB Layout Guidelines

General Recommendations

To achieve the best possible performance, a PCB with at least four layers is recommended. When doing the layout, please keep in mind that each square unit of 1 ounce copper has resistance of ~0.53mΩ at room temperature.

Whenever high currents must be routed to a different PCB layers, vias should be used properly to create several parallel current paths so that the resistance and inductance introduced by these current paths are minimized, and the via current-rating is not exceeded.

If critical signal traces must be routed close to power circuitry, a signal ground plane must be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.

An analog ground island should be used around and under the FAN5182 as a reference for the components associated with the controller. This analog ground should be connected to the power ground at a single point.

The components around the FAN5182 should be close to the controller with short traces. The output capacitors should be placed as close as possible to the load. If the load is distributed, the capacitors should also be distributed in proportion to the respective load.

Power Circuitry Recommendations

The PCB layout starts with high frequency power component placement. Try to minimize stray inductance of the MOSFET half bridge which is composed of the input capacitors, and top and bottom MOSFETs. A good practice is to use short and wide traces or copper pours to minimize the inductance in the MOSFET half bridge. Failure to do so can lead to severe phase node ringing. A snubber circuit is always recommended to partly kill the phase node switching noise.

Whenever using a power dissipating component, for example, a power MOSFET that is soldered to the PCB, the proper use of vias, both directly on the mounting pad and immediately surrounding the mounting pad is recommended. Make a mirror image of the power pad being used on the component side to heatsink the MOSFETs on the opposite side of the PCB. Use large copper pour for high current traces to lower the electrical impedance and help dissipate heat. Do not make the switching node copper pour unnecessarily large, since it could radiate noise.

An undisturbed solid power ground plane should be used as one of the inner layers.

Signal Circuitry Recommendations

The output voltage is sensed from the FB and the FBRTN pins. To avoid differential mode noise pickup in these differential sensed traces, the loop area between the FB and FBRTN traces should be minimized. In other words, the FB and FBRTN traces should be routed adjacent to each other with minimum spacing on top of the analog / power ground plane back to the controller.

The signal traces connecting to the switch nodes should be tied as close as possible to the inductor pins. The CSREF sense trace should be connected to the second nearest inductor pin to the controller.

Detailed step-by-step PCB layout instructions are available from Fairchild upon request.

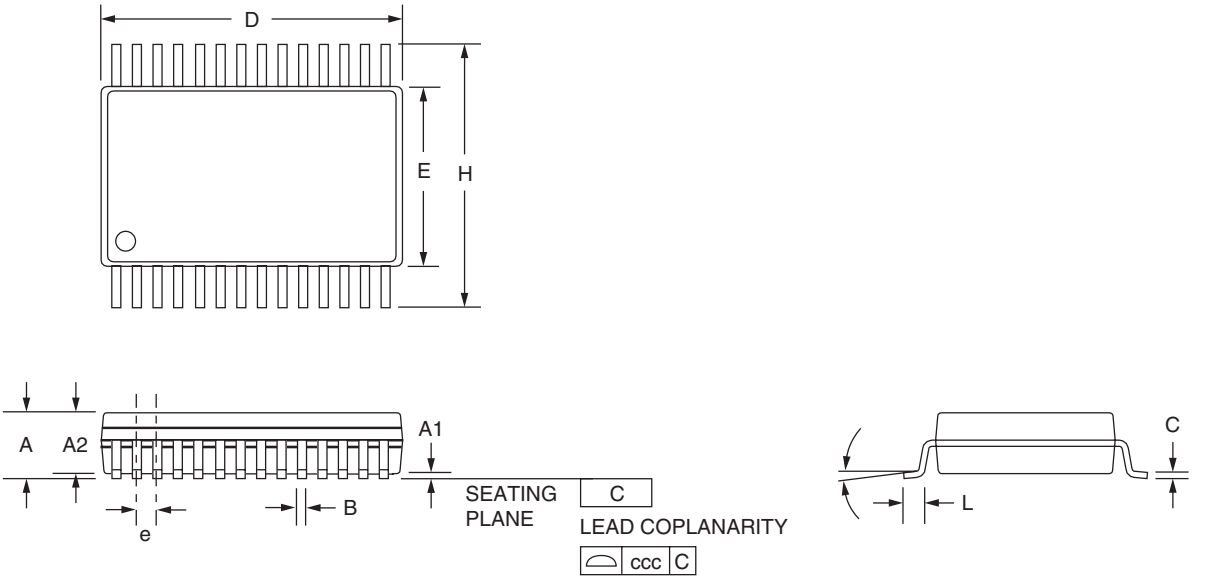
Mechanical Diagram

20 Pin - QSOP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	0.053	0.069	1.35	1.75	
A1	0.004	0.010	0.10	0.25	
A2	-	0.061	-	1.54	
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	
D	0.386	0.394	9.81	10.00	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		
H	0.228	0.244	5.80	6.19	
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	20		20		7
	0	8	0	8	

Notes:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamber on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the maximum number of terminals.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.



Ordering Information

Part Number	Temperature Range	Package Type	Packing Method	Quantity per Reel
FAN5182QSCX_NL	0°C to +85°C	QSOP-20L	Tape and Reel	2500

Note: FAN5182QSCX_NL is a Pb-free part.

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CROSSVOLT™	GlobalOptoisolator™	MicroFET™	PowerTrench®	SuperSOT™-6
DOME™	GTO™	MicroPak™	QFET®	SuperSOT™-8
EcoSPARK™	HiSeC™	MICROWIRE™	QS™	SyncFET™
E²CMOS™	I²C™	MSX™	QT Optoelectronics™	TinyLogic®
EnSigna™	*i-Lo*™	MSXPro™	Quiet Series™	TINYOPTO™
FACT™	ImpliedDisconnect™	OCX™	RapidConfigure™	TruTranslation™
FACT Quiet Series™		OCXPro™	RapidConnect™	UHC™
Across the board. Around the world.™		OPTOLOGIC®	µSerDes™	UltraFET®
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Programmable Active Droop™		PACMAN™	SMART START™	VCX™

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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