MMN 2716:2048 x 8 BIT EPROM

MMN 2616:2048 x 8 BIT PROM

GENERAL DESCRIPTION

The MMN 2716 is a static, electrically programmable read-only memory (16k EPROM) which has a transparent lid to allow erasure of the bit pattern with ultraviolet light.
The device is fabricated with N-channel silicon gate technology. It is packaged in a 24-pin dual-in-line ceramic package.
The MMN 2616 is a factory-programmed read-only memory (16k PROM), also manufactured with N-channel silicon gate technology. The device is packaged in a 24-pin dual-in-line plastic pckage. Pin assignment; A.C. and D.C. characteristics of both the MMN 2616 and MMN 2716 circuits are identical. The two devices feature a 16,384-bit storage capacity organized as 2048 x 8 bits.

FEATURES

MMN2716

- The device is a 2048 x 8 bit UV erasable PROM
- Single 5 volts supply in READ mode
- Access Time in Read Cycle:
  MMN 2716-1 tACC1 = 350 ns
  MMN 2716-2 tACC1 = 390 ns
  MMN 2716 tACC1 = 450 ns
- STANDBY mode of operation reduces the active device power by 75% approx.
- Tri-state outputs, bidirectional data pins
- Programming with 50-ms TTL level pulses
- Programming by bytes (8 bits) of data is possible

MMN 2616

- The device is a 2048x8 bit factory-programmable PROM
- VCC = 5 V power supply
- Access Time in Read Cycle:
  MMN 2616-1 tACC1 = 350 ns
  MMN 2616-2 tACC1 = 390 ns
  MMN 2616 tACC1 = 450 ns
- STANDBY mode of operation reduces the active device power by 75% approx.
- Tri-state outputs

ABSOLUTE MAXIMUM RATINGS

(Voltages relative to Vss = 0V)

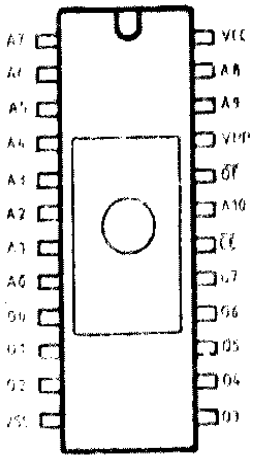
PARAMETER	SYMBOL	Min.	Max.	UNITS
Voltage on any pin except VPP	VT	−0,5	6,5	V
VPP Supply Voltage	VPP	−0,5	26,0	V
Power Dissipation	PT		1	W
Ambient Temperature	TA	0	70	°C
Storage Temperature	TS	−55	125	C

PIN NAMES

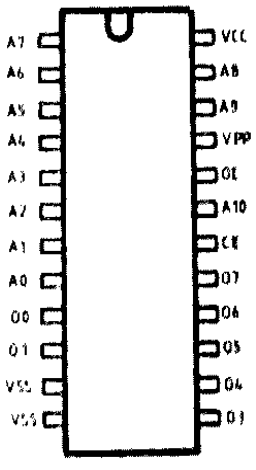
A0 A10	ADDRESSES
O0 O7	OUTPUTS INPUTS
OE	OUTPUT ENABLE
CE	CHIP ENABLE
VCC	POWER SUPPLY
VPP	PROGRAMMING POWER SUPPLY
VSS	GROUND

CONNECTION DIAGRAM

MMN 2716



MMN 2616



STATIC ELECTRICAL CHARACTERISTICS

(Voltages relative to Vss = 0V)

PARAMETER	SYMBOL	TEST CONDITION	Min.	Typ.	Max.	UNITS
Supply Voltage	VCC		4,75	5	5,25	V
VPP Supply Voltage with respect to Ground during Read	VPP		VCC −0,6	VCC	VCC +0,6	V
Input Low Voltage	VIL		−0,3		0,8	V
Input High Voltage	VIH		2,0		VCC +1	V
Input Leakage Current	ILI	VI=5,25 V			10	µA
Output Leakage Current	ILO	VO=5,25 V OE=VIH			10	µA
Output Law Voltage	VOL	IOL = 2,1 mA			0,4	V
Output High Voltage	VOH	IOH=−0,4 mA	2,4			V
Operating Temperature	TA		0	25	70	°C

PARAMETER	SYMBOL	TEST CONDITION	MMN2616 MMN2716 Min.	MMN2616 MMN2716 Max.	MMN2716-1 MMN2616-1 Min.	MMN2716-1 MMN2616-1 Max.	MMN2716-2 MMN2616-2 Min.	MMN2716-2 MMN2616-2 Max.	UNITS
VCC Standby Power Supply Current	ICC1	OE=VIL CE=VIH		25		30		25	mA
VCC Active Power Supply Current	ICC2	OE=VIL CE=VIL		100		120		100	mA
VPP Supply Current (in READ mode)	IPP1	VPP=5,25		5		6		5	mA
VPP Supply Current during Programming Pulse (MMN2716)	IPP2	VPP=25		30		40		30	mA

NOTES : 1. VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP
2. VPP may be connected directly to VCC except during programming. The supply current would then be the sum of ICC and IPP1.
3. The tolerance of 0,6 V allows the use of a driver circuit for switching the VPP supply pin from VCC in read to 25 V for programming.

DYNAMIC ELECTRICAL CHARACTERISTICS

(TA = 0C ~ 70C, VCC = 5V ±5%, VPP = VCC ±0,6 V)

PARAMETER	SYMBOL	TEST CONDITION	MMN2616 MMN2716 Min.	MMN2616 MMN2716 Max.	MMN2716-1 MMN2616-1 Min.	MMN2716-1 MMN2616-1 Max.	MMN2716-2 MMN2616-2 Min.	MMN2716-2 MMN2616-2 Max.	UNITS
Addresses to Output Delay	tACC1	$\overline{CE}$=$\overline{OE}$=VIL		450		350		390	ns
$\overline{CE}$ to Output Delay	tACC2	$\overline{OE}$=VIL		450		350		390	ns
$\overline{OE}$ to Output Delay	tCO	$\overline{CE}$=VIL		120		120		120	ns
$\overline{OE}$ High to Output Hi-Z	tDF	$\overline{CE}$=VIL		100		100		100	ns
$\overline{CE}$ High to Output Hi-Z	tPF			100		100		100	ns

CAPACITANCES

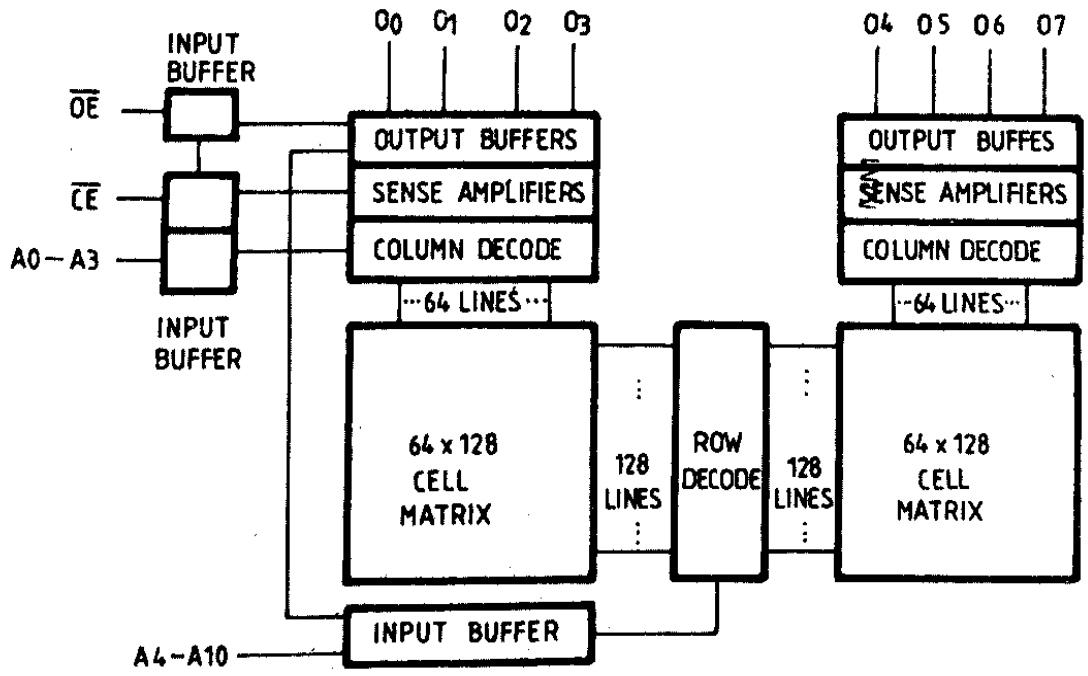
PARAMETER	SYMBOL	TEST	Min.	Max.	UNITS
Input capacitance (A0-A10, CE, OE)	CIN	f = 1 MHz V = 0 V TA = 25°C		6	pF
Output capacitance	COUT			12	pF

PROGRAM OPERATION

PARAMETER	SYMBOL	Min.	Typ.	Max.	UNITS
VPP Supply Voltage	VPP	24	25	26	V
Operating Temperature	TA	20	25	30	C
Address Setup Time	tAS	2			µs
$\overline{OE}$ Setup Time	tCSS	2			µs
Data Setup Time	tDS	2			µs
Address Hold Time	tAH	2			µs
$\overline{OE}$ Hold Time	tCSH	2			µs
Data Hold Time	tDH	2			µs
$\overline{OE}$ = VIH to Output Hi-Z Delay ($\overline{CE}$ = VIL)	tDF	0		120	ns
$\overline{OE}$ = VIL to Output Delay ($\overline{CE}$ = VIL)	tCO			120	ns
Program Pulse Width	tPW	45	50	55	ms
Program Pulse Rise Time	tPRT	10			ns
Program Pulse Fall Time	tPFT	10			ns

NOTES : 1. VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP. The 2716 must not be inserted into or removed from a board with VPP at 25±1 V to prevent damage to the device.
2. The maximum allowable voltage which may be applied to the VPP pin during programming is +26 V. Care must be taken when switching the VPP supply to prevent overshoot exceeding this 26 V maximum specification.

BLOCK DIAGRAM



DEVICE OPERATION

The modes of operation of the MMN2716 and MMN2616 are listed in Table 1 and Table 2.
The power supplies required are VCC and VPP. The VPP power supply must be at 25 V during the three programming modes and must be at 25 V in the three modes.
All input signals are fully TTL compatible during both read and program modes. The data outputs are three state to facilitate memory expansion by OR tving

Table 1 MMN2716 MODE SELECTION

Mode	VCC (24)	VPP (21)	CE (18)	OE (20)	OUTPUTS 9; 11; 13—17
Read	+5	+5	VIL	VIL	Data Output
Outputs Deselected	+5	+5	VIL	VIH	High impedance state
Standby Mode	+5	+5	VIH	VIL/VIH	High impedance state
Programming	+5	+25	VIH	VIH	Data Input
Program Verify	+5	+25	VIL	VIL	Data Output
Program Inhibit	+5	+25	VIL	VIH	High impedance state

Table 2 MMN2616 MODE SELECTION

Mode	VCC (24)	VPP (21)	CE (18)	OE (20)	OUTPUTS 9; 11; 13—17
Read	+5	+5	VIL	VIL	Data Output
Outputs Deselected	+5	+5	VIL	VIH	High impedance state
Stabdby Mode	+5	+5	VIH	VIL/ViH	High impedance state

Read Mode

The 2716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs.
CHIP ENABLE ($\overline{CE}$) is the power control and should be used for device selection. OUTPUT ENABLE ($\overline{OE}$) is the output control and should be used to gate data to the output pin, independent of device selection. Assuming that addresses are stable, address access time (tACC1) is equal to the delay from $\overline{CE}$ to output (TACC2). Data is available at the outputs 120 ns (tCO) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC1 — tCO.

Standby mode

The 2716 has a standby mode which reduces the active power dissipation by 75%, from 525 mW to 132 mW. The 2716 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Programming

The EPROM MMN 2716 is in the programming mode when the VPP power supply is at 25V and $\overline{OE}$ is at VIH. The data to be programmed is applied 8 bits in parallel to the data pins. These should be treated as a tri-state bus; during program operation, the outputs become the data inputs. When the adresses and data are stable, a 50 ms, active high, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time, either individually, sequentially or at random.
Initially, and after each erasure, all bits of MMN 2716 are in the „1" state. Data is introduced by selectively programming „0's" into the desired bit locations. Although only „0's" will be programmed, both „1's" and „0's" can be presented in the data word

Program inhibit

Programming of multiple MMN 2716 in parallel with different data is also easily accomplished. A TTL level program pulse applied to a MMN 2716's CE input, with VPP at 25V will program that MMN 2716. A low level $\overline{CE}$ input inhibits the other MMN 2716 from being programmed.

Program verify

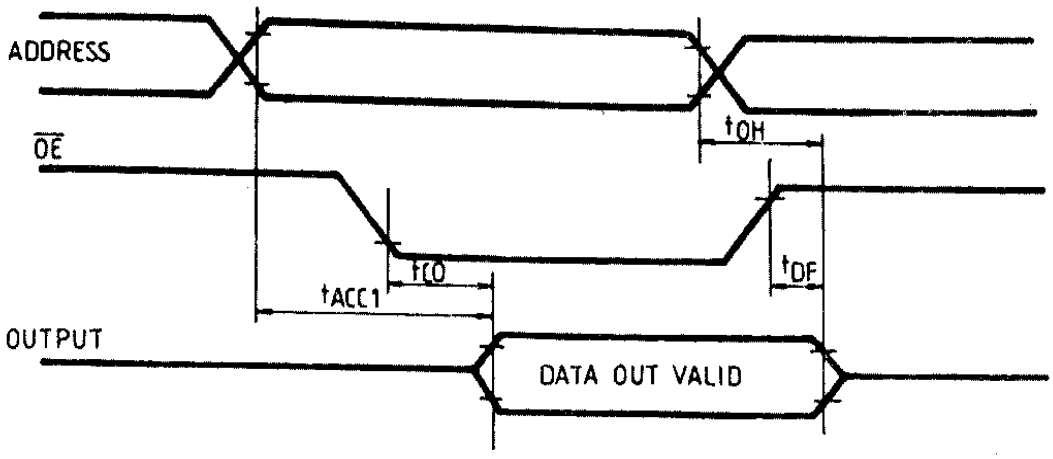
A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with VPP at 25V. Note that the device should be placed within a distance equal to or less than one inch from the top edge of its package to the lamp tube. Depending on the type of lamp used the time required for an effective erasure is three times the latent erasure time. The latent erasure time is the time after the elapse of wich the memory contents are just no longer detectable. The erasure time should not be less than ten minutes.
Contamination of the transparent lid will deteriorate the transparency and hence affect the erasure time. At least 20 programming/erasure cycles are possible. The erasure time will increase with a greater number of programming/erasure cycles.

ERASURE CHARACTERISTICS

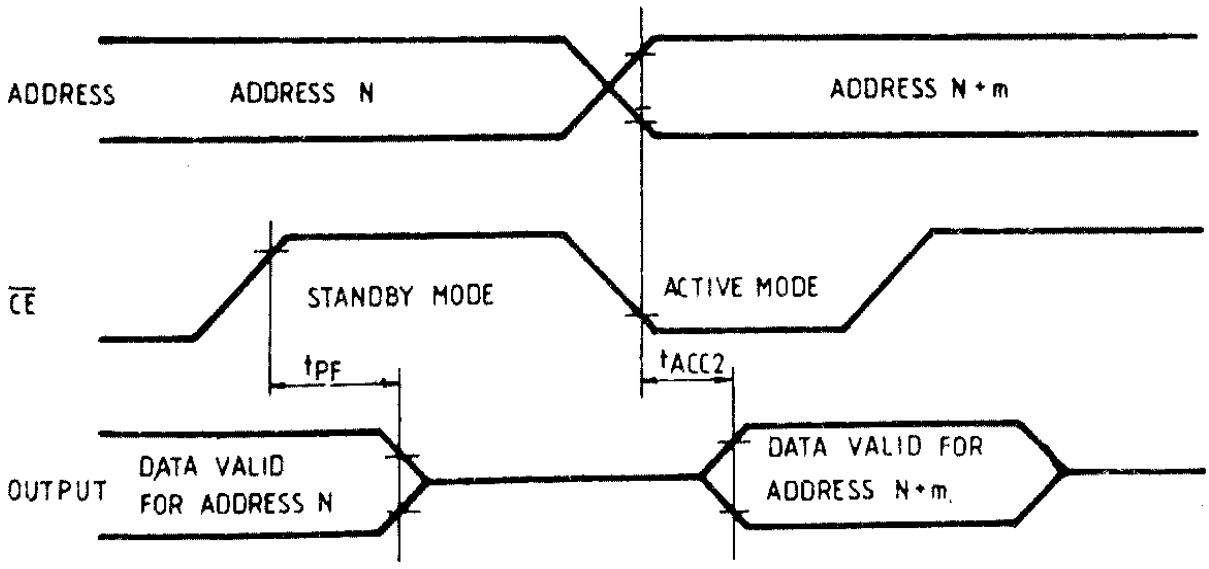
The only way to change a „0" to a „1" is by ultraviolet light erasure. The window provided in the package allow the programmed bit pattern to be erased through exposure to ultraviolet light.
The recommended erasure procedure for the MMN 2716 is exposure to shortware ultraviolet light wich has a ware length of 2537 Angstroms (A). The integrated dose (UE UV intensity * exposure time), for erasure should be

A_{min} = 15 watt seconds/cm — for quartz lids
A_{min} = 30 watt seconds/cm — for ceramic lids

READ WAVEFORMS



POWER DOWN READ WANEFORMS



PROGRAMMING WAVEFORMS