

INTERNATIONAL RECTIFIER

AVALANCHE ENERGY AND dv/dt RATED

HEXFET® TRANSISTORS

IRFG110

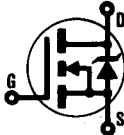
2N7334

JANTX2N7334

JANTXV2N7334

[REF: MIL-S-19500/597]

**4 N-CHANNEL
POWER MOSFETs**



14 LEAD DUAL-IN-LINE QUAD
(CERAMIC SIDE BRAZED PACKAGE)

100 Volt, 0.70 Ohm

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dv/dt capability.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for both military and commercial applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

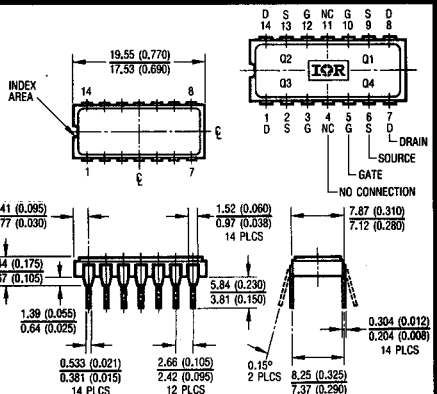
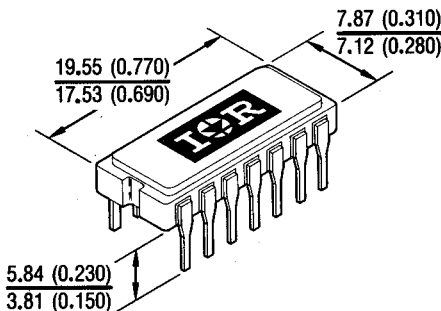
Product Summary

Part Number	VDS	RDS(on)	ID
IRFG110	100V	0.70Ω	1.0A

Features:

- Avalanche Energy Rating
- Dynamic dv/dt Rating
- Hermetically Sealed
- For Automatic Insertion
- Lightweight
- Simple Drive Requirements
- Ease of Paralleling
- 4 N-Channel Co-Packaged HEXFETs

CASE STYLE AND DIMENSIONS



Conforms to JEDEC MO-036AB
Dimensions in Millimeters and (Inches)

Absolute Maximum Ratings For Each Chip

Parameter		Units
I_D @ $V_{GS} = 10V$, $T_C = 25^\circ C$	Continuous Drain Current	1.0
I_D @ $V_{GS} = 10V$, $T_C = 100^\circ C$	Continuous Drain Current	0.6
I_{DM}	Pulsed Drain Current $\text{\textcircled{1}}$	4.0
P_D @ $T_C = 25^\circ C$	Max. Power Dissipation	1.4
	Linear Derating Factor	0.011
V_{GS}	Gate-to-Source Voltage	± 20
E_{AS}	Single Pulse Avalanche Energy $\text{\textcircled{2}}$	75 (See Fig. 12)
dv/dt	Peak Diode Recovery $\text{\textcircled{3}}$	5.5 (See Fig. 13)
T_J	Operating Junction	-55 to 150
T_{STG}	Storage Temperature Range	
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)
	Weight	1.3 (typical)
		A
		W
		WK $\text{\textcircled{4}}$
		V
		mJ
		V/ns
		$^\circ C$
		g


Electrical Characteristics For Each Chip @ $T_J = 25^\circ C$ (Unless Otherwise Specified)

Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	100	—	—	V	$V_{GS} = 0V$, $I_D = 1.0$ mA
$\Delta BV_{DSS}/\Delta T_J$	—	0.13	—	V/ $^\circ C$	Reference to $25^\circ C$, $I_D = 1.0$ mA
$R_{DS(on)}$	—	—	0.70	Ω	$V_{GS} = 10V$, $I_D = 0.6A$ $V_{GS} = 10V$, $I_D = 1.0A$ $\text{\textcircled{4}}$
$V_{GS(th)}$	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250$ μA
g_{fs}	0.86	—	—	S (ft)	$V_{DS} \geq 15V$, $I_{PS} = 0.6A$ $\text{\textcircled{4}}$
I_{DSS}	—	—	25	μA	$V_{DS} = 0.8 \times$ Max. Rating, $V_{GS} = 0V$
	—	—	250		$V_{DS} = 0.8 \times$ Max. Rating $V_{GS} = 0V$, $T_J = 125^\circ C$
I_{GSS}	—	—	100	nA	$V_{GS} = 20V$
I'_{GSS}	—	—	-100		$V_{GS} = -20V$
Q_g	—	—	15	nC	$V_{GS} = 10V$, $I_D = 1.0A$
Q_{gs}	—	—	7.5		$V_{DS} = 0.5 \times$ Max. Rating
Q_{gd}	—	—	7.5		See Fig. 6 and 14
$t_{d(on)}$	—	—	20	ns	$V_{DD} = 50V$, $I_D = 1.0A$, $R_G = 24\Omega$ See Fig. 11
t_r	—	—	25		
$t_{d(off)}$	—	—	40		
t_f	—	—	40		
L_D	—	4.0	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die. Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
L_S	—	6.0	—		
C_{iss}	—	180	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$ $f = 1.0$ MHz See Fig. 5
C_{oss}	—	82	—		
C_{rss}	—	15	—		





Source-Drain Diode Ratings and Characteristics for Each Chip

Parameter		Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) @ $T_C = 25^\circ\text{C}$	—	—	1.0	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier. 
	I_{SM}	—	—	4.0		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 1.0\text{A}, V_{GS} = 0\text{V}$ ⓐ
t_{rr}	Reverse Recovery Time	—	—	200	ns	$T_J = 25^\circ\text{C}, I_F = 1.0\text{A}, di/dt \leq 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovery Charge	—	—	0.83	μC	$V_{DD} \leq 50\text{V}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

ⓐ Repetitive Rating: Pulse width limited by maximum junction temperature (see figure 9) Refer to current HEXFET reliability report

ⓑ $I_{SD} \leq 1.0\text{A}, di/dt \leq 75\text{A}/\mu\text{s}$
 $V_{DD} \leq 50\text{V}, T_J \leq 150^\circ\text{C}$
 Suggested $R_G = 240$

ⓒ $K/W = ^\circ\text{C}/\text{W}$
 $W/K = \text{W}/^\circ\text{C}$

ⓓ $V_{DD} = 25\text{V}$. Starting $T_J = 25^\circ\text{C}$
 $L \geq 112\text{mH}$. $R_G = 250$,
 Peak $I_L = 1.0\text{A}$

ⓔ Pulse width $\leq 300\mu\text{s}$; Duty Cycle $\leq 2\%$

Power Ratings

Test	Single FET	All Four FETs With Equal Power	Units
P_D @ $T_A = 25^\circ\text{C}$ Maximum Power Dissipation	1.4	2.5	W
L_{DF} Linear Derating Factor	0.011	0.020	W/K
R_{thJC} Thermal Resistance Junction-to-Case	17	—	K/W
R_{thJA} Thermal Resistance Junction-to-Ambient	90	50	K/W
K_{14}, K_{13} Thermal Coupling Factors	45	40	%

To a first order approximation the temperature rise of each device within the package is the result of the power dissipated by the device itself and the power dissipated by the other adjacent devices. The power dissipated by the adjacent devices does not have the same effect as the power dissipated within the junction itself. The temperature rise for any particular unit (eg. (1)) within the package can be calculated with the following expression:

$$(1) \Delta T_1 = 90 (P_1 + K_{14} P_4 + K_{13} P_3)$$

where the K_{ij} are the thermal coupling coefficients shown in the Power Ratings table.

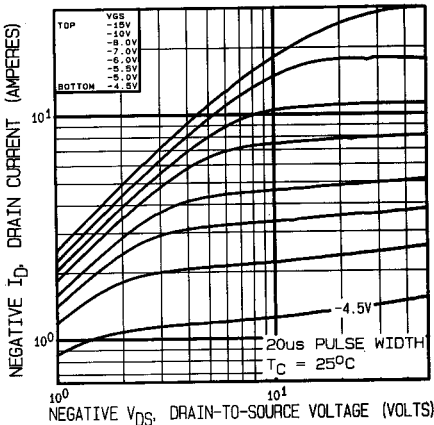
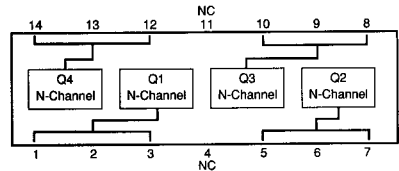


Fig. 1—Typical Output Characteristics, $T_C = 25^\circ\text{C}$

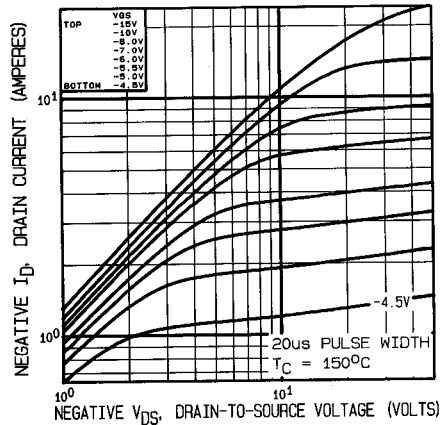


Fig. 2—Typical Output Characteristics, $T_C = 150^\circ\text{C}$

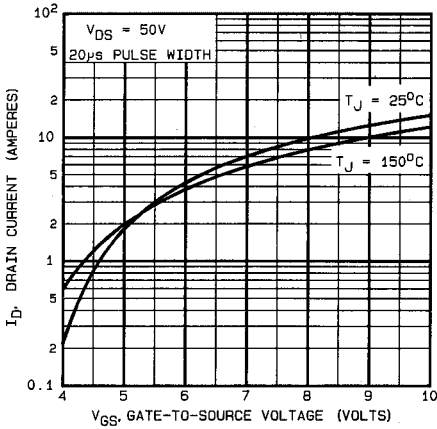


Fig. 3—Typical Transfer Characteristics

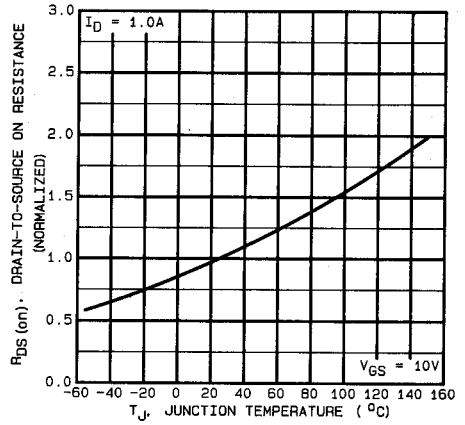


Fig. 4—Normalized On-Resistance Vs. Temperature

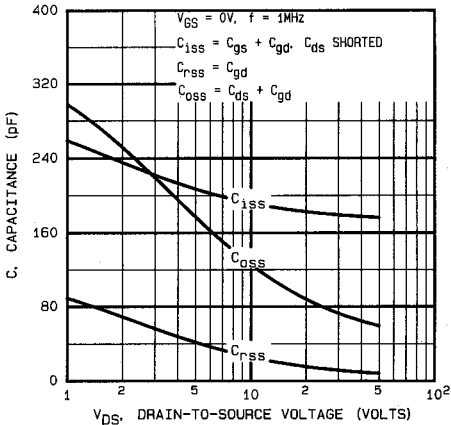


Fig. 5—Typical Capacitance Vs. Drain-to-Source Voltage

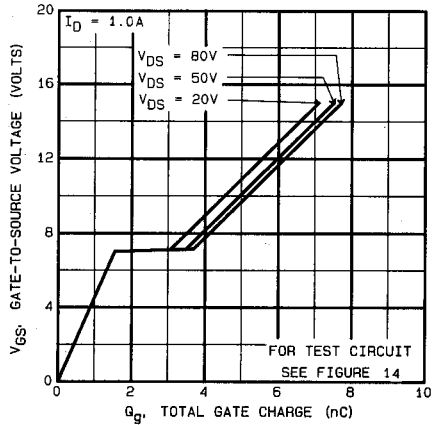


Fig. 6—Typical Gate Charge Vs. Gate-to-Source Voltage

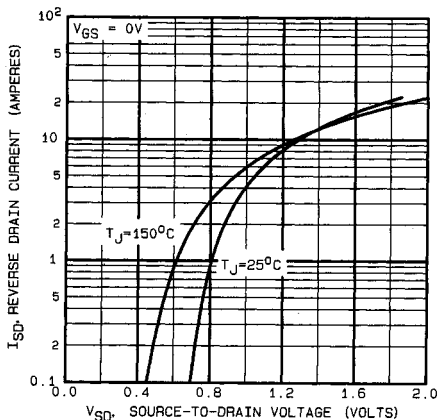


Fig. 7—Typical Source-Drain Diode Forward Voltage

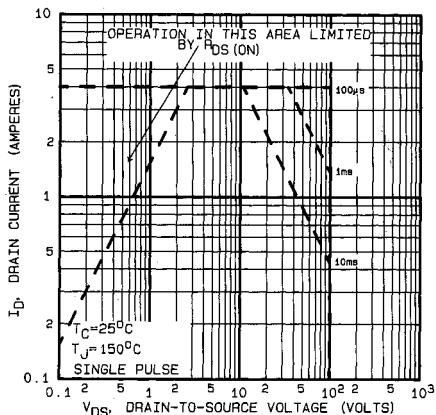


Fig. 8—Maximum Safe Operating Area

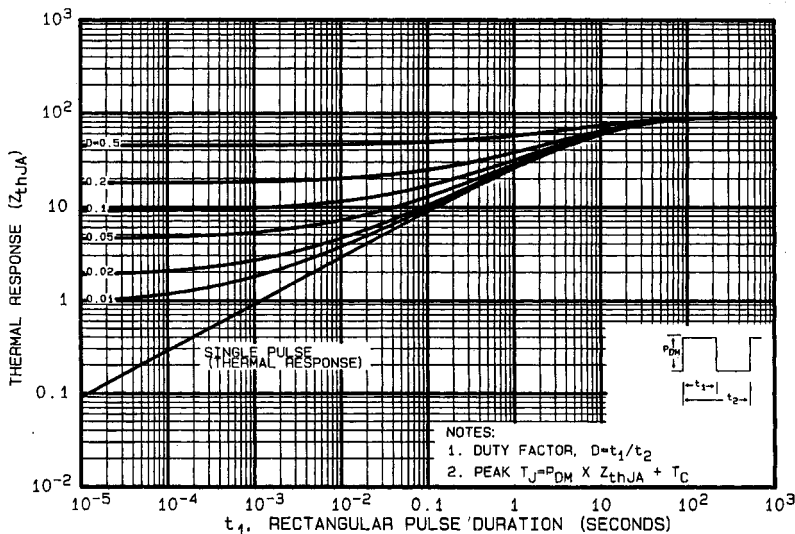


Fig. 9—Maximum Effective Transient Thermal Impedance, Junction-to-Ambient Vs. Pulse Duration

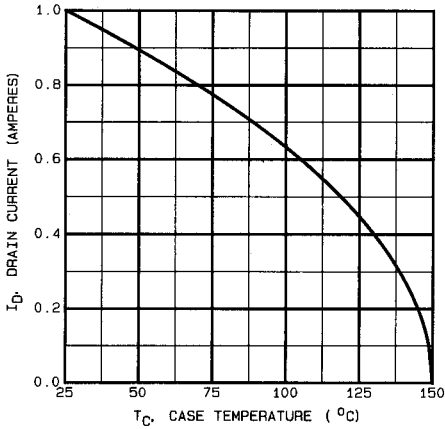


Fig. 10—Maximum Drain Current Vs. Case Temperature

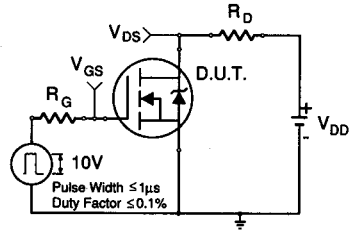


Fig. 11a — Switching Time Test Circuit

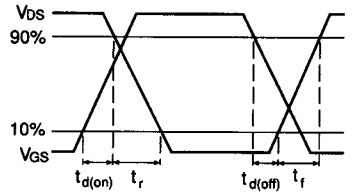


Fig. 11b — Switching Time Waveforms

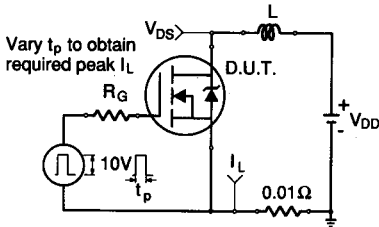


Fig. 12a—Unclamped Inductive Test Circuit

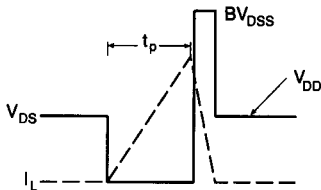


Fig. 12b—Unclamped Inductive Waveforms

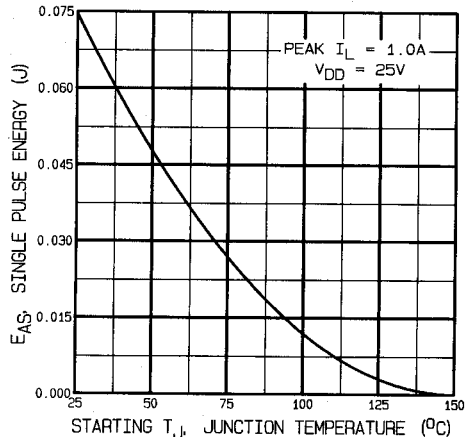


Fig. 12c—Maximum Avalanche Energy Vs. Starting Junction Temperature

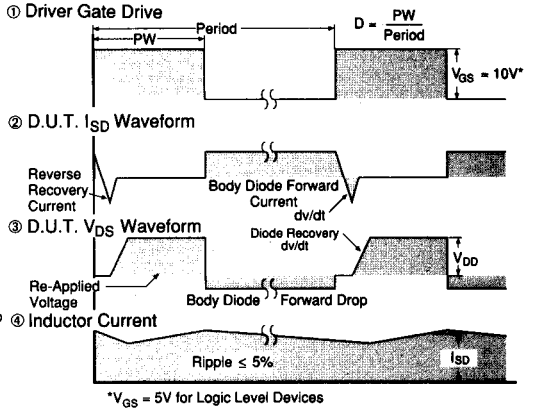
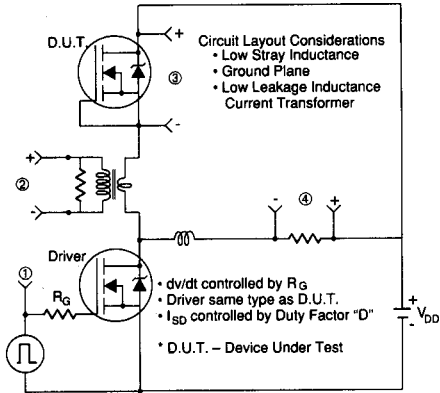


Fig. 13—Peak Diode Recovery dv/dt Test Circuit

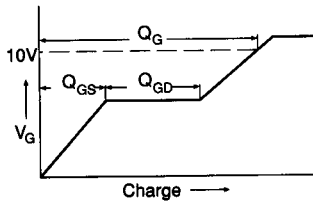


Fig. 14a—Basic Gate Charge Waveform

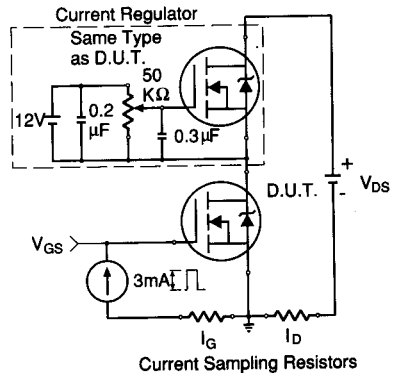


Fig. 14b—Gate Charge Test Circuit