IMI145152

INTERNATIONAL MICROCIRCUITS INC

CMOS LSI
PARALLEL INPUT PLL FREQUENCY SYNTHESIZER

T-50-17

PRODUCT FEATURES

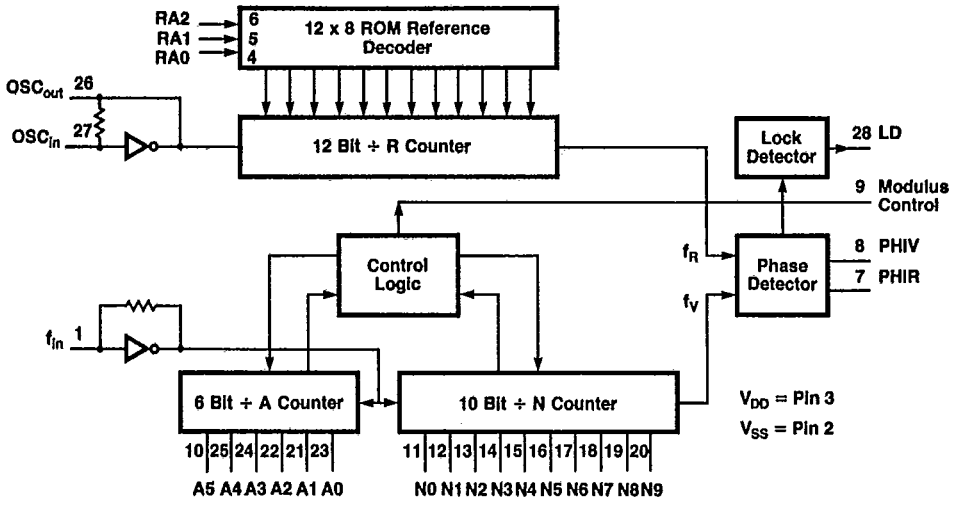
- >40 MHz Typical Input Capability @ V_{DD} = 5V
- On- or Off-Chip Reference Oscillator Operation with Buffered Output
- Lock Detect Signal
- Dual Modulus/Parallel Programming
- 8 User-Selectable ÷R Values: 8, 64, 128, 256, 512, 1024, 1160, 2048
- ÷N Range = 3 to 1023; ÷A Range = 0 to 63
- Packaging Options Include: Plastic and Ceramic Dual-In-Line, Plastic J-Leaded, Ceramic Leadless Chip Carriers, and Small-Outline Packages. Die available for Hybrid Applications.
- Grades Available Include: Commercial, Military Operating Range, and Military Screened

PRODUCT DESCRIPTION

The IMI145152 is one of a family of LSI PLL frequency synthesizers from International Microcircuits. In the 28-pin ceramic or plastic dual-in-line packages, this product is pin-for-pin compatible with the MC145152, and can be used as a direct replacement with identical or superior operating characteristics. This product can be alternatively packaged to meet your needs. MIL-STD-883 screening is available for high-reliability applications.

The IMI145152 CMOS PLL frequency synthesizer is programmed by 16 parallel inputs. The device features consist of a reference oscillator, selectable-reference divider, two output phase detector, 10-bit programmable ÷N counter and 6-bit programmable ÷A counter. When combined with a loop filter and VCO, the IMI145152 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a dual modulus prescaler can be used between the VCO and IMI145152.

BLOCK DIAGRAM



NOTE: N0 through N9, A0 through A5 and RA0 through RA2 have pullup resistors not shown.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +10	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} +0.5	Vdc
Operating Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

(Voltage Referenced to V_{SS})

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	−55°C Min	−55°C Max	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	125°C Min	125°C Max	Units
Power Supply Voltage	V_{DD}	—	3	8	3	8	3	—	8	3	8	3	8	Vdc
Output Voltage V_{in} = V_{DD} or 0	V_{OL}	3	—	0.05	—	0.05	—	0	0.05	—	0.05	—	0.05	Vdc
		5	—	0.05	—	0.05	—	0	0.05	—	0.05	—	0.05	
		8	—	0.05	—	0.05	—	0	0.05	—	0.05	—	0.05	
V_{in} = 0 or V_{DD}	V_{OH}	3	2.95	—	2.95	—	2.95	3	—	2.95	—	2.95	—	
		5	4.95	—	4.95	—	4.95	5	—	4.95	—	4.95	—	
		8	7.95	—	7.95	—	7.95	8	—	7.95	—	7.95	—	
Input Voltage V_O = 2.5 or 0.5	V_{IL}	3	—	0.9	—	0.9	—	1.35	0.9	—	0.9	—	0.9	Vdc
V_O = 4.5 or 0.5		5	—	1.5	—	1.5	—	2.75	1.5	—	1.5	—	1.5	
V_O = 7.5 or 1.5		8	—	2.4	—	2.4	—	3.65	2.4	—	2.4	—	2.4	
V_O = 0.5 or 2.5	V_{IH}	3	2.1	—	2.1	—	2.1	1.65	—	2.1	—	2.1	—	
V_O = 0.5 or 4.5		5	3.5	—	3.5	—	3.5	2.75	—	3.5	—	3.5	—	
V_O = 1.5 or 7.5		8	5.6	—	5.6	—	5.6	4.45	—	5.6	—	5.6	—	
Output Current V_{OH} = 2.7	I_{OH}	3	−1.6	—	−1.6	—	−1.4	−2.0	—	−0.8	—	−0.8	—	mAdc
V_{OH} = 4.6		5	−2.4	—	−2.4	—	−2.0	−2.8	—	−1.6	—	−1.6	—	
V_{OH} = 7.5		8	−4.8	—	−1.6	—	−3.6	−4.6	—	−2.8	—	−2.8	—	
V_{OH} = 2.7 OSC_{out}	I_{OH}	3	−0.8	—	−0.8	—	−0.7	−1.0	—	−0.4	—	−0.4	—	
V_{OH} = 4.6 only		5	−1.2	—	−1.2	—	−1.0	−1.4	—	−0.8	—	−0.8	—	
V_{OH} = 7.5		8	−2.4	—	−0.8	—	−1.8	−2.3	—	−1.4	—	−1.4	—	
V_{OL} = 0.3	I_{OL}	3	1.6	—	1.6	—	1.4	2.0	—	0.8	—	0.8	—	
V_{OL} = 0.4		5	2.4	—	2.4	—	2.0	2.8	—	1.6	—	1.6	—	
V_{OL} = 0.5		8	4.8	—	1.6	—	3.6	4.6	—	2.8	—	2,8	—	
V_{OL} = 0.3 OSC_{out}	I_{OL}	3	0.8	—	0.8	—	0.7	1.0	—	0.4	—	0.4	—	
V_{OL} = 0.4 only		5	1.2	—	1.2	—	1.0	1.4	—	0.8	—	0.8	—	
V_{OL} = 0.5		8	2.4	—	0.8	—	1.8	2.3	—	1.4	—	1.4	—	
Input Current f_{in}, OSC_{in}	I_{in}	8	—	±50	—	±50	—	±10	±25	—	±22	—	±22	μAdc
Other Inputs	I_{IH}	8	—	±0.3	—	±0.3	—	±.00001	±0.1	—	±1.0	—	±1.0	
(With Pullup)	I_{IL}	8	—	−400	—	−400	—	−90	−200	—	−170	—	−170	
Input Capacitance	C_{in}	3–8	—	10	—	10	—	6	10	—	10	—	10	pF
Output Capacitance	C_{out}	3–8	—	10	—	10	—	6	10	—	10	—	10	pF
Quiescent Current (Static)	I_{DD}	8	—	150	—	150	—	40	150	—	150	—	150	μAdc

SWITCHING CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Units
Output Rise and Fall Time OSC_{out}	t_{TLH} t_{THL}	3	—	30	40	ns
		5	—	20	30	
		8	—	10	20	
Others		3	—	15	20	
		5	—	10	15	
		8	—	5	10	
Propagation Delay Time f_{in} to Modulus Control	t_{PLH} t_{PHL}	3	—	90	135	ns
		5	—	55	80	
		8	—	35	50	
Output Pulse Width PHIR, PHIV with f_R in Phase with f_V	t_{WO}	3	10	40	90	ns
		5	5	25	55	
		8	1	15	35	
Input Rise and Fall Times OSC_{in}, f_{in}	t_{TLH} t_{THL}	3	—	10	5	ms
		5	—	5	2	
		8	—	2	0.5	

(T_A = −55°C to +125°C, C_L = 50 pF)

FREQUENCY CHARACTERISTICS

Characteristic	Symbol	V_{DD}	−55°C to 125°C Max	Typical	−40°C to 85°C Max	Units
Operating Frequency f_{in} OSC_{in} Input = SQ Wave V_{DD}–V_{SS} or Sinewave 500mVP-P	f_{max}	3	15	35	17	MHz
		5	20	40	23	
		8	25	45	28	

PIN DESCRIPTIONS

f_{in} (Pin 1) – Input to the positive edge triggered ÷ N and ÷ A counters. f_{in} is typically derived from a dual modulus prescaler and is AC coupled into pin 1. For larger amplitude signals (standard CMOS logic levels) DC coupling may be used.

V_{SS} (Pin 2) – Circuit Ground.

V_{DD} (Pin 3) – Positive power supply.

RA0, RA1, RA2 (Pins 4, 5, and 6) – These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below. Pullup resistors ensure that inputs left open remain at a logic one and require only a SPST switch to alter data to the zero state.

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	512
1	0	1	1024
1	1	0	1160
1	1	1	2048

ΦR, ΦV (Pin 7 and 8) – These phase detector outputs can be combined externally for a loop error signal.

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ΦV pulsing low, ΦR remains essentially high.

If the frequency of f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ΦR pulsing low, ΦV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ΦV and ΦR remain high except for a small minimum time period when both pulse low in phase.

MODULUS CONTROL (Pin 9) – Signal generated by the on-chip control logic circuitry for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the ÷ A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N-A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T)=N*P+A where P and P+1 represent the dual modulus control levels; N represents the number programmed into the ÷ N counter; and A represents the number programmed into the ÷ A counter.

N INPUTS (Pin 11 through 20) – The N inputs provide the data that is preset into the ÷ N counter when it reaches the count of zero. N0 is the least significant digit and N9 is the most significant. Pullup resistors ensure that inputs left open remain at a logic one and require only a SPST switch to alter data to the zero state.

A INPUTS (Pin 23, 21, 22, 24, 25, 10) – The A inputs define the number of clock cycles of f_{in} that require a logic zero on the modulus control output. See the explanation of dual modulus prescaling. The A inputs all have internal pullup resistors that ensure that inputs left open will remain at a logic one.

OSC_{out}, OSC_{in} (Pin 26 and 27) – These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

LD (Pin 28) – Lock detector signal. High level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

DUAL MODULUS PRESCALING

The technique of dual modulus prescaling is well established as a method of achieving high-performance frequency synthesizer operation at high frequencies. The approach allows relatively low-frequency programmable counters to be used as high-frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that would otherwise result if a fixed (single modulus) divider was used for the prescaler.

In dual modulus prescaling, the lower-speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P+1 in the prescaler for the required amount of time (see modulus control definition). The IMI145152 contains this feature, and can be used with a variety of dual modulus prescalers to allow speed, complexity, and cost to be tailored to the system requirements. Prescaler with P, P+1 divide values in the range of ÷3/÷4 to ÷64/÷65 can be controlled by the IMI145152.

DESIGN GUIDELINES APPLICABLE TO THE IMI145152

The system total divide value (N_{total}) will be dictated by the application:

$$N_{total} = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N*P+A$$

N is the number programmed into the ÷ N counter; A is the number programmed into ÷ A counter. P and P+1 are two selectable divide ratios available in the two modulus prescalers. To have a range of N_{total} values in sequence, the ÷ A counter is programmed from zero through P−1 for a particular value N in the ÷ N counter. N is then incremented to N+1, and the ÷ A is sequenced from zero through P−1 again.

There are minimum and maximum values that can be achieved for N_{total}. These are a function of P and the size of the ÷ N and ÷ A counters. The constraint $N \geq A$ always applies. If $A_{max} = P-1$, then $N_{min} \geq P-1$; then $N_{total-min} = (P-1)P+A$ or $(P-1)P$, since A is free to assume the value of zero.

$$N_{total-min} = N_{max}*P+A_{max}$$

To maximize system frequency capability, the dual modulus prescaler's output must go from low to high after each group of P or P+1 input cycles. The prescaler should divide by P when its modulus control line is high, and by P+1 when its modulus control is low.

For the maximum frequency into the prescaler (F_{VCO} max), the value used for P must be large enough so that:

A. F_{VCO} max divided by P may not exceed the frequency capability of Pin 1 of the IMI145152.

B. The period of F_{VCO} divided by P must be greater than the sum of the times:

   a. Propagation delay through the dual modulus prescaler.

   b. Prescaler setup or release time relative to its modulus control signal.

   c. Propagation time from f_{in} to the modulus control output for the IMI145152.

A sometimes useful simplification in the IMI145152 programming code can be achieved by choosing the values for P of 8, 16, 32, 64. For these cases, the desired value to N_{total} will result when N_{total} in binary is used as the program code to the ÷ N and ÷ A counters in the following manner:

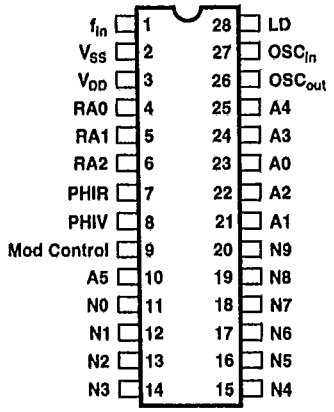
A. Assume the ÷ A counter contains "b" bits where $2^b=P$.

B. Always program all higher order ÷ A counter bits above "b" to zero.

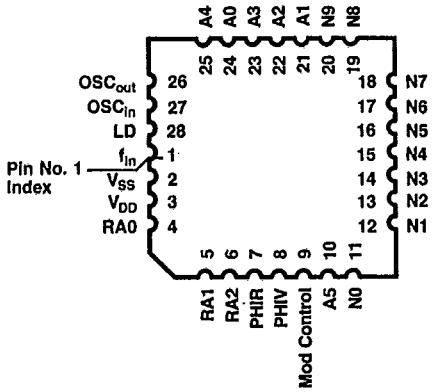
C. Assume the ÷ N counter and ÷ A counter (with all the higher order bits above "b" ignored) combined into a single binary counter of 10+b bits in length. The MSB of this "hypothetical" counter is to correspond to the LSB of ÷ A. The system divide value, N_{total}, now results when the value of N_{total} in binary is used to program the "new" 10+b bit counter.

CONNECTION DIAGRAMS

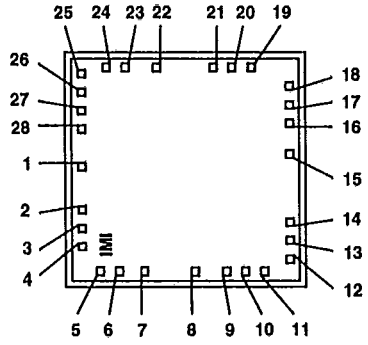
DUAL-IN-LINE PACKAGES



CHIP CARRIER



DIE LAYOUT



NOTE: Pin numbers correspond to DIP pin-out.

ORDERING INFORMATION

VALID COMBINATIONS:

IMI145152028**PB**
IMI145152028**QB**
IMI145152028**XB**
IMI145152028**ST**
IMI145152028**SK**
IMI145152028**LT**
IMI145152028**LK**
IMI145152000**DG**
IMI145152000**DQ**

For detailed ordering information see page 2.