

# 8 x 8-bit Parallel Multiplier

# LMU08/LMU8U

## FEATURES

- 35 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- LMU08 Replaces TRW MPY008H
- LMU8U Replaces TRW MPY08HU
- Two's Complement (LMU08), or Unsigned Operands (LMU8U)
- Three-State Outputs
- Available Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 40-pin Plastic DIP
  - 40-pin Sidebrazed, Hermetic DIP
  - 44-pin Plastic LCC, J-Lead (LMU08 only)
  - 44-pin Ceramic LCC (Type C)

## DESCRIPTION

The LMU08 and LMU8U are 8-bit parallel multipliers which feature high speed with low power consumption. They are pin-for-pin equivalents with TRW MPY08H and MPY08HU type multipliers. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

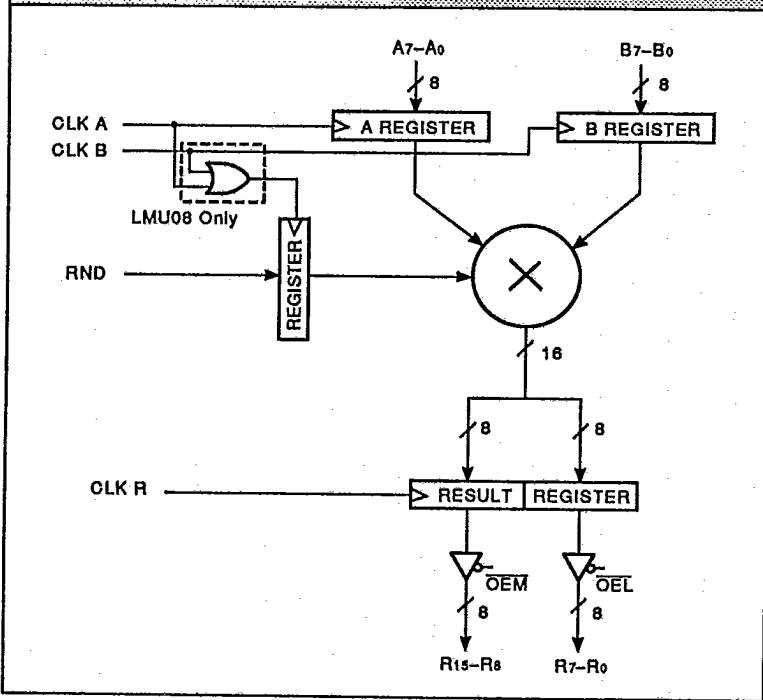
Both the LMU08 and the LMU8U produce the 16-bit product of two 8-bit numbers. The LMU08 accepts operands in two's complement format, and produces a two's complement result. The product is provided in two halves with the sign bit replicated as the most significant bit of

both halves. This facilitates use of the LMU08 product as a double precision operand in 8-bit systems. The LMU8U operates on unsigned data, producing an unsigned magnitude result.

Both the LMU08 and the LMU8U feature independently controlled registers for both inputs and the product, which along with three-state outputs allows easy interfacing with microprocessor busses. Provision is made in the LMU08 and LMU8U for proper rounding of the product to 8-bit precision. The round input is loaded at the rising edge of the logical OR of CLK A and CLK B for the LMU08. The LMU8U latches RND on the rising edge of CLK A only. In either case, a '1' is added in the most significant position of the lower product byte when RND is asserted. Subsequent truncation of the least significant product byte results in a correctly rounded 8-bit result.

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### LMU08/LMU8U BLOCK DIAGRAM

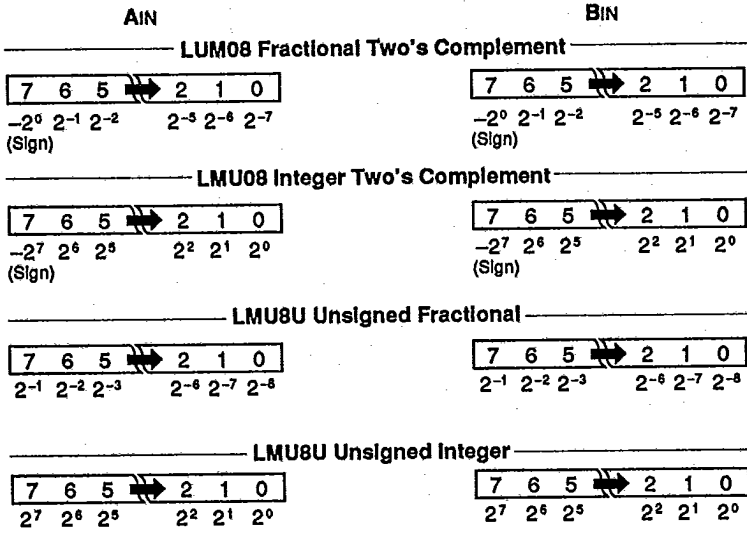


8 x 8-bit Parallel Multiplier

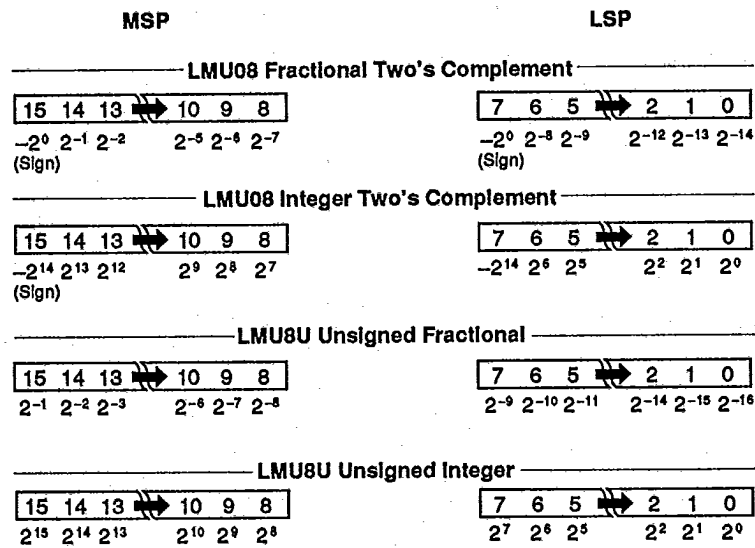
LMU08/8U

T-45-07

INPUT FORMATS



OUTPUT FORMATS



**MAXIMUM RATINGS** Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature .....	-65°C to +150°C
Operating ambient temperature .....	-55°C to +125°C
Vcc supply voltage with respect to ground .....	-0.5 V to +7.0 V
Input signal with respect to ground .....	-3.0 V to +7.0 V
Signal applied to high Impedance output .....	-3.0 V to +7.0 V
Output current into low outputs .....	25 mA
Latchup current .....	> 400 mA

**OPERATING CONDITIONS** To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ Vcc ≤ 5.25 V
Active Operation, Military	-55°C to +125°C	4.50 V ≤ Vcc ≤ 5.50 V

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**ELECTRICAL CHARACTERISTICS** Over Operating Conditions

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	IOH = -2.0 mA	3.5			V
VOL	Output Low Voltage	IOL = 8.0 mA			0.5	V
VIH	Input High Voltage		2.0		Vcc	V
VIL	Input Low Voltage	(Note 3)	0.0		0.8	V
IIX	Input Current	Ground ≤ VIN ≤ Vcc			±20	µA
I0Z	Output Leakage Current	Ground ≤ VOUT ≤ Vcc			±20	µA
I0S	Output Short Current	VOUT = Ground, VCC = Max (Notes 4, 8)			-250	mA
ICC1	Vcc Current, Dynamic	(Notes 5, 6)		8	24	mA
ICC2	Vcc Current, Quiescent	(Note 7)			1.0	mA

**SWITCHING CHARACTERISTICS**

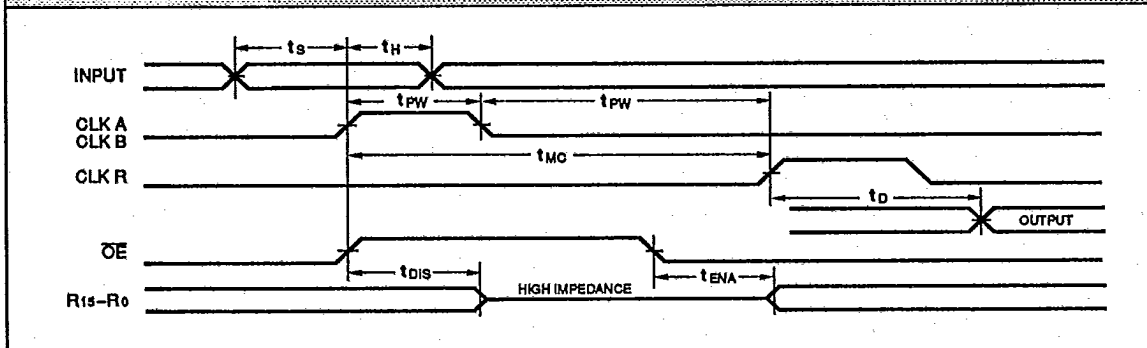
**COMMERCIAL OPERATING RANGE (0°C to +70°C) Notes 9, 10 (ns)**

Symbol Parameter		LMU08/LMU8U-					
		70		50		35	
		Min	Max	Min	Max	Min	Max
t <sub>MC</sub>	Multiply Time (Clocked)		70		50		35
t <sub>D</sub>	Output Delay		25		20		18
t <sub>ENA</sub>	Output Enable Time (Note 11)		20		18		18
t <sub>DIS</sub>	Output Disable Time (Note 11)		18		17		17
t <sub>PW</sub>	Clock Pulse Width	20		20		10	
t <sub>H</sub>	Input Register Hold Time	4		0		0	
t <sub>S</sub>	Input Register Setup Time	14		14		14	

**MILITARY OPERATING RANGE (-55°C to +125°C) Notes 9, 10 (ns)**

Symbol Parameter		LMU08/LMU8U-					
		90		60		45	
		Min	Max	Min	Max	Min	Max
t <sub>MC</sub>	Multiply Time (Clocked)		90		60		45
t <sub>D</sub>	Output Delay		35		20		20
t <sub>ENA</sub>	Output Enable Time (Note 11)		35		20		20
t <sub>DIS</sub>	Output Disable Time (Note 11)		35		18		18
t <sub>PW</sub>	Clock Pulse Width	25		20		15	
t <sub>H</sub>	Input Register Hold Time	5		0		0	
t <sub>S</sub>	Input Register Setup Time	20		15		15	

**SWITCHING WAVEFORMS**



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NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above VCC will be clamped beginning at -0.6 V and VCC + 0.6 V. The device can withstand indefinite operation with inputs in the range of -3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

- N = total number of device outputs
- C = capacitive load per output
- V = supply voltage
- F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of VCC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except tEN/tDIS test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified IOL and IOH plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 μF ceramic capacitor should be installed between VCC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device VCC and the tester common, and device ground and tester common.

b. Ground and VCC supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and VCC noise to maintain required DUT input levels relative to the DUT ground pin.

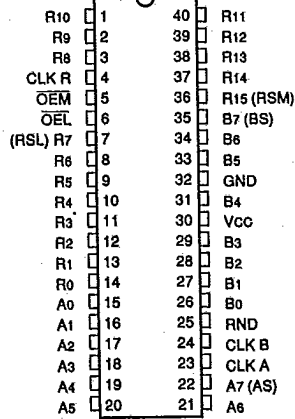
10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

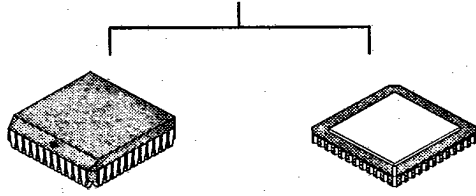
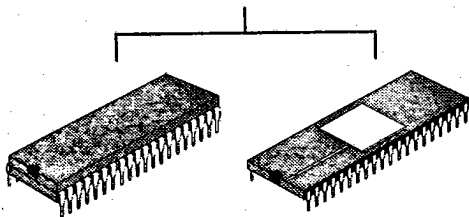
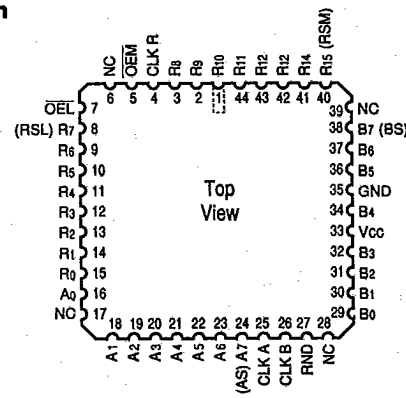
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**LMU08 — ORDERING INFORMATION**

**40-pin**



**44-pin**



Speed	Plastic DIP (P3)	Sidebraze Hermetic DIP (D3)	Plastic J-Lead Chip Carrier (J1)	Ceramic Leadless Chip Carrier (K2)
<b>0°C to +70°C — COMMERCIAL SCREENING</b>				
70 ns	LMU08PC70	LMU08DC70	LMU08JC70	LMU08KC70
50 ns	• • 50	• • 50	• • 50	• • 50
35 ns	• • 35	• • 35	• • 35	• • 35
<b>-55°C to +125°C — COMMERCIAL SCREENING</b>				
90 ns		LMU08DM90		LMU08KM90
60 ns		• • 60		• • 60
45 ns		• • 45		• • 45
<b>-55°C to +125°C — EXTENDED SCREENING</b>				
90 ns		LMU08DME90		LMU08KME90
60 ns		• • 60		• • 60
45 ns		• • 45		• • 45
<b>-55°C to +125°C — MIL-STD-883 COMPLIANT</b>				
90 ns		LMU08DMB90		LMU08KMB90
60 ns		• • 60		• • 60
45 ns		• • 45		• • 45



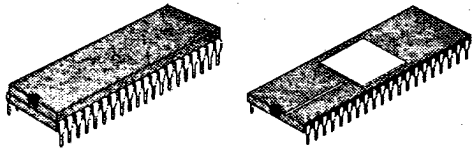
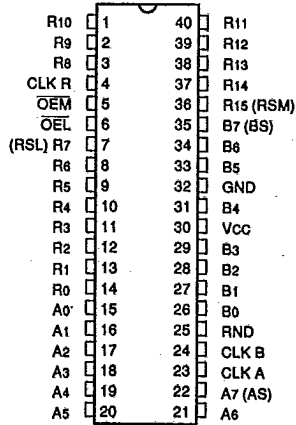
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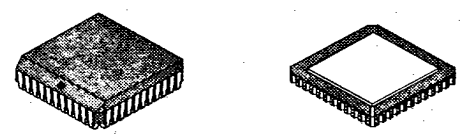
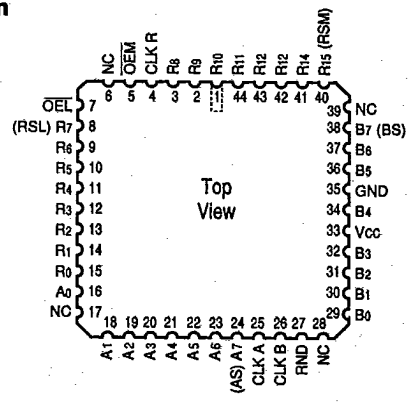
LDS.08/BU-B

**LMU8U — ORDERING INFORMATION**

40-pin



44-pin



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Speed	Plastic DIP (P3)	Sidebraze Hermetic DIP (D3)	Plastic J-Lead Chip Carrier (J1)	Ceramic Leadless Chip Carrier (K2)
<b>0°C to +70°C — COMMERCIAL SCREENING</b>				
70 ns	LMU8UPC70	LMU8UDC70	LMU8UJC70	LMU8UKC70
50 ns	▪ ▪ 50	▪ ▪ 50	▪ ▪ 50	▪ ▪ 50
35 ns	▪ ▪ 35	▪ ▪ 35	▪ ▪ 35	▪ ▪ 35
<b>-55°C to +125°C — COMMERCIAL SCREENING</b>				
90 ns		LMU8UDM90		LMU8UKM90
60 ns		▪ ▪ 60		▪ ▪ 60
45 ns		▪ ▪ 45		▪ ▪ 45
<b>-55°C to +125°C — EXTENDED SCREENING</b>				
90 ns		LMU8UDME90		LMU8UKME90
60 ns		▪ ▪ 60		▪ ▪ 60
45 ns		▪ ▪ 45		▪ ▪ 45
<b>-55°C to +125°C — MIL-STD-883 COMPLIANT</b>				
90 ns		LMU8UDMB90		LMU8UKMB90
60 ns		▪ ▪ 60		▪ ▪ 60
45 ns		▪ ▪ 45		▪ ▪ 45