Am27S02/Am27S03

64-Bit Inverting-Output Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 16 word x 4-bit low-power Schottky RAMS
- Ultra-Fast Version: Address access time 25 ns
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with open-collector outputs (Am27S02) or with three-state outputs (Am27S03)
- Pin-compatible replacements for 3101A, 74S289, (use Am27S02); for 74S189, (use Am27S03)

GENERAL DESCRIPTION

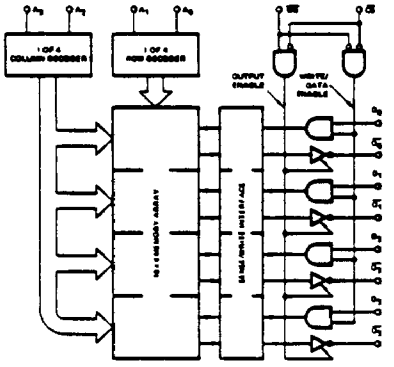
The Am27S02 and Am27S03 are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active-LOW chip select ($\overline{CS}$) input and open-collector OR-tieable outputs (Am27S02) or three-state outputs (Am27S03). Chip selection for large memory systems can be controlled by active-LOW output decoders such as the Am74S138.

An active-LOW Write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word and preconditions the output circuitry so that correct data is present at the outputs when the write cycle is complete. This preconditioning operation ensures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{O_0}$ to $\overline{O_3}$.

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

BLOCK DIAGRAM



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MODE SELECT TABLE

Input		Data Output Status $\overline{O_0} - \overline{O_3}$	Mode
$\overline{CS}$	$\overline{WE}$		
L	L	Output Disabled	Write
L	H	Selected Word (Inverted)	Read
H	X	Output Disabled	Deselect

H = HIGH
L = LOW
X = Don't Care

PRODUCT SELECTOR GUIDE

Access Time	25 ns	30 ns	35 ns	50 ns
I_{CC}	70 mA	70 mA	70 mA	70 mA
Temperature Range	C	M	C	M
Open Collector	Am27S02A	Am27S02A	Am27S02	Am27S02
Three State	Am27S03A	Am27S03A	Am27S03	Am27S03

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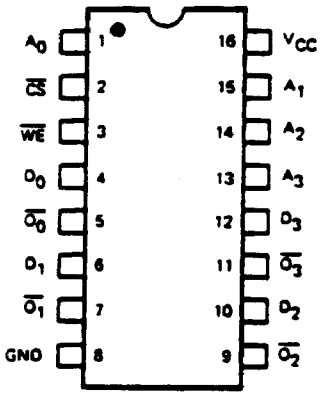
CONNECTION DIAGRAMS
Top View

DIP*



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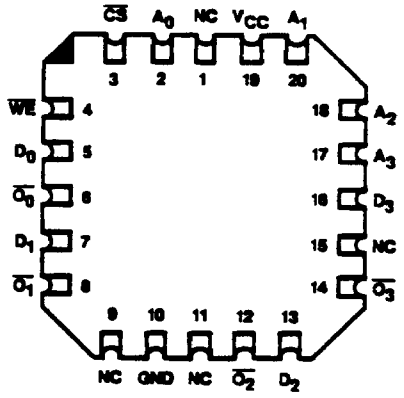
LCC



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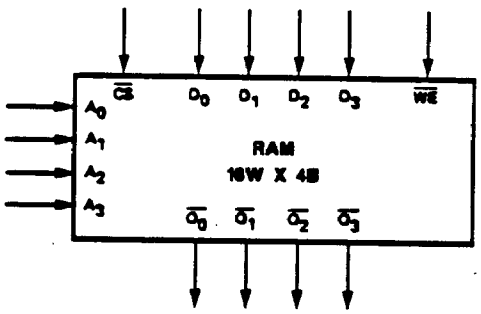
*Also available in 16-Pin Ceramic Flatpack. Connections identical to DIPs.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



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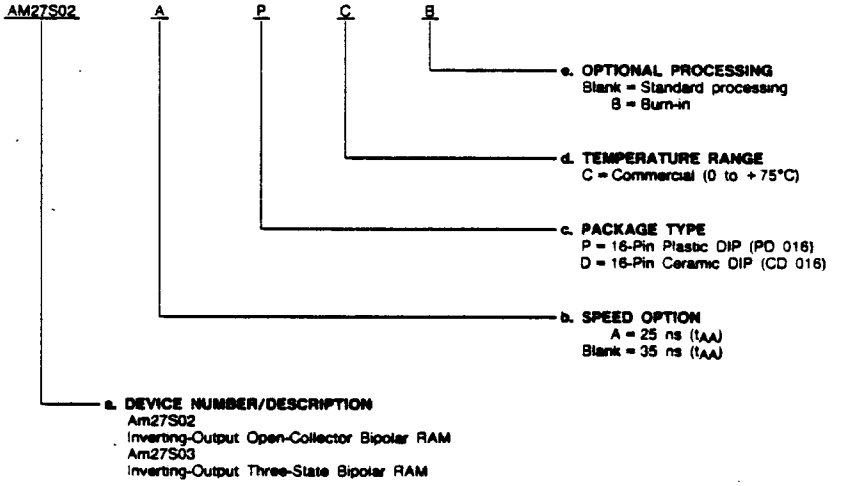
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option** (if applicable)
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM27S02	PC, PCB, DC, DCB
AM27S02A	
AM27S03	
AM27S0A	

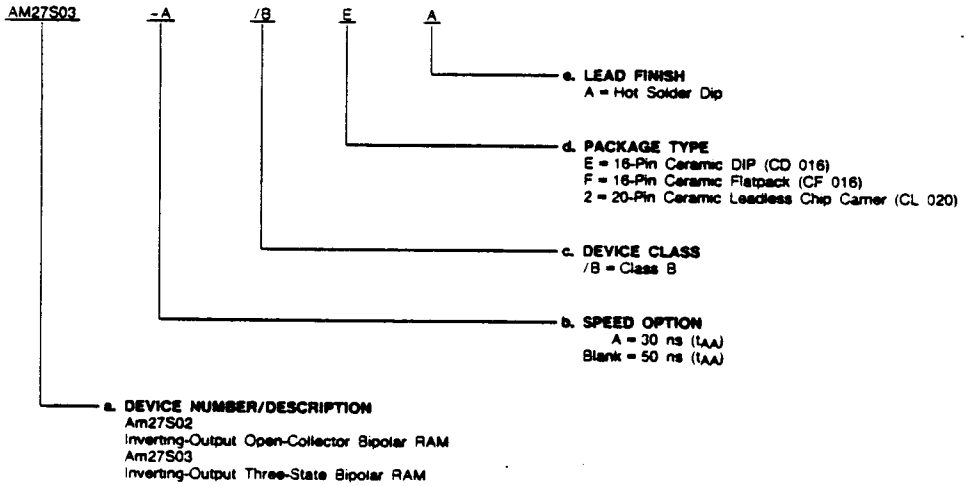
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM27S02	/BEA, /BFA, /82A
AM27S02A	
AM27S03	
AM27S03A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 V to +V_{CC} Max.
DC Input Voltage ..... −0.5 V to +5.5 V
Output Current into Outputs ..... 20 mA
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military* (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

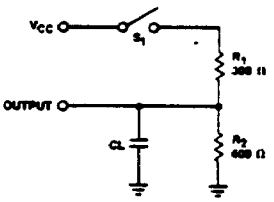
*Military products 100% tested at T_C = +25°C, +125°C, and −55°C.
(see note 5)

DC CHARACTERISTICS over opeating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Am27S02/Am27S03 Min.	Typ.	Max.	Unit
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2 mA	COM'L	2.4	3.0		V
			I_{OH} = −2.0 mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA			350	450	mV
			I_{OL} = 20 mA			380	500	
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 3)			2.0			V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs (Note 3)					0.8	
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V	$\overline{WE}$, D_0–D_3, A_0–A_3			−15	−250	μA
			$\overline{CS}$			−30	−250	
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V				0	10	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 4)			−20	−45	−90	mA
I_{CC}	Power Supply Current	All Inputs = GND Outputs = Open V_{CC} = Max.				50	70	
V_{CL}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−0.85	−1.2	V
I_{CEX}	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} V_{OUT} = 2.4 V, V_{CC} = Max.				0	40	μA
		$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} V_{OUT} = 0.4 V, V_{CC} = Max.		(Note 2)	−40	0		

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. Operating specifications with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performance instantaneously where T_A = T_C = T_J.
θ_{JA} ≈ 50 °C/W (with moving air) for Ceramic DIP.
θ_{JA} ≈ 10-17°C/W for flatpack and leadless chip carrier.

SWITCHING TEST CIRCUIT



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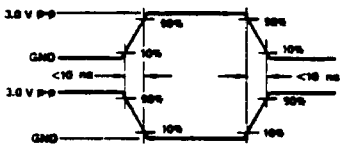
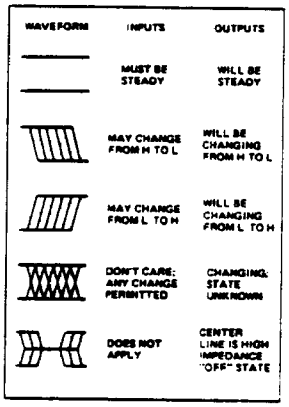
SWITCHING TEST WAVEFORM



TW000031

KEY TO THE SWITCHING WAVEFORMS



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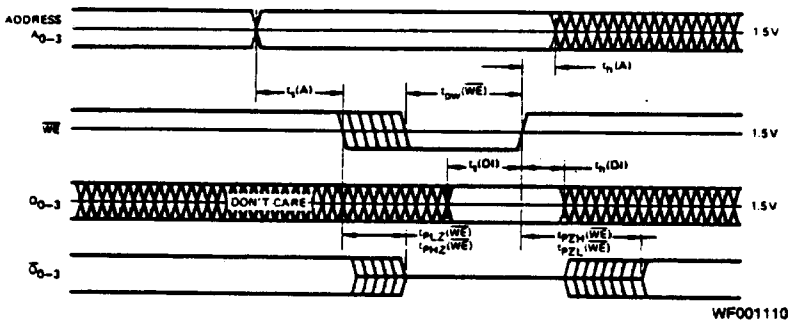
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified*

No.	Parameter Symbol	Parameter Description	Am27S02A/3A· A C Devices Min.	Am27S02A/3A· A C Devices Max.	Am27S02A/3A· A M Devices Min.	Am27S02A/3A· A M Devices Max.	Am27S02/3 STD C Devices Min.	Am27S02/3 STD C Devices Max.	Am27S02/3 STD M Devices Min.	Am27S02/3 STD M Devices Max.	Units
1	$t_{PLH}(A)$	Delay from Address to Output		25		30		35		50	ns
2	$t_{PHL}(A)$										
3	$t_{PZH}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data		15		20		17		25	ns
4	$t_{PZL}(\overline{CS})$										
5	$t_{PZH}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery-See Note 1)		20		25		35		40	ns
6	$t_{PZL}(\overline{WE})$										
7	$t_s(A)$	Setup Time Address (Prior to Initation of Write)	0		0		0		0		ns
8	$t_h(A)$	Hold Time Address (After Termination of Write)	0		0		0		0		ns
9	$t_s(DI)$	Setup Time Data Input (Prior to Termination of Write)	20		25		25		25		ns
10	$t_h(DI)$	Hold Time Data Input (After Termination of Write)	0		0		0		0		ns
11	$t_{pw}(\overline{WE})$	MIN Write Enable Width Pulse to Insure Write	20		25		25		25		ns
12	$t_{PHZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (HI-Z)		15		20		17		25	ns
13	$t_{PLZ}(\overline{CS})$										
14	$t_{PLZ}(\overline{WE})$	Delay from Write Enable (LOW) to Inactive Output (HI-Z)		20		25		25		35	ns
15	$t_{PHZ}(\overline{WE})$										

Notes:
1. Output is preconditioned to data in during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
2. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with S_1 closed and C_L = 50 pF with both input and output timing referenced to 1.5 V.
3. For open collector, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output (D_{OUT}), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed and C_L = 30 pF and with both the input and output timing referenced to 1.5 V.
4. For 3-state output, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with S_1 open, C_L = 50 pF and with both the input and output timing referenced to 1.5 V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed, C_L = 50 pF and with both the input and output timing referenced to 1.5 V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with S_1 open and $C_L \leq 5$ pF and are measured between the 1.5 V level on the input to the V_{OH} – 500 mV level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with S_1 closed and $C_L \leq 5$ pF and are measured between the 1.5 V level on the input and the V_{OL} + 500 mV level on the output.

SWITCHING WAVEFORMS



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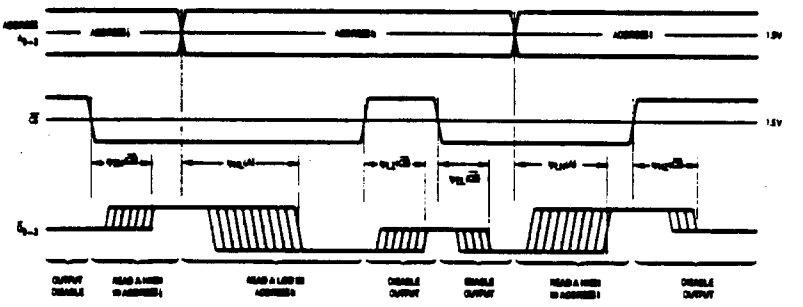
Write Mode

Write Cycle Timing. The cycle is initiated by an address change. After t_s(A)min, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A)min must be allowed before the address may be changed again. The output will be inactive (floating for the Am27S03) while the write enable is ($\overline{WE}$) LOW.



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Read Mode

Switching delays from address and chip select inputs to the data output. For the Am27S03 disabled output is "OFF", represented by a single center line. For the Am27S02, a disabled output is HIGH.