PERICOM Enabling Serial Connectivity

Product Brief

Product: **PCIe® Packet Switch - 5-Port/5-lane**

Part Numbers: **PI7C9X20505GP GreenPacket™ Family**

Product Description

The PI7C9X20505GP is a 5-port, 5-lane, PCI Express® Packet Switch specifically designed to meet the latest GREEN low-power, lead (Pb)-free system requirements, such as laptop, docking station, and other mobile or power sensitive platforms. The name of the family, GreenPacket™, refers to Pericom proprietary power saving technology.

The PI7C9X20505GP provides one upstream port supporting x1, and 4 downstream ports that support x1 operation. The PI7C9X20505GP provides users the flexibility to expand or fanout from a wide range of I/O Bridge such as MCH, ICH, nVidia, and it is a suitable solution for HBA, Surveillance, Combo card and other applications.

Industry Specifications Compliance

- PCI Express® Base Specification, Revision 1.1
- PCI Express CEM Specification, Revision 1.1
- PCI-to-PCI® Bridge Architecture Specification, Rev 1.2
- Advanced Configuration Power Interface (ACPI) Specification
- PCI Standard Hot-Plug Controller (SHPC) and Subsystem Specification Revision 1.0

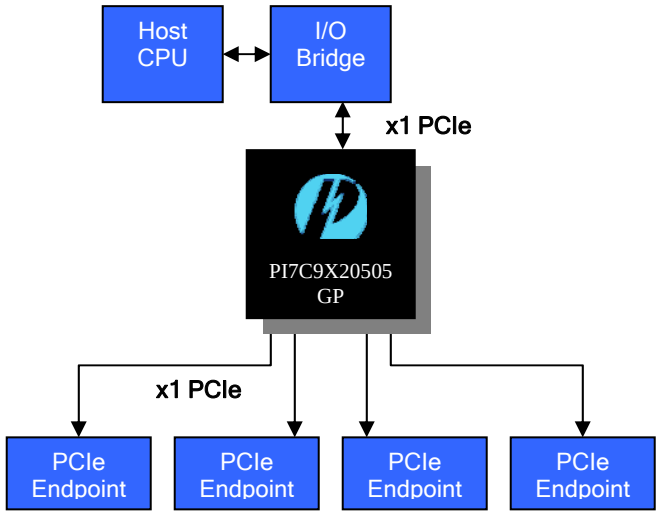
Features

- Non-blocking full-wired switching capability at 16 Gbps when all 4 lanes are enabled
- Peer-to-peer switching between any 2 downstream ports
- Reliability, Availability and Serviceability
  - Supports Data Poisoning and End-to-End CRC
  - Advanced Error Reporting and Logging
  - Hot Plug support
  - IEEE 1149.6 JTAG interface support
- Link Power Management
  - Supports L0, L0s, L1, L2, L2/$L3_{Ready}$ and L3 link power state
  - Active state power management for L0s and L1 state
  - Beacon or Wake# support in L2 state
- Device State Power Management
  - Supports D0, $D3_{Hot}$ and $D3_{Cold}$
  - 3.3V Aux Power support in $D3_{Cold}$ power state
- Port Arbitration: Round Robin (RR), Weighted RR and Time-based Weighted RR
- Extended Virtual Channel capability:
  - Two Virtual Channels (VC) and Eight Traffic Class (TC) support
  - Non-enabled VC buffer assigned to enabled VCs for resource sharing
  - Independent TC/VC mapping per each port
  - Provides VC arbitration selections: Strict Priority, Round Robin (RR) and Programmable Weighted RR
- Supports Isochronous Traffic
  - Isochronous traffic class mapped to VC1 only
  - Strict time based credit policing
- Header/Data queue at each VC of each port
  - Four-entry non-posted request header and data (VC0 only) queue
  - Four-entry posted request header queue
  - Four-entry completion header queue
  - 512-byte posted write data buffer
  - 512-byte completed read data buffer
- Supports up to 256-byte maximum payload size
- Power Dissipation: 0.75W typical in L0 normal mode
- Industrial Temperature Range -40° to 85°
- Package: 17x17mm, 256-pin PBGA, w/1.0mm ball pitch - Pb free and 100% Green.

Enhanced Features

- Programmable Driver Current and De-Emphasis Level at each individual port
- 150ns typical latency for packet running through switch without blocking
- Supports “Cut-through”(Default) as well as “Store and Forward” mode for switching packets
- Supports up to 256-byte maximum payload size
- Advanced Power Savings
  - Empty downstream ports are set to idle
  - Clock to corresponding circuit is turned off when any port enters L1 or ASPM L1

Application



Pericom Semiconductor Corp.
www.pericom.com
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