

NTMS4118N

Product Preview

Power MOSFET

30 V, 14.8 A, Single N-Channel, SO-8

Features

- Low $R_{DS(on)}$
- Fast Switching Times
- Pb-Free Package is Available

Applications

- Notebooks, Graphics Cards
- Low Side Switch
- DC-DC

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	30	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	12.3	A
		$T_A = 85^\circ\text{C}$		8.8	
	$t \leq 10$ s	$T_A = 25^\circ\text{C}$		14.8	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	P_D	1.5	W
				$t \leq 10$ s	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	I_D	9.1	A
		$T_A = 85^\circ\text{C}$		6.6	
Power Dissipation (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	P_D	0.9	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$		I_{DM}	44	A
Operating Junction and Storage Temperature			T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode)			I_S	2.8	A
Single Pulse Drain-to-Source Avalanche Energy			E_{AS}	TBD	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^\circ\text{C}$

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	81.5	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - $t \leq 10$ s (Note 1)	$R_{\theta JA}$	56	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	146.5	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Surface mounted on FR4 board using 1 in sq pad size (Cu area 1.127 in sq [1 oz] including traces).
2. Surface mounted on FR4 board using the minimum recommended pad size (Cu area = TBD in sq).

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

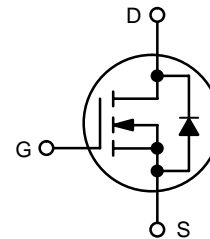


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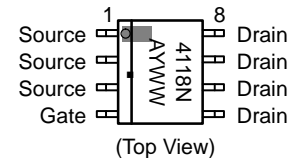
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX (Note 1)
30 V	4.6 m Ω @ 10 V	14.8 A
	6.5 m Ω @ 4.5 V	



MARKING DIAGRAM/ PIN ASSIGNMENT



SO-8
CASE 751
STYLE 12



4118N = Specific Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTMS4118NR2	SO-8	2500/Tape & Reel
NTMS4118NR2G	SO-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTMS4118N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			TBD		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 24 V	T _J = 25°C		1.0	μA
			T _J = 125°C		10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.5		2.5	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			TBD		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 12.3 A		4.6	6.0	mΩ
		V _{GS} = 4.5 V, I _D = 10.3 A		6.5	8.5	
Forward Transconductance	g _{FS}	V _{DS} = 15 V, I _D = 10 A		1.5		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 24 V		3600		pF
Output Capacitance	C _{OSS}			550		
Reverse Transfer Capacitance	C _{RSS}			320		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 24 V, I _D = 10.3 A		32	35	nC
Threshold Gate Charge	Q _{G(TH)}			3.8		
Gate-to-Source Charge	Q _{GS}			11		
Gate-to-Drain Charge	Q _{GD}			15.2		
Gate Resistance	R _G			1.2		

SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 4)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 4.5 V, V _{DS} = 15 V, I _D = 1.0 A, R _G = 6.0 Ω		29.6		ns
Rise Time	t _r			30.4		
Turn-Off Delay Time	t _{d(OFF)}			37.6		
Fall Time	t _f			26.7		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 2.8 A	T _J = 25°C		0.8	1.0	V
			T _J = 125°C		TBD		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, di _S /dt = 100 A/μs, I _S = 2.8 A			33.2		ns
Charge Time	t _a				17		
Discharge Time	t _b				16		
Reverse Recovery Charge	Q _{RR}				0.0335		

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

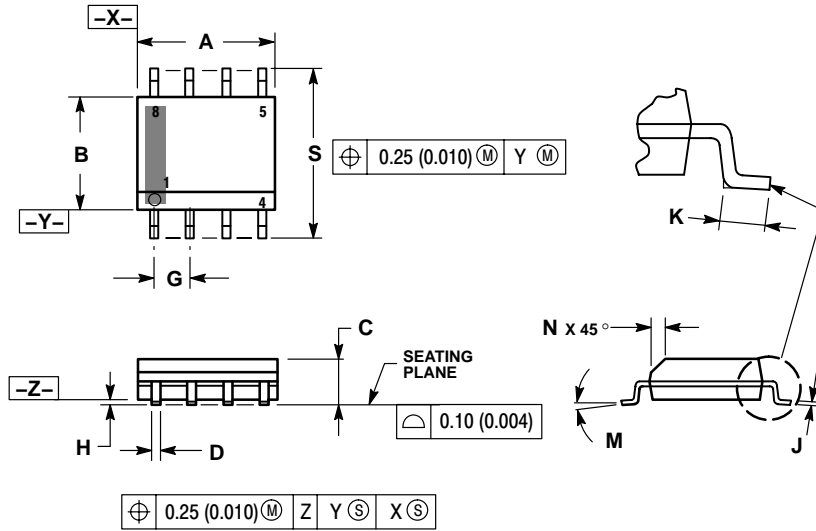
4. Switching characteristics are independent of operating junction temperatures.

NTMS4118N

PACKAGE DIMENSIONS

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SO-8
CASE 751-07
ISSUE AF



NOTES:

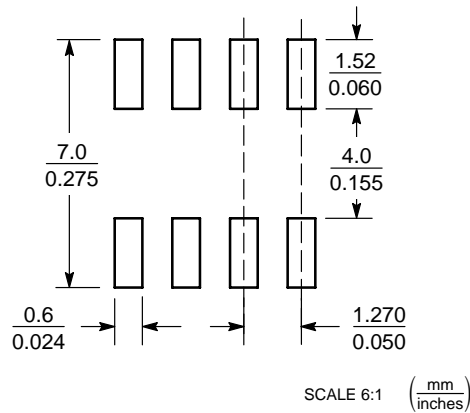
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0° - 8°		0° - 8°	
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 12:

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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