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DEVICE SPECIFICATION FOR
TFT-LCD Module
 MODEL No.
LQ150X1LBS2



FU-15-007-1

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1. Application

This specification applies to a color TFT-LCD module, LQ150X1LBS2.

2. Overview

This module is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver ICs, control circuit and power supply circuit and a backlight unit. Graphics and texts can be displayed on a 1024×3×768 dots panel with 262,144 colors by using LVDS (Low Voltage Differential Signaling) to interface and supplying +3.3V DC supply voltage for TFT-LCD panel driving and supply voltage for backlight.

In this TFT-LCD panel, low reflection / color filters of excellent color performance and backlights of high brightness are incorporated to realize brighter and clearer pictures, making this model optimum for use in multi-media applications.

Optimum viewing direction is 6 o'clock.

Backlight-driving DC/AC inverter is not built in this module.

3. Mechanical Specifications

Parameter	Specifications	Unit
Display size	38 (15.0") Diagonal	cm
Active area	304.1 (H)×228.1 (V)	mm
Pixel format	1024 (H)×768 (V)	pixel
	(1 pixel = R+G+B dots)	
Aspect ratio	4 : 3	
Pixel pitch	0.297 (H)×0.297 (V)	mm
Pixel configuration	R,G,B vertical stripe	
Display mode	Normally white	
Surface treatment	Glare and hard-coating 2H Low reflection	

Parameter	Min.	Typ.	Max.	Unit	
Unit outline dimensions [Note 1]	Width	316.8	317.3	317.8	mm
	Height	241.5	242.0	242.6	mm
	Depth	—	—	6.5	mm
Mass	—	580	600	g	

[Note 1] excluding backlight cables.

Outline dimensions is shown in Fig.2

4. Input Terminals

4-J, TFT-LCD panel driving

CNI (LVDS signals and +3.3V DC power supply)

Pin No.	Symbol	Function	Remark
1	GND		
2	Vcc	+3.3V power supply	
3	Vcc	+3.3V power supply	
4	Vedid	DDC +3.3V power supply	[Note 4]
5	NC		[Note 3]
6	CLKedid	DDC Clock	[Note 4]
7	DATAedid	DDC Data	[Note 4]
8	RxIN0-	Receiver signal of LVDS CH0 (-)	[Note 1]
9	RxIN0+	Receiver signal of LVDS CH0 (+)	[Note 1]
10	GND		
11	RxIN1-	Receiver signal of LVDS CH1 (-)	[Note 1]
12	RxIN1+	Receiver signal of LVDS CH1 (+)	[Note 1]
13	GND		
14	RxIN2-	Receiver signal of LVDS CH2 (-)	[Note 1]
15	RxIN2+	Receiver signal of LVDS CH2 (+)	[Note 1]
16	GND		
17	CK IN-	Receiver signal of LVDS CLK (-)	[Note 1]
18	CK IN+	Receiver signal of LVDS CLK (+)	[Note 1]
19	GND		
20	NC		[Note 3]
21	NC		[Note 3]
22	GND		
23	NC		[Note 3]
24	NC		[Note 3]
25	GND		
26	NC		[Note 3]
27	NC		[Note 3]
28	GND		
29	NC		[Note 3]
30	NC		[Note 3]

[Note 1] Relation between RxINi(i=0,1,2) and actual data is shown in following section (4-2)(7-2).

[Note 2] The shielding case is connected with signal GND.

[Note 3] Please use NC by OPEN or GND. NC terminal is not connected with the internal circuit.

[Note 4] In case of you don't use EDID, use this pin as OPEN or GND.

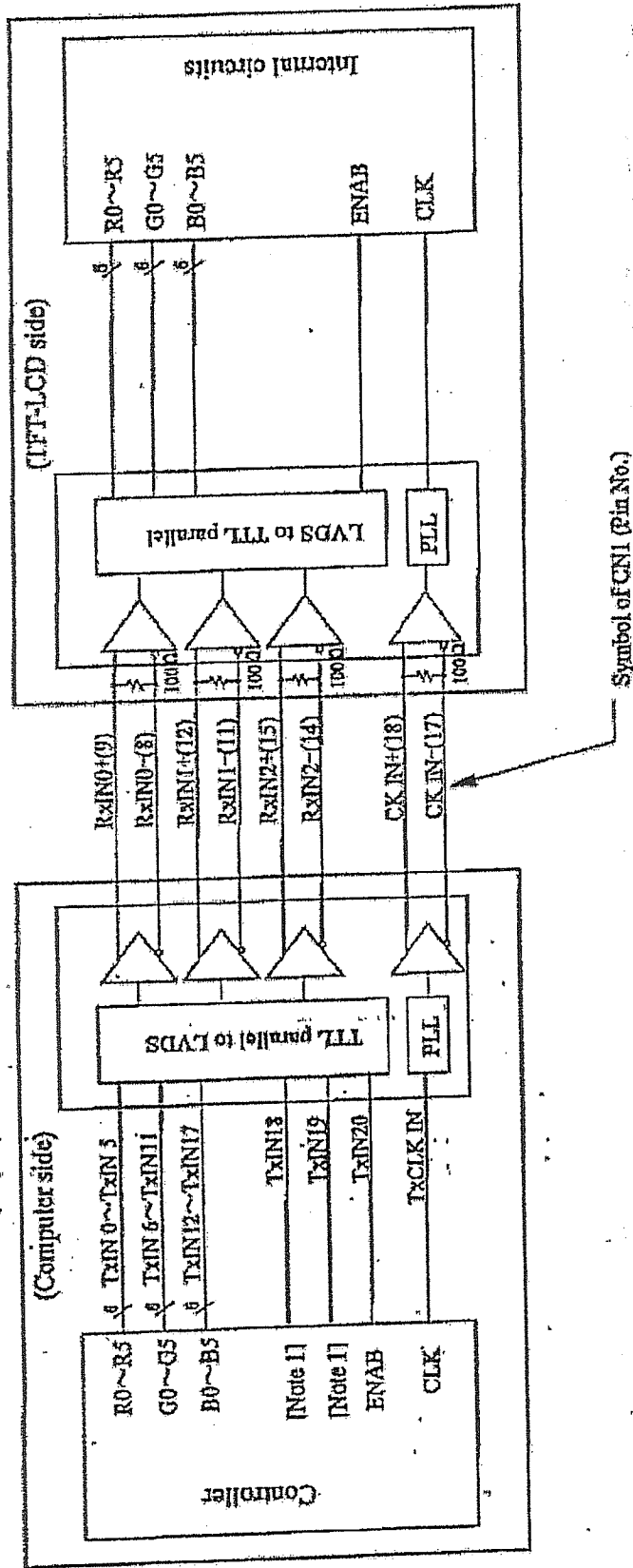
Using connector: FI-XB30EL-HF10 (JAB) or equivalent.

Corresponding connector: FI-X30M, FI-X30ML or FI-X30H (JAE)

(Sharp is not responsible to its product quality, if the user applies a connector not corresponding to the above model.)

4-2 LVDS interface block diagram

Using receiver : Single LVDS interface contained in a control IC
 Corresponding Transmitter : THC63LYDM63A (CRINE) or equivalent



[Note 1] Do not use at high-impedance TXIN 18 - 19.

4-3. Backlight driving

CN2 Using connector: BHSR-02YS-1(JST)

Mating connector : SM02B-BHSS-1-1B(JST)

(Sharp is not responsible to its product quality, if the user applies a connector not corresponding to the above model.)

Connector No.	Pin No.	Symbol	Function	FL cable color
CN2	1	V_{High}	Power supply for lamp (High voltage side)	Blue
	2	V_{Low}	Power supply for lamp (Low voltage side)	White

5. Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings		Unit	Remark
			Min.	Max.		
Input voltage	V_I	$T_a=25^\circ\text{C}$	-0.3	$V_{cc}+0.3$	V	[Note 1]
+3.3V supply voltage	V_{cc}	$T_a=25^\circ\text{C}$	0	+4.0	V	
Storage temperature	T_{stg}	—	-25	+60	$^\circ\text{C}$	[Note 2]
Operating temperature (Ambient)	T_{opa}	—	0	+50	$^\circ\text{C}$	

[Note 1] LVDS signals

[Note 2] Humidity : 95%RH Max. at $T_a \leq +40^\circ\text{C}$.Maximum wet-bulb temperature at $+39^\circ\text{C}$ or less at $T_a > +40^\circ\text{C}$.

No condensation.

6. Electrical Characteristics

6-1. TFT-LCD panel driving

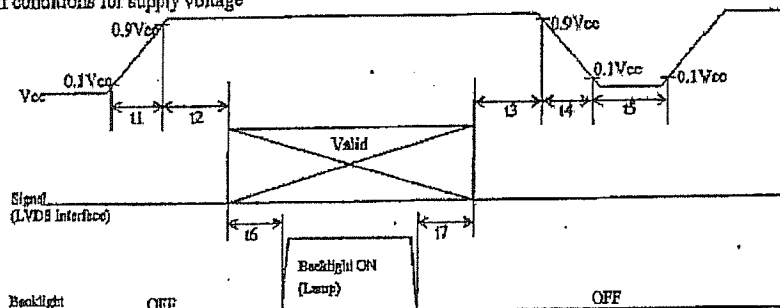
 $T_a = +25^\circ\text{C}$

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply voltage	V_{cc}	+3.0	+3.3	+3.6	V	[Note 2]
Current dissipation	I_{cc}	—	265	400	mA	[Note 3]
Permissive input ripple voltage	V_{RP}	—	—	100	mV _{RP}	$V_{cc} = +3.3\text{V}$
Input voltage range	V_I	0	—	2.4	V	LVDS signals
Differential input threshold voltage	High	V_{TH}	—	+100	mV	$V_{CM} = +1.2\text{V}$ [Note 1]
	Low	V_{TL}	-100	—	mV	
Input current (High)	I_{OH}	—	—	± 10	μA	$V_I = +2.4\text{V}$ $V_{cc} = +3.6\text{V}$
Input current (Low)	I_{OL}	—	—	± 10	μA	$V_I = 0\text{V}$ $V_{cc} = 3.6\text{V}$
Terminal resistor	R_T	—	100	—	Ω	Differential input

[Note 1] V_{CM} : Common mode voltage of LVDS driver.

[Note 2]

On-off conditions for supply voltage



Symbol	Min.	Max.	Unit	Remark
t1	0	10	ms	
t2	0	1	s	
t3	0	1	s	
t4	0	400	ms	
t5	200	—	ms	
t6	180	—	ms	*1
t7	5	—	ms	*1

*1: As for the power sequence for backlight, it is recommended to apply above mentioned input timing. If the backlight is lit on and off at a timing other than shown above, displaying image may get disturbed. This is due to variation of output signal from timing generator when LVDS signal is changed from on to off or vice versa, but has no harm to the module itself.

[Note] Do not keep the interface signal high-impedance or unusual signal when power is on.

Vcc-dip conditions

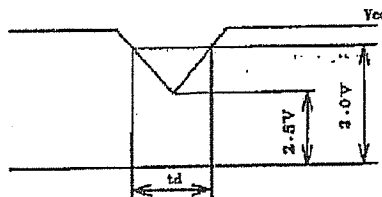
- 1) $2.5V \leq V_{cc} < 3.0V$

$t_d \leq 10 \mu s$

Under above condition, the display image should return to an appropriate figure after Vcc voltage recovers.

- 2) $V_{cc} < 2.5V$

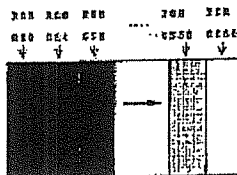
Vcc-dip conditions should also follow the On-off conditions for supply voltage



[Note 3] Typical current situation : 16-gray-bar pattern.

$V_{cc} = +3.3V$

Maximum current situation : $V_{cc} = +3.0V$



6-2. Backlight driving

The backlight system is edge-lighting type with single CCFT (Cold Cathode Fluorescent Tube).

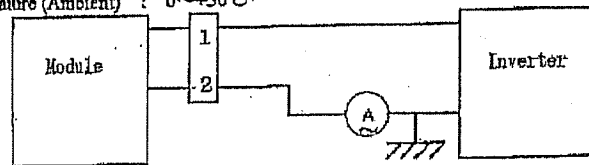
The characteristics of one lamp are shown in the following table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp current range	I_L	3.0	6.0	6.5	mA _{rms}	[Note 1]
Lamp voltage	V_L	—	690	—	V _{rms}	
Lamp power consumption	P_L	—	4.1	—	W	[Note 2]
Lamp frequency	F_L	42	52	70	kHz	[Note 3]
Kick-off voltage	V_S	—	—	1450	V _{rms}	Ta=25°C
		—	—	1600	V _{rms}	Ta=0°C
Lamp life time	L_L	10000	—	—	Hour	[Note 5]

[Note 1] The lamp current range, which can be turned on, is shown.

Lamp current measures by connecting the ammeter for high frequency to the V_{Low} side in the circuit of the following figure.

- Lamp frequency : 42~70kHz
- Temperature (Ambient) : 0~450°C



* 2pin is V_{Low}

In addition, please check lighting starting nature and lighting stability after mounting a module and an inverter on the occasion of use in a low current region.

[Note 2] Calculated value for reference ($I_L \times V_L$)

[Note 3] Lamp frequency may produce interference with horizontal synchronous frequency, and this may cause beat on the display. Therefore lamp frequency shall be detached as much as possible from the horizontal synchronous frequency and from the harmonics of horizontal synchronous to avoid interference.

[Note 4] It is defined at 22pF for the ballast capacitor of a DC/AC inverter.

The voltage above this value should be applied to the lamp for more than 1 second to start-up. Otherwise the lamp may not be turned on.

[Note 5] Above value is applicable when the long side of LCD module is placed horizontally. (Landscape position)
(Lamp lifetime may vary if LCD module is in portrait position due to the change of mercury density inside the lamp)

Lamp life time is defined as the time when either ① or ② occurs in the continuous operation under the condition of $T_a = 25^\circ\text{C}$ and $I_L = 6.0 \text{ mA}_{rms}$.

① Brightness becomes 50% of the original value under standard condition.

② Kick-off voltage at $T_a = 0^\circ\text{C}$ exceeds maximum value, 1600 V_{rms}.

[Note] The performance of the backlight, for example life time or brightness, is much influenced by the characteristics of the DC-AC inverter for the lamp.

When you design or order the inverter, please make sure that a poor lighting caused by the mismatch of the backlight and the inverter (miss-lighting, flicker, etc.) never occur.

When you confirm it, the module should be operated in the same condition as it is installed in your instrument.

[Note] Insulate the high voltage area in order to prevent direct contacts to the area. As countermeasures for excessive heat or exothermic fire, use protection elements such as fuses to cut the circuit.

Use burn-resistant (or noncombustible) material for board or resin.

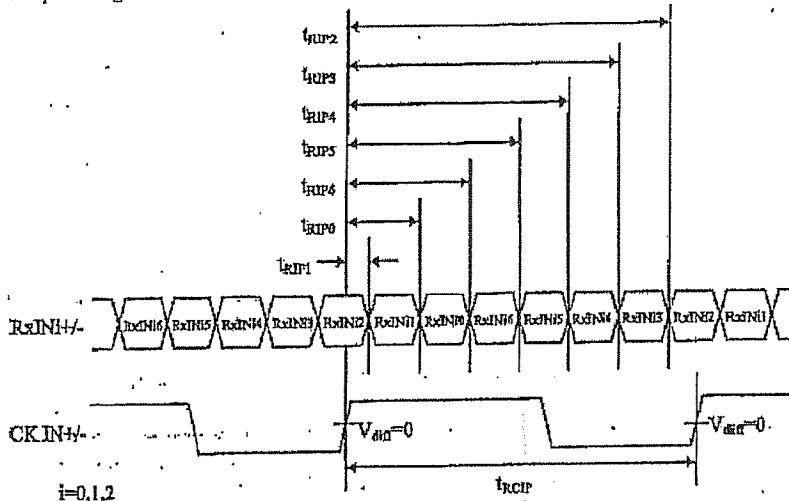
6-3. LVDS input specification

6.3.1. AC characteristics

$V_{CC}=+3.0V \sim +3.6V$, $T_a=0^{\circ}C \sim +50^{\circ}C$

Parameter	Symbol	Min	Typ.	Max.	Unit
Input Data Position 0 (RCIP=15.38ns)	t_{RIP0}	-0.25	0.0	+0.25	ns
Input Data Position 1 (RCIP=15.38ns)	t_{RIP1}	$t_{RCIP}/7-0.25$	$t_{RCIP}/7$	$t_{RCIP}/7+0.25$	ns
Input Data Position 2 (RCIP=15.38ns)	t_{RIP2}	$2 t_{RCIP}/7-0.25$	$2 t_{RCIP}/7$	$2 t_{RCIP}/7+0.25$	ns
Input Data Position 3 (RCIP=15.38ns)	t_{RIP3}	$3 t_{RCIP}/7-0.25$	$3 t_{RCIP}/7$	$3 t_{RCIP}/7+0.25$	ns
Input Data Position 4 (RCIP=15.38ns)	t_{RIP4}	$4 t_{RCIP}/7-0.25$	$4 t_{RCIP}/7$	$4 t_{RCIP}/7+0.25$	ns
Input Data Position 5 (RCIP=15.38ns)	t_{RIP5}	$5 t_{RCIP}/7-0.25$	$5 t_{RCIP}/7$	$5 t_{RCIP}/7+0.25$	ns
Input Data Position 6 (RCIP=15.38ns)	t_{RIP6}	$6 t_{RCIP}/7-0.25$	$6 t_{RCIP}/7$	$6 t_{RCIP}/7+0.25$	ns
Phase Lock Loop Set	t_{RPLL}	—	—	10	ms
Input Clock Period	t_{RCIP}	14.9	15.4	20	ns

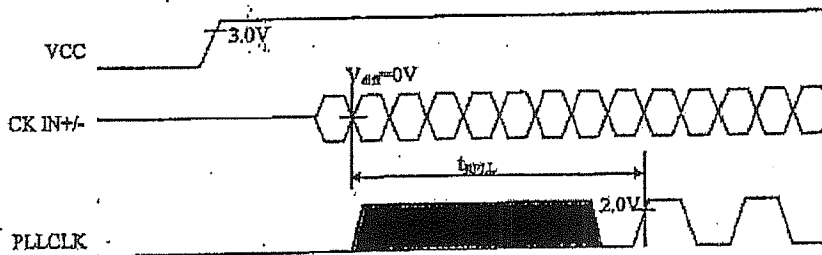
LVDS input timing



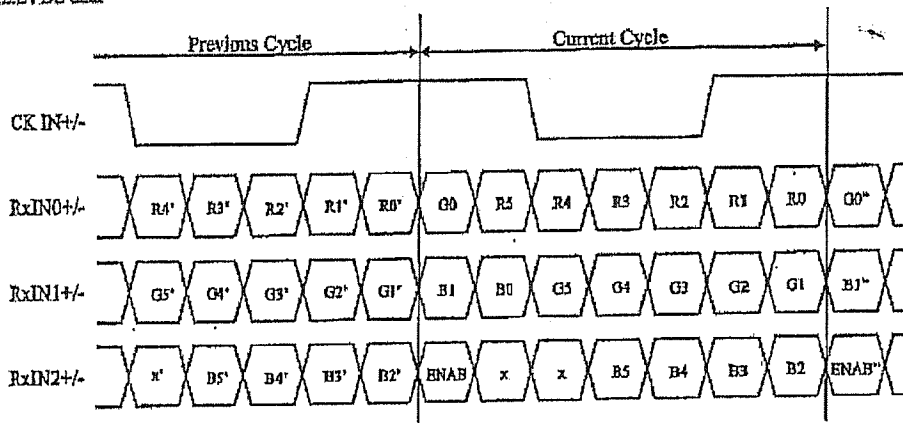
Note

$V_{diff}=(R_x IN+) - (R_x IN-), (CK IN+) - (CK IN-)$

LVDS phase lock loop set



6.3.2.LVDS data



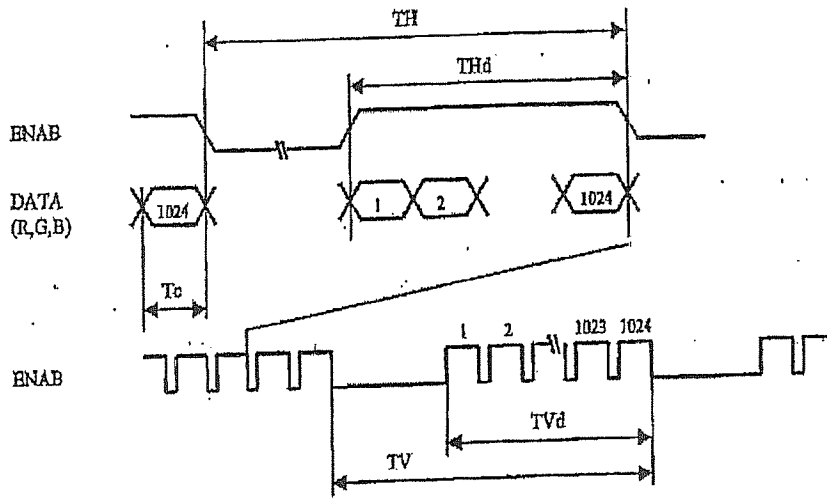
7. Timing Characteristics of Input Signals

7-1. Timing characteristics

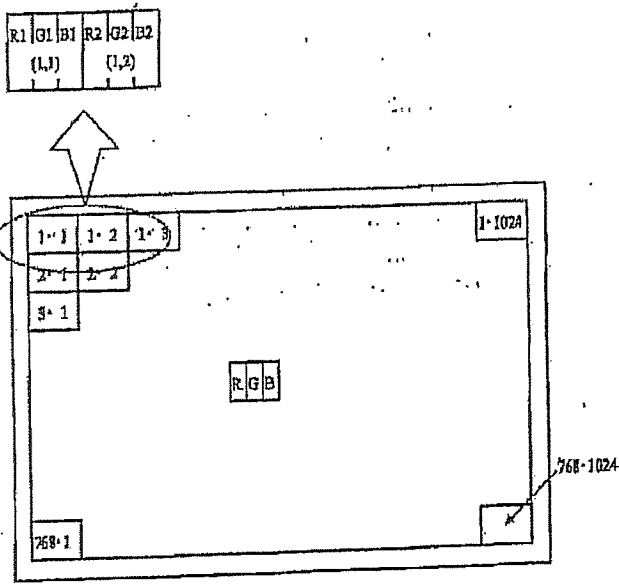
V_{CC}=+3.0V~+3.6V, T_a=0°C~+50°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Clock	Frequency	1/T _c	50	65	67	MHz [Note 1]
Data enable Signal	Horizontal period	TH	1260	1344	1408	clock
			19.38	20.68	—	μs
	Horizontal period (High)	THd	1024	1024	1024	clock
	Vertical period	TV	803	806	900	Line
15.56			16.67	—	ms	
Vertical period (High)	TVd	768	768	768	line	

[Note 1] In case of using the long vertical period, the deterioration of display quality, flicker, etc., may occur.



7-2. Input data signals and display position on the screen



Display position of input data(V·H)

8. Input Signals, Basic Display Colors and Gray Scale of Each Color

Color & Gray scale	Data signal																			
	Gray Scale	R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5	
Basic Color	Black	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	—	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Green	—	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	—	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Red	—	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	—	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	—	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	—	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑	↓			↓				↓				↓							
	↓	↓			↓				↓				↓							
	Brighter	GS61	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	↓	GS62	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS63	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑	GS1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	↑	↓			↓				↓				↓							
	↓	↓			↓				↓				↓							
	Brighter	GS61	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
	↓	GS62	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
	Green	GS63	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑	GS1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	↑	↓			↓				↓				↓							
	↓	↓			↓				↓				↓							
	Brighter	GS61	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1
	↓	GS62	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	Blue	GS63	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

0 : Low level voltage, 1 : High level voltage

Each basic color can be displayed in 64 gray scales from 6 bit data signals. According to the combination of total 18 bit data signals, the 262,144-color display can be achieved on the screen.

9. EDID Specifications

※Please use it by EDID specification in the case of use of EDID.

9-1 EDID data structure

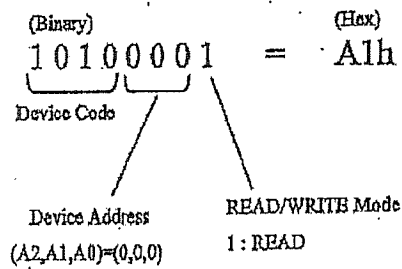
Byte (decimal)	Byte (hex)	Field Name and Comments	Value (Dec)	Value (hex)	Value (Binary)
0	0	Header	0	00	00000000
1	1	Header	255	FF	11111111
2	2	Header	255	FF	11111111
3	3	Header	255	FF	11111111
4	4	Header	255	FF	11111111
5	5	Header	255	FF	11111111
6	6	Header	255	FF	11111111
7	7	Header	0	00	00000000
8	8	EISA manufacture code = SHP	77	4D	01001101
9	9	EISA manufacture code (Compressed ASCII)	16	10	00010000
10	0A	Product code (LQ150X(LBE2 : 5047)	183	B7	10110111
11	0B	Product code (hex LSB first)	19	13	00010011
12	0C	LCD module Serial No (fixed "0")	0	00	00000000
13	0D	LCD module Serial No (fixed "0")	0	00	00000000
14	0E	LCD module Serial No (fixed "0")	0	00	00000000
15	0F	LCD module Serial No (fixed "0")	0	00	00000000
16	10	Week of manufacture (fixed "0")	0	00	00000000
17	11	Year of manufacture - 1990 (ex 2000 - 1990 = 10) (fixed "0")	0	00	00000000
18	12	EDID structure version # = 1	1	01	00000001
19	13	EDID revision # = 3	3	03	00000011
20	14	Video I/p definition = Digital I/p	128	80	10000000
21	15	Max H Image size(cm) = 30cm	30	1E	00011110
22	16	Max V Image size(cm) = 23cm	23	17	00010111
23	17	Display gamma (2.2 x 100) - 100 = 120	120	78	01111000
24	18	Feature support(stanby,suspend,RGB on/off,prefer Time)	202	CA	11001010
25	19	Red/Green Low bit(RxRy/GxGy)	0	00	00000000
26	1A	Blue/White Low bit(BxBy/WxWy)	0	00	00000000
27	1B	Red X(Rx) (written value "0.***")	0	00	00000000
28	1C	Red Y(Ry) (written value "0.***")	0	00	00000000
29	1D	Green X(Gx) (written value "0.***")	0	00	00000000
30	1E	Green Y(Gy) (written value "0.***")	0	00	00000000
31	1F	Blue X(Bx) (written value "0.***")	0	00	00000000
32	20	Blue Y(By) (written value "0.***")	0	00	00000000
33	21	White X(Wx) (written value "0.***")	0	00	00000000

Byte (decimal)	Byte (hex)	Field Name and Comments	Value (Dec)	Value (Hex)	Value (Binary)
34	22	White Y(Wy) (written value "0.***")	0	00	00000000
35	23	Established timings 1	0	00	00000000
36	24	Established timings 2 (1024x768@60Hz "05h")	8	08	00001000
37	25	Established timings 3(Manufacturer's reserved timing)	0	00	00000000
38	26	Standard timing ID1 (Horizontal active pixels)	97	61	01100001
39	27	Standard timing ID1 (Aspect ratio 4:3=4h / Refresh Rate 60Hz-60=0b)	64	40	01000000
40	28	Standard timing ID2	1	01	00000001
41	29	Standard timing ID2	1	01	00000001
42	2A	Standard timing ID3	1	01	00000001
43	2B	Standard timing ID3	1	01	00000001
44	2C	Standard timing ID4	1	01	00000001
45	2D	Standard timing ID4	1	01	00000001
46	2E	Standard timing ID5	1	01	00000001
47	2F	Standard timing ID5	1	01	00000001
48	30	Standard timing ID6	1	01	00000001
49	31	Standard timing ID6	1	01	00000001
50	32	Standard timing ID7	1	01	00000001
51	33	Standard timing ID7	1	01	00000001
52	34	Standard timing ID8	1	01	00000001
53	35	Standard timing ID8	1	01	00000001
54	36	Detailed timing descriptor#1 fck/10000 (=65MHz/10000=6500=1954h)	100	64	01100100
55	37	#1 fck	25	19	00011001
56	38	#1 Horizontal active 1024=0400h "00h"	0	00	00000000
57	39	#1 Horizontal blanking 320=0140h "40h"	64	40	01000000
58	3A	#1 Horizontal active/Horizontal blanking "41h"	65	41	01000001
59	3B	#1 Vertical active 768=0300h "00h"	0	00	00000000
60	3C	#1 Vertical blanking 38=0026h "26h"	38	26	00100110
61	3D	#1 Vertical active/Vertical blanking "30h"	48	30	00110000
62	3E	#1 Horizontal sync, offset 12=00Ch "0Ch"	12	0C	00001100
63	3F	#1 Horizontal sync, width 136=86h	136	88	10001000
64	40	#1 Vertical sync, offset / Vertical sync, width (offset=3h/width=6h)	54	36	00110110
65	41	#1 Horizontal sync, offset/width/Vertical sync, offset/width	0	00	00000000
66	42	#1 Horizontal image size 304mm=0130h "30h"	48	30	00110000
67	43	#1 Vertical image size 228mm=00E4h "E4h"	228	E4	11100100
68	44	#1 Horizontal image size / Vertical image size "10h"	16	10	00010000
69	45	Horizontal border	0	00	00000000

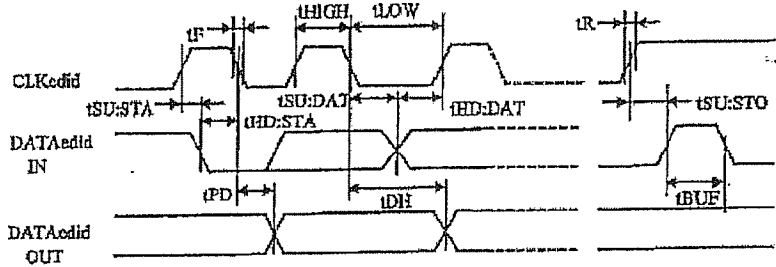
Byte (decimal)	Byte (hex)	Field Name and Comments	Value (Dec)	Value (hex)	Value (binary)
70	46	Vertical border	0	00	00000000
71	47	Flags(Non-interlaced/Horizontal polarity/Vertical polarity)	24	18	00011000
72	48	Detailed timing descriptor #2	0	00	00000000
73	49	Flag	0	00	00000000
74	4A	Reserved	0	00	00000000
75	4B	Dummy Descriptor	16	10	00010000
76	4C	Flag	0	00	00000000
77	4D	1 st dummy	0	00	00000000
78	4E	2 nd dummy	0	00	00000000
79	4F	3 rd dummy	0	00	00000000
80	50	4 th dummy	0	00	00000000
81	51	5 th dummy	0	00	00000000
82	52	6 th dummy	0	00	00000000
83	53	7 th dummy	0	00	00000000
84	54	8 th dummy	0	00	00000000
85	55	9 th dummy	0	00	00000000
86	56	10 th dummy	0	00	00000000
87	57	11 th dummy	0	00	00000000
88	58	New line character #2 indicates end	10	0A	00001010
89	59	Padding with "blank" character	32	20	00100000
90	5A	Detailed timing descriptor #3	0	00	00000000
91	5B	Flag	0	00	00000000
92	5C	Reserved	0	00	00000000
93	5D	Dummy Descriptor	16	10	00010000
94	5E	Flag	0	00	00000000
95	5F	1 st Dummy	0	00	00000000
96	60	2 nd Dummy	0	00	00000000
97	61	3 rd Dummy	0	00	00000000
98	62	4 th Dummy	0	00	00000000
99	63	5 th Dummy	0	00	00000000
100	64	6 th Dummy	0	00	00000000
101	65	7 th Dummy	0	00	00000000
102	66	8 th Dummy	0	00	00000000
103	67	9 th Dummy	0	00	00000000
104	68	10 th Dummy	0	00	00000000
105	69	11 th Dummy	0	00	00000000

Byte (decimal)	Byte (hex)	Field Name and Comments	Value (Dec)	Value (hex)	Value (binary)
106	6A	New line character #3 indicates end	10	0A	00001010
107	6B	Padding with "blank" character	32	20	00100000
108	6C	Detailed timing descriptor #4	0	00	00000000
109	6D	Flag	0	00	00000000
110	6E	Reserved	0	00	00000000
111	6F	Dummy descriptor	16	10	00010000
112	70	Flag	0	00	00000000
113	71	Supplier P/N#1 (L)	76	4C	01001100
114	72	Supplier P/N#2 (Q)	81	51	01010001
115	73	Supplier P/N#3 (I)	49	31	00110001
116	74	Supplier P/N#4 (S)	53	35	00110101
117	75	Supplier P/N#5 (0)	48	30	00110000
118	76	Supplier P/N#6 (X)	88	58	01011000
119	77	Supplier P/N#7 (1)	49	31	00110001
120	78	Supplier P/N#8 (L)	76	4C	01001100
121	79	Supplier P/N#9 (E)	66	42	01000010
122	7A	Supplier P/N#10 (S)	83	53	01010011
123	7B	Supplier P/N#11 (Z)	50	32	00110010
124	7C	Supplier P/N#12 ("Space")	32	20	00100000
125	7D	If <13 char, then terminate with ASCII code 0A1, set remaining char 20h	10	0A	00001010
126	7E	Extension flag	0	00	00000000
127	7F	Checksum	86	56	01010110

9-2. Device addressing (slave address)



9-3. EDID timing characteristics



Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings		Unit	Remark
			Min.	Max.		
Input voltage	V _I	T _a =25°C	-0.3	V _{cc} +0.3	V	[Note]
Supply voltage	V _{edid}	T _a =25°C	0	+6.5	V	

[Note] It applies to DATA_{edid}-CLK_{edid}

Recommended Operating Voltage

Parameter	Symbol	Condition	Ratings		Unit	Remark
			Min.	Max.		
Input voltage	V _I	T _a =25°C	0	V _{cc}	V	[Note]
Supply voltage	V _{edid}	T _a =25°C	2.7	+5.5	V	

[Note] It applies to DATA_{edid}-CLK_{edid}

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
"H" input voltage	V _{IH}	0.7V _{edid}	—	—	V	
"L" input voltage	V _{IL}	—	—	0.3V _{edid}	V	
"L" output voltage	V _{OL}	—	—	0.4	V	I _{OL} =3.0mA
Input leak current	I _{IL}	-1.0	—	1.0	μA	
Output leak current	I _{LO}	-1.0	—	1.0	μA	
Current dissipation (operating)	I _{CC}	—	—	2.0	mA	V _{edid} =5.5V, DATA _{edid} -CLK _{edid} =V _{edid}

AC Characteristics

Parameter	Symbol	High-speed operation mode 4.5V ≤ V _{edid} ≤ 5.5V			Standard operation mode 2.7V ≤ V _{edid} ≤ 5.5V			Unit	Remark
		Min.	Typ.	Max.	Min.	Typ.	Max.		
CLK _{edid} frequency	f _{SCL}	—	—	400	—	—	100	kHz	
CLK _{edid} "H" time	t _{HIGH}	0.6	—	—	4.0	—	—	μs	
CLK _{edid} "L" time	t _{LOW}	1.2	—	—	4.7	—	—	μs	
DATA _{edid} -CLK _{edid} rising time	t _R	—	—	0.3	—	—	1.0	μs	
DATA _{edid} -CLK _{edid} falling time	t _F	—	—	0.3	—	—	0.3	μs	
Start condition hold time	t _{HD:STA}	0.6	—	—	4.0	—	—	μs	
Start condition setup time	t _{SU:STA}	0.6	—	—	4.7	—	—	μs	
Input data hold time	t _{HD:DAT}	0	—	—	0	—	—	ns	
Input data setup time	t _{SU:DAT}	100	—	—	250	—	—	ns	
Output data delay time	t _{PD}	0.1	—	0.9	0.2	—	3.5	μs	
Output data hold time	t _{DH}	0.1	—	—	0.2	—	—	μs	
Stop condition setup time	t _{SU:STO}	0.6	—	—	4.7	—	—	μs	
Bus release time	t _{BUF}	1.2	—	—	4.7	—	—	μs	
Noise removal valid time	t _I	—	—	0.1	—	—	0.1	μs	[Note]

[Note] It applies to DATA_{edid}-CLK_{edid}

10. Optical Characteristics

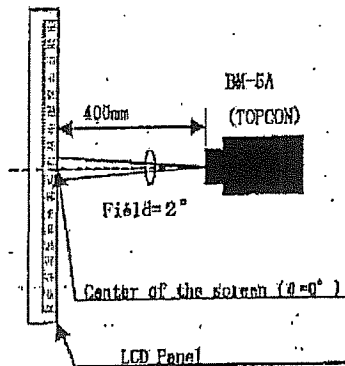
Ta=+25°C, Vcc=+3.3V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	Horizontal	CR>10	45	—	—	Deg.	[Note 1,2,3]
			10	—	—	Deg.	
	Vertical		30	—	—	Deg.	
Contrast ratio	CRn	$\theta = 0^\circ$	150	—	—		[Note 1,3,5]
	CRo	Optimum viewing angle	150	300	—		
Response time	$\tau r + \tau d$	$\theta = 0^\circ$	—	30	60	ms	[Note 1,4,5]
Chromaticity of white	x		0.283	0.313	0.343		[Note 1,5]
	y		0.299	0.329	0.359		
Luminance of white	Y11	160	200	—	cd/m ²	[Note 1,5] IL=6.0mA rms	
		145	180	—		[Note 1,6] FL=52kHz	
White Uniformity	δv		—	1.20	1.45		[Note 1,7]

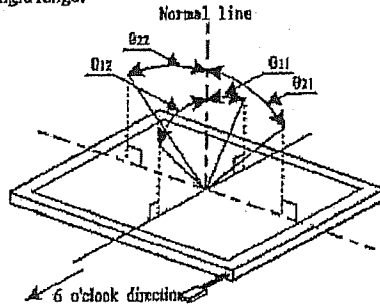
The measurement shall be executed 30 minutes after lighting at rating. Condition : (IL=6.0mA rms)

The optical characteristics shall be measured in a dark room or equivalent.

[Note 1] Optical Characteristics Measurements



[Note 2] Definitions of viewing angle range:



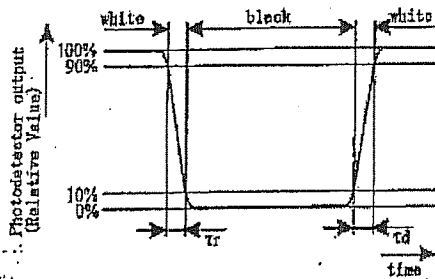
[Note 3] Definition of contrast ratio:

The contrast ratio is defined as the following.

$$\text{Contrast Ratio (CR)} = \frac{\text{Luminance (brightness) with all pixels white}}{\text{Luminance (brightness) with all pixels black}}$$

[Note 4] Definition of response time:

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white".

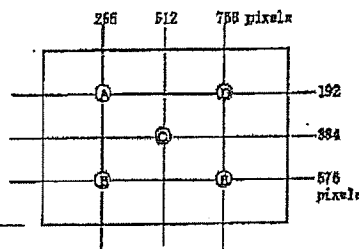


[Note 5] This shall be measured at center of the screen.

[Note 6] Average of five point (A~E)

[Note 7] Definition of white uniformity:

White uniformity is defined as the following with five measurements (A~E).



$$W = \frac{\text{Maximum Luminance of five points (brightness)}}{\text{Minimum Luminance of five points (brightness)}}$$

