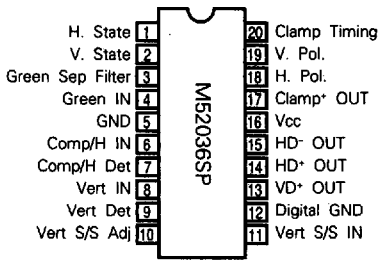
M52036SP

SYNC SIGNAL PROCESSOR

DESCRIPTION

The M52036SP is a semiconductor integrated circuit which selects automatically one of the three sync signals separate sync (bipolar 1~5$V_{p\text{-}p}$), composite sync (bipolar 1~5$V_{p\text{-}p}$) and sync on video (sync negative) and also shapes the waveform of the signal thus selected. It is most suitable for processing the sync signals for automatic tracking type displays.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4B

FEATURES

- Sync signal input and its polarity are detectable.
- Open collector output from pulse output terminal
- Clamp pulse output. Clamp pulse is triggered at the front edge for separate sync and composite sync inputs, and at the rear edge for sync on video input (front edge when pin ① is Hi, rear edge when Lo).
- 20 pin shrink DIP

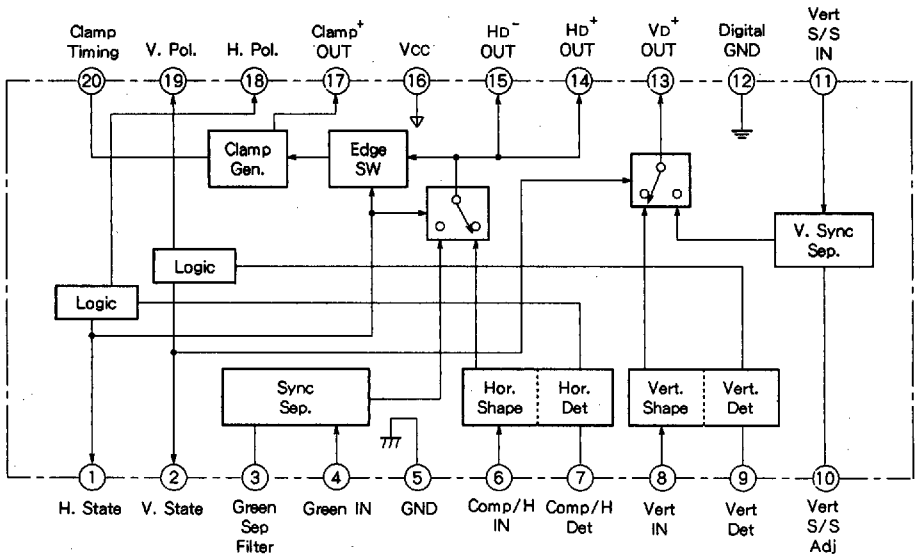
APPLICATION

Display monitor

RECOMMENDED OPERATING CONDITION

Supply voltage range ..... 11~13V
Rated supply voltage 12V

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	14.0	V
P_d	Internal power dissipation	1000	mW
T_{opr}	Operating temperature	−20~85	℃
T_{stg}	Storage temperature	−40~150	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions: Switch condition 4	6	8	16	Input terminal	Input condition	Output terminal	Output waveform	Limits: Min.	Typ.	Max.	Unit	Remark
Icc	Circuit current	2	2	2	2	16		A		25	35	45	mA	No input to pins ④, ⑥, and ⑧. Connect to GND by means of C-cutting. V_{CC} should be opened.
1OH	Pin ① output Hi − level	2	1	1	1	6	7.5µs 16kHz 1V_{P-P}	1	DC	4.0	5.0	5.3	V	
						8	7.5µs 16kHz 1V_{P-P}							
1OL	Pin ① output Low − level	2	1	1	1	6	7.5µs 16kHz 0.7V_{P-P}	1	DC	−	−	0.5	V	0.7 Vp-p of input signal is equivalent to NO SYNC.
						8	7.5µs 16kHz 0.7V_{P-P}							
2OH	Pin ② output Hi − level	2	1	1	1	6	7.5µs 16kHz 1V_{P-P}	2	DC	4.0	5.0	5.3	V	
						8	7.5µs 16kHz 1V_{P-P}							
2OL	Pin ② output Low − level	2	1	1	1	6	7.5µs 16kHz 0.7V_{P-P}	2	DC	−	−	0.5	V	0.7 Vp-p of input signal is equivalent to NO SYNC.
						8	7.5µs 16kHz 0.7V_{P-P}							
18OH	Pin ⑱ output Hi − level	2	1	1	1	6	7.5µs 16kHz 1V_{P-P}	18	DC	4.0	5.0	5.3	V	
						8	7.5µs 16kHz 1V_{P-P}							

For truth table, refer to Table 1.

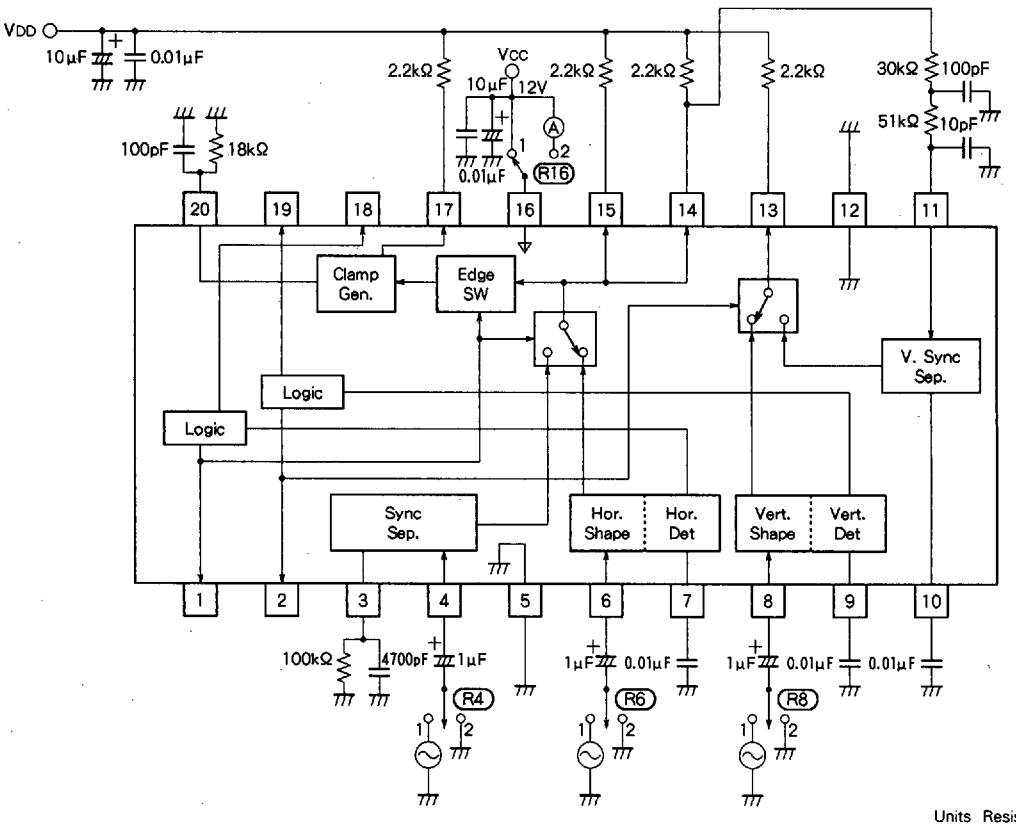
ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test conditions: Switch condition 4	6	8	16	Input terminal	Input condition	Output terminal	Output waveform	Limits: Min.	Typ.	Max.	Unit	Remark
18OL	Pin ⑱ output Low – level	2	1	1	1	6	7.5µs 16kHz 1VP-P	18	DC	–	–	0.5	V	For truth table, refer to Table 1.
						8	7.5µs 16kHz 1VP-P							
19OH	Pin ⑲ output Hi – level	2	1	1	1	6	7.5µs 16kHz 1VP-P	19	DC	4.0	5.0	5.3	V	
						8	7.5µs 16kHz 1VP-P							
19OL	Pin ⑲ output Low – level	2	1	1	1	6	7.5µs 16kHz 1VP-P	19	DC	–	–	0.5	V	
						8	7.5µs 16kHz 1VP-P							
V_{IO}	Threshold voltage	2	2	2	1			10	DC	0.7	1.0	1.4	V	
SS – NV	Sync – Sep Sync input signal Max. noise amplitude	1	2	2	1	4	1.5µs 16kHz 0.1VP-P	14	No pulse output permitted.	–	–	0.1	V	Input signal, 0.1 Vp – p , is for noise simulation
SS – LV	Sync – Sep Sync input signal Min. amplitude	1	2	2	1	4	1.5µs 16kHz 0.2VP-P	14	16kHz No pulse output permitted in the indicated zone.	0.2	–	–	V	Confirm no malfunction produced by noise.
15OL	Pin ⑮ HD^- output Low – level	2	1	2	1	6	7.5µs 16kHz 1VP-P	15	.....V Meas	–	–	0.5	V	
14OL	Pin ⑭ HD^+ output Low – level	2	1	2	1	6	7.5µs 16kHz 1VP-P	14	.....V Meas	–	–	0.5	V	
17OL	Pin ⑰ CP^+ output Low –	2	1	2	1	6	7.5µs 16kHz 1VP-P	17	.....V Meas	–	–	0.5	V	
13OL	Pin ⑬ VD^+ output Low – level	2	2	1	1	8	7.5µs 16kHz 1VP-P	13	.....V Meas	–	–	0.5	V	

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test conditions: Switch condition 4	6	8	16	Input terminal	Input condition	Output terminal	Output waveform	Limits: Min.	Typ.	Max.	Unit	Remark
HD^-–DA	HD^-– Delay time (A)	2	1	2	1	6	7.5µs 16kHz 1Vp-p	15	Input (50%) Time Meas (50%) Output	–	120	350	ns	
HD^-–DB	HD^-– Delay time (B)	2	1	2	1	6	7.5µs 16kHz 1Vp-p	15	Input (50%) Time Meas (50%) Output	–	150	350	ns	
HD^+–DA	HD^+– Delay time (A)	2	1	2	1	6	7.5µs 16kHz 1Vp-p	14	Input (50%) Time Meas (50%) Output	–	120	350	ns	
HD^+–DB	HD^+– Delay time (B)	2	1	2	1	6	7.5µs 16kHz 1Vp-p	14	Input (50%) Time Meas (50%) Output	–	100	350	ns	
CP^+–DT	CP^+– Delay time	2	1	2	1	6	7.5µs 16kHz 1Vp-p	17	Input (50%) Time Meas (50%) Output	–	120	350	ns	
CP^+–PW	CP^+–PULSE – WIDTH	2	1	2	1	6	7.5µs 16kHz 1Vp-p	17	Time Meas	450	700	950	ns	
VD^+–DA	VD^+– Delay time (A)	2	2	1	1	8	7.5µs 16kHz 1Vp-p	13	Input (50%) Time Meas (50%) Output	–	120	350	ns	
VD^+–DB	VD^+– Delay time (B)	2	2	1	1	8	7.5µs 16kHz 1Vp-p	13	Input (50%) Time Meas (50%) Output	–	100	350	ns	

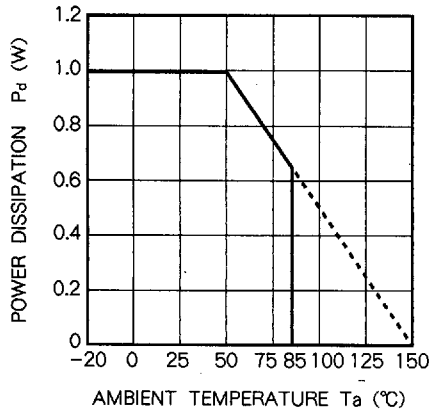
TEST CIRCUIT



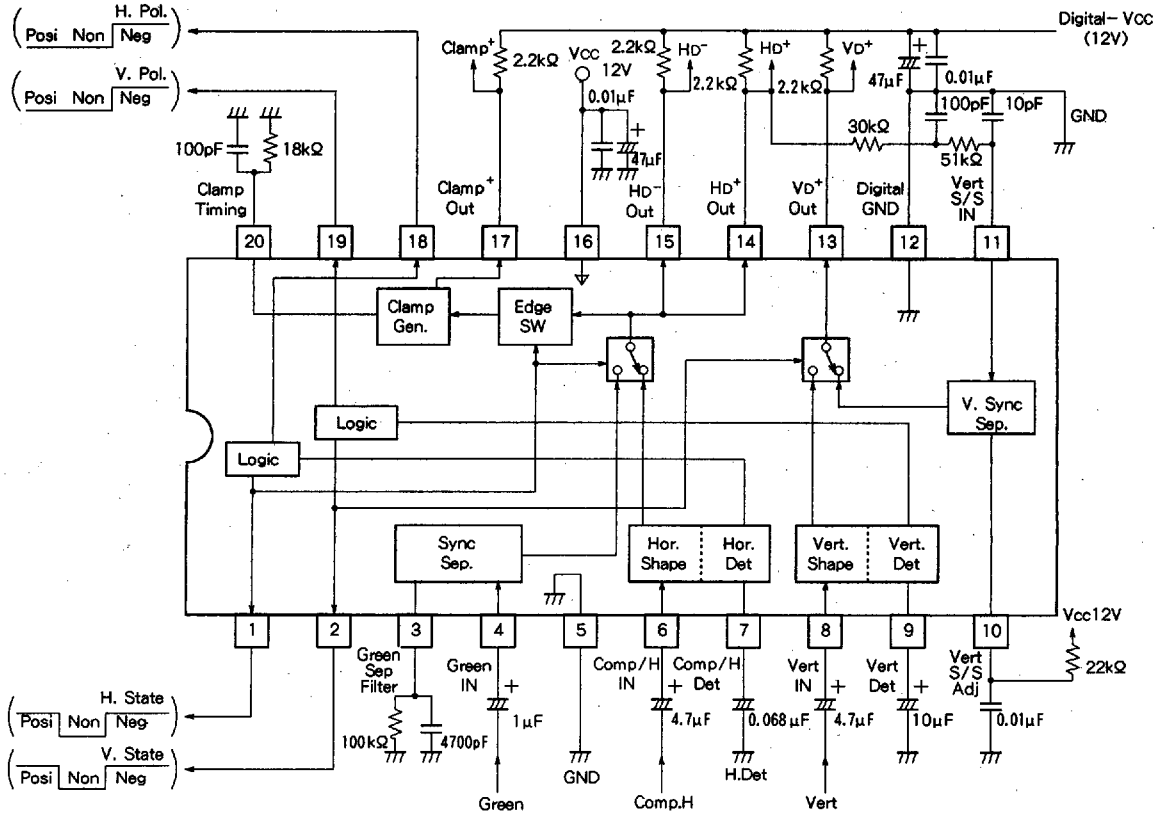
Units Resistance: Ω
Capacitance: F

TYPICAL CHARACTERISTICS

THERMAL DERATING (MAXIMUM RATING)

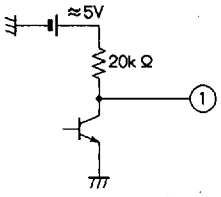
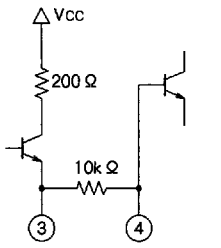
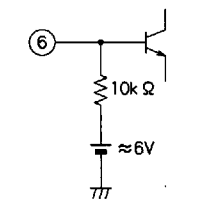
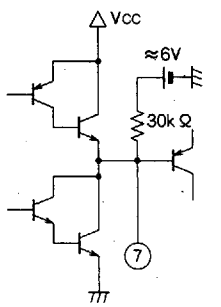


APPLICATION EXAMPLE (fH = 15kHz, fV = 60Hz)

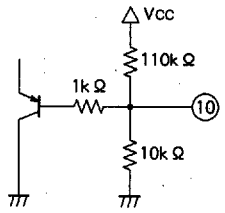
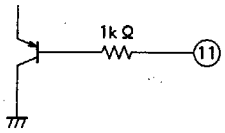
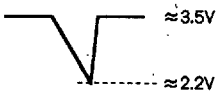
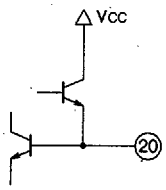


Units Resistance: Ω
Capacitance: F

DESCRIPTION OF PIN

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description of pin
①	H. State	0VDC or 5VDC		Logic output pin for horizontal sync signal. H, L or H appears depending on the input signal to pin ⑥ of positive, empty or negative.
②	V. State	0VDC or 5VDC	Same as pin ①	Logic output pin for vertical sync signal. H, L or H appears depending on the input signal to pin ⑧ of positive, empty or negative.
③	Green Sep Filter	When opened ≈4V		Green(Video)Sep. Filter pin, which is self-biased by the time constant of the capacitor and resistor installed externally. Being of discharging type, this resistor improves the response of the self-biasing circuit. A resistor of lower capacitance reduces the gain of the self-biasing circuit.
④	Green IN	When opened ≈4V		Green(Sync on Video)input pin. Using a C-connection, a green(sync on video) signal is input. The sync has a negative polarity.
⑤	GND	——	——	Grounding
⑥	Comp/H IN	When opened ≈6V		Composite sync/H sync input pin with a bias of approximately 6 V and impedance of 10kΩ. Waveform shaping and polarity detection is performed by an internally installed double threshold converter. The most suitable input amplitude is approximately 1.5 Vp−p. Waveform shaping and polarity detection can be made to a duty of approximately 50%.
⑦	Comp/H Det	When opened ≈6V (Non-signal)		An externally installed capacitor is required as a filter for polarity detection and no-signal input detection. The larger the capacitance, the smaller the ripple and malfunctioning is reduced. However, the detection response time is lengthened.
⑧	Vert IN	When opened ≈6V	Same as pin ⑥	V sync input pin Same as pin ⑥
⑨	Vert Det	When opened ≈6V (Non-signal)	Same as pin ⑦	Same as pin ⑦

DESCRIPTION OF PIN (cont.)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description of pin
⑩	Vert S/S Adj	When opened ≈1V		Vert s/s Adj pin If no external sdjustment is made, the threshold is approxi mately 1 V.
⑪	Vert S/S IN	——		Vert s/s IN pin The composite sync signal is externally integrated, and the result-ing signal is entered for V – sync separation.
⑫	Digital GND	——	——	Grounding
⑬	VD^+ OUT			VD^+ pulse output pin Being of open collector output type, this pin can adjust the output amplitude. Approximately 6 mA can be charged.
⑭	HD^+ OUT	——	Same as pin ⑬	HD^+ pulse output pin Same as pin ⑬
⑮	HD^- OUT	——	Same as pin ⑬	HD^- pulse output pin Same as pin ⑬
⑯	Vcc	12V	——	Power supply
⑰	$Clamp^+$ OUT	——	Same as pin ⑬	$Clamp^+$ pulse output pin Same as pin ⑬
⑱	H. Pol.	0VDC or 5VDC	Same as pin ①	Logic output pin for horizontal sync signal. "L," "L" or "H" appears corresponding to "positive," "non" or "negative" of the input signal to pin ⑧.
⑲	V. Pol.	0VDC or 5VDC	Same as pin ①	Logic output pin for vertical sync signal. "L," "L" or "H" appears corresponding to "positive," "non" or "negative" of the input signal to pin ⑧.
⑳	Clamp Timing			Clamp timing pin The clamp pulse width depends on the capacitor and resistor installed externally. Larger capacity capacitor and resitor will increase the clamp pulse width.

LOGIC TABLE

TABLE 1 DECODER LOGIC OUTPUT

Pin ⑥ input HD. COMP.	Pin ⑧ input VD	Output pin ①	②	⑱	⑲
HD. COMP.(POS.)	NON	H	L	L	L
HD. COMP.(POS.)	VD (POS.)	H	H	L	L
HD. COMP.(POS.)	VD (NEG.)	H	H	L	H
HD. COMP.(NEG.)	NON	H	L	H	L
HD. COMP.(NEG.)	VD (POS.)	H	H	H	L
HD. COMP.(NEG.)	VD (NEG.)	H	H	H	H
NON	NON	L	L	L	L
NON	VD (POS.)	L	H	L	L
NON	VD (NEG.)	L	H	L	H

TABLE 2 ALLOWABLE INPUT AMPLITUDE VOLTAGE

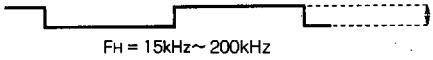
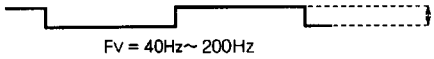
Pin ④ input amplitude	 VV 0~2.1 (VP-P) VS 0.2~0.6 (VP-P)
Pin ⑥ input amplitude	 VS 1.0~5.0 (VP-P) FH = 15kHz~ 200kHz
Pin ⑧ input amplitude	 VS 1.0~5.0 (VP-P) FV = 40Hz~ 200Hz

TABLE 3 OUTPUT PRIORITY

Input signal (pin)			Output signal (pin)		
Pin ④	Pin ⑥	Pin ⑧	Pin ⑭ Pin ⑮	Pin ⑬	Pin ⑰
○	×	×	4	11	4
○	○	×	6	11	6
○	×	○	4	8	4
○	○	○	6	8	6
×	×	×	×	×	×
×	○	×	6	11	6
×	×	○	×	8	×
×	○	○	6	8	6

TABLE 4 PULSE DUTY RATIO OF ALLOWABLE MAXIMUM INPUT SIGNAL

Pin ⑥ input pulse (HD. COMP.) FH = 16kHz

Max. amplitude (VP-P)		1.0	3.3	4.0	5.0
POS.	%	15.0	13.8	11.2	9.0
	Time (μs)	9.38	8.63	7.00	5.63
NEG.	%	15.0	13.0	10.5	8.8
	Time (μs)	9.38	8.13	6.56	5.50

Pin ⑧ input pulse (VD) FV = 60Hz

Max. amplitude (VP-P)		1.0	3.3	4.5	5.0
POS.	%	14.1	12.1	9.8	7.7
	Time (ms)	2.35	2.02	1.63	1.28
NEG.	%	14.8	11.3	9.2	7.5
	Time (ms)	2.47	1.88	1.53	1.25

PRECAUTIONS FOR APPLICATION

1. Input

1) Green (Sync on Video) input (pins ③ and ④)
The input signals must be in sync negative polarity. For sync separation, a method is used in which the sync tip is clamped by a capacitor attached externally to pin ④ and by the C and R attached to pin ③. The sync tip of pin ④ shows approximately 4V.

2) Comp Sync/H sync, V sync input
Connect the composite sync input to pin ⑥. For the separate sync input, connect H and V to pins ⑥ and ⑧ respectively. The bias and impedance at pins ⑥ and ⑧ are 6V and 10kΩ, respectively.
Waveform shaping and polarity detection are performed by a double threshold converter installed inside.
The internal circuit is as shown in Fig. B. The average DC voltage of input signals is V_2. Each threshold voltage is set to approximately 0.7V higher and lower than V_2.
Thus, as shown in Fig. A, this processor is energized by an input signal $0.7V_{p\text{-}p}$ or over when the duty ratio is small. On the other hand, approximately 1.4 $V_{p\text{-}p}$ is suitable when the duty ratio is large. Fig. C indicates an allowable standard value for the input duty.

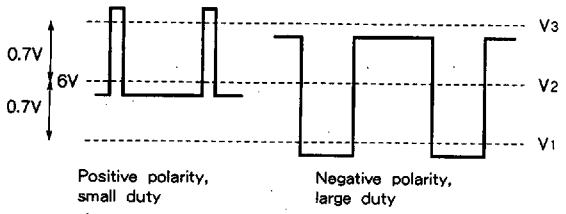


Fig. A

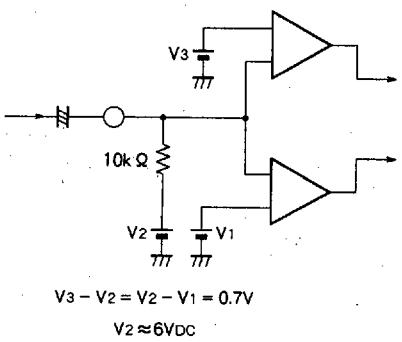


Fig. B

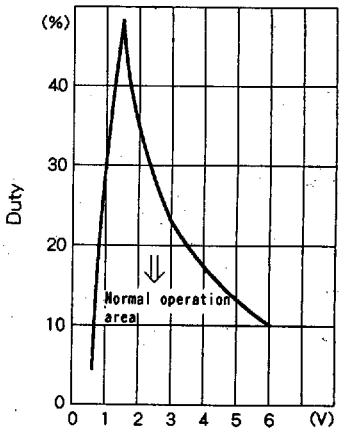


Fig. C

Fig.D shows an example of the measures for improving the allowable duty ratio in a range of $1.4V_{p\text{-}p}$ or over of the input signal.

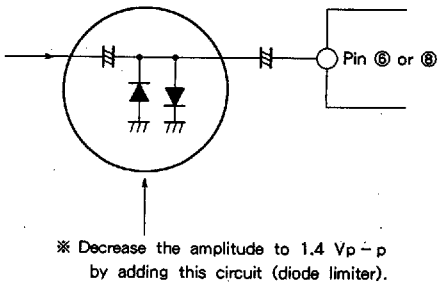


Fig. D

For use in a range outside the specified value, confirm that the waveform complies with Fig.E when measured it after removing the filters in pins ⑦ and ⑨.

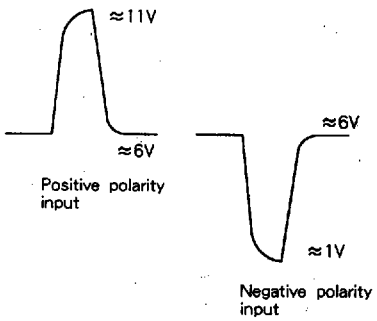


Fig. E

3) Polarity detection and empty input detection (pins ⑦ and ⑨)

A capacitor is required to be installed external as a filter for polarity detection and empty input detection. The larger the capacitance, the smaller the ripple and reduces malfunction. However, the detecting time is lengthened. For an input of 15kHz, a capacitor of 0.05 μF or larger is recommended. For 60Hz, a 10 μF or larger is sufficient. If it is necessary to use a capacitor of smaller capacitance, measure the waveform at the filter terminal under the condition of the lowest frequency of the input sync signal to be used and the smallest duty ratio. And make sure that the signal shows 7.5V (actually 6.6V) or over for a positive polarity input or 4.5V (actually 5.5V) or lower for a negative polarity input.

4) VERT S/S IN (pin ⑪)

For V sync separation, signals are generated by externally integrating composite sync signals, and are then input.

The composite sync signals that are input to pin ⑥ (H + V) are output to pin ⑭ HD^+. For V sync separation, pin ⑭ HD^+ output is externally integrated, and is input to pin ⑪. Check pin ⑪ waveform to see if the H element is adequately low.

In the IC, the sync separation threshold level is set to approximately 1V when no external adjustment is provided.

5) VERT S/S ADJ (pin ⑩)

The threshold voltage is approximately 1V when no external adjustment is provided. The threshold voltage is dependent on IC internal resistance. Pin ⑩ may be open ; however, if noise may give adverse effect, ground the pin with capacitor.

When the H element cannot be lowered sufficiently, connect resistance between pin ⑩ and Vcc to change the threshold level. (Provide resistance such that when V_{DD}(Digital Vcc) is 12V, the threshold voltage will be 8V or less ; and when V_{DD} is 5V, the threshold voltage will be 4V or less.)

When there are serration pulses or other pulses during the V period, provide resistance such that the threshold voltage will be half as high as V_{DD}.

2. CP-Width

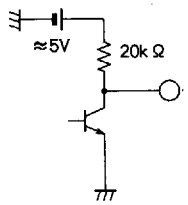
Timing terminal (pin ⑳)

The time constant depends on the current flowing out through pin ⑳ and the capacitance of the timing terminal. The current flowing out through pin ⑳ is usually determined by the terminal voltage and the resistance of externally attached resistor. A pulse width of 0.7 μ sec is obtained by an 18kΩ (or 200 μA) resistor and a 100pF capacitor both installed externally.

3. Output Stage

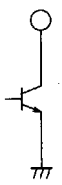
1) Logic output (pins ①, ②, ⑱ and ⑲)

This output system is illustrated in the figure shown below. The internal load resistance of this IC is 20kΩ.



2) Pulse output (pins ⑬, ⑭, ⑮ and ⑰)

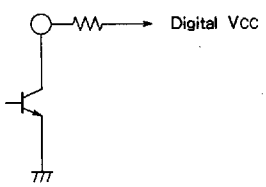
This output system is of open collector type as illustrated in the figure shown below. Approximately 6mA can be charged in.



3) Power Supply

Supply 12V to pin ⑯.

For the pulse output power, supply a digital Vcc of 5 to 12V as illustrated below.



4. Other

Differences between M52036SP and M52346SP

The clamp pulse trigger is different between M52036SP and M52346SP when "S on G" and "H/H + V" are input simultaneously, or when only "H/H + V" is input.

M52036SP·····Generated at the first edge of "H/H + V" input.

M52346SP·····Generated at the latter edge of "H/H + V" input.

M52346SP clamp pulses are generated at the latter edge of signals that have been given priority.

The M52036SP pin configuration is the same as that of M52346SP.